Lecture #21

OUTLINE

- More diode applications
- The MOSFET

Reference Reading

- **Rabaey *et al.***
  - Chapter 3.3.1
- **Howe & Sodini**
  - Chapter 4.1 – 4.3
- **Schwarz and Oldham**
  - Chapter 13.4

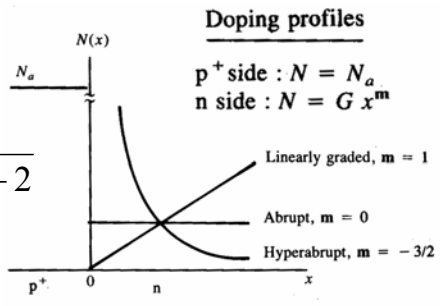
Varactor Diode

- Voltage-controlled capacitor
  - Used in oscillators and detectors
    (*e.g.* FM demodulation circuits in your radios)
  - Response changes by tailoring the doping profile:

$C_j \propto \left(-V_D\right)^{-n}$ where $n = \dfrac{1}{m+2}$

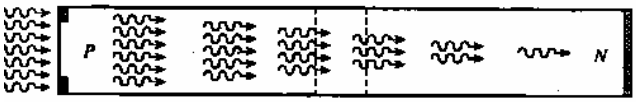
for

$\left|V_D\right| >> \phi_0$



Optoelectronic Diodes (cont'd)

- Light incident on a pn junction generates electron-hole pairs
- The minority carriers which are generated in the depletion region, and the minority carriers which are generated in the quasi-neutral regions and then diffuse into the depletion region, are swept across the junction by the electric field



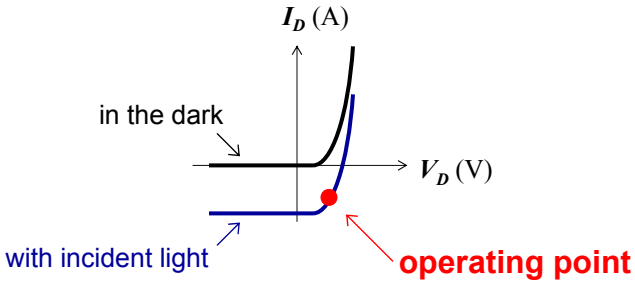
- This results in an additional component of current flowing in the diode:

$$I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$$

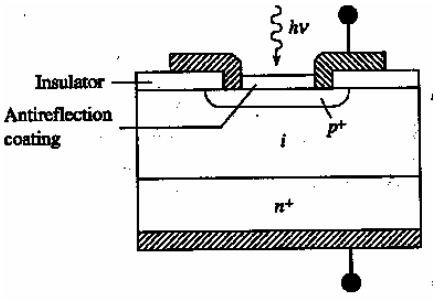
where $I_{optical}$ is proportional to the intensity of the light

Photovoltaic (Solar) Cell

$$I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$$

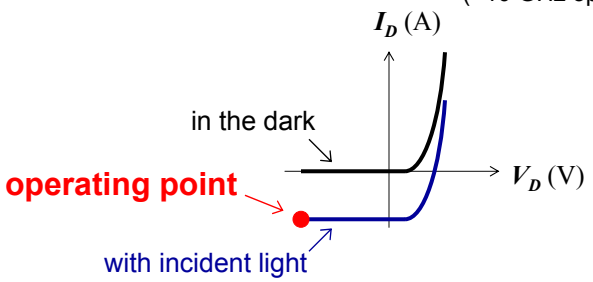


Photodiode



- An intrinsic region is placed between the p-type and n-type regions
  - $W_j \cong W_{\text{i-region}}$, so that most of the electron-hole pairs are generated in the depletion region

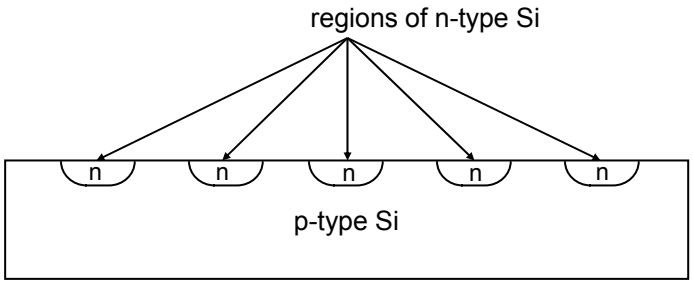
    → faster response time (~10 GHz operation)



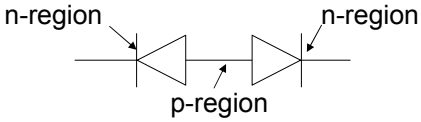
Why are pn Junctions Important for ICs?

- The basic building block in digital ICs is the MOS transistor, whose structure contains reverse-biased diodes.
  - pn junctions are important for electrical isolation of transistors located next to each other at the surface of a Si wafer.
  - The junction capacitance of these diodes can limit the performance (operating speed) of digital circuits

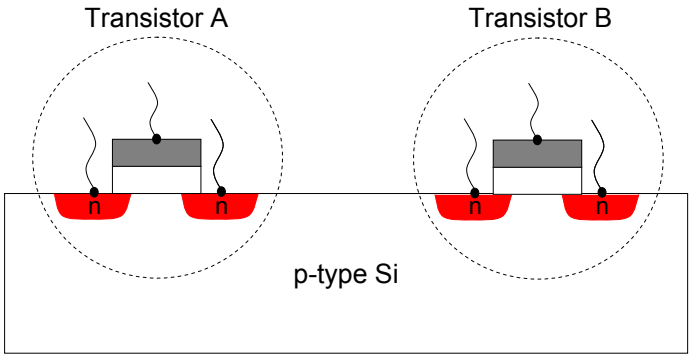
Device Isolation using pn Junctions



No current flows if voltages are applied between n-type regions, because two pn junctions are “back-to-back”



=> n-type regions **isolated** in p-type substrate and vice versa



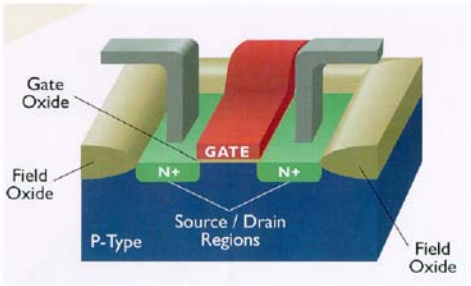
We can build large circuits consisting of many transistors without worrying about current flow between devices. The p-n junctions **isolate** the transistors because there is always at least one **reverse-biased** p-n junction in every potential current path.

Modern Field Effect Transistor (FET)

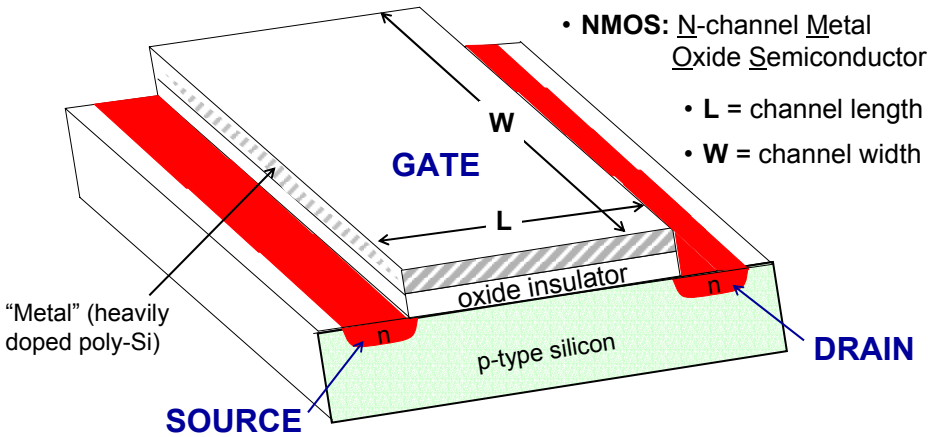
- An electric field is applied normal to the surface of the semiconductor (by applying a voltage to an overlying electrode), to modulate the conductance of the semiconductor

→ Modulate drift current flowing between 2 contacts ("source" and "drain") by varying the voltage on the "gate" electrode

Metal-oxide-semiconductor (MOS) FET:



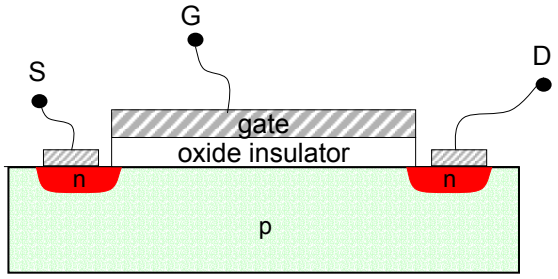
MOSFET



- **NMOS:** N-channel Metal Oxide Semiconductor
- **L** = channel length
- **W** = channel width

- A GATE electrode is placed above (electrically insulated from) the silicon surface, and is used to control the resistance between the SOURCE and DRAIN regions

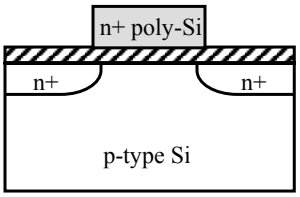
N-channel MOSFET



- Without a gate voltage applied, no current can flow between the source and drain regions.
- Above a certain gate-to-source voltage (***threshold voltage V_T***), a conducting layer of mobile electrons is formed at the Si surface beneath the oxide. These electrons can carry current between the source and drain.

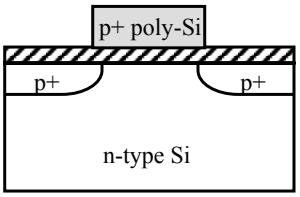
N-channel *vs.* P-channel MOSFETs

NMOS



- For current to flow, $V_{GS} > V_T$
- Enhancement mode: $V_T > 0$
- Depletion mode: $V_T < 0$
  - Transistor is ON when V_G=0V

PMOS

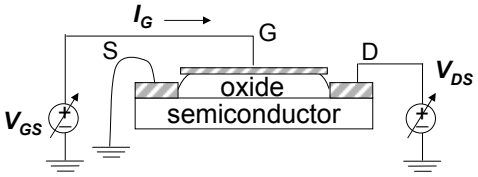


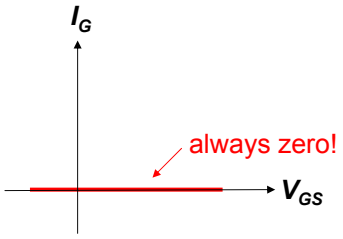
- For current to flow, $V_{GS} < V_T$
- Enhancement mode: $V_T < 0$
- Depletion mode: $V_T > 0$
  - Transistor is ON when V_G=0V

("n+" denotes very heavily doped n-type material; "p+" denotes very heavily doped n-type material)

NMOSFET I_G vs. V_{GS} Characteristic

Consider the current I_G (flowing into **G**) versus V_{GS}:

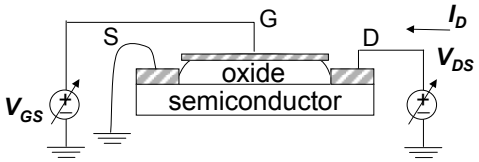


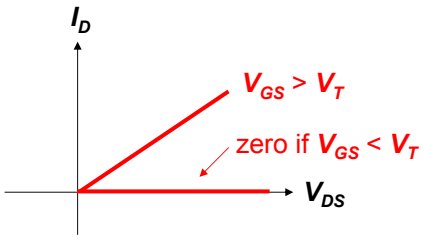


The gate is insulated from the semiconductor, so there is no significant gate current.

NMOSFET I_D vs. V_{DS} Characteristics

Next consider I_D (flowing into **D**) versus V_{DS}, as V_{GS} is varied:





Above threshold ($V_{GS} > V_T$): "inversion layer" of electrons appears, so conduction between **S** and **D** is possible

Below "threshold" ($V_{GS} < V_T$): no charge → no conduction