Lecture #24

OUTLINE

- The common-source (CS) amplifier
  - load line analysis
  - DC bias circuit example
  - small-signal analysis of CS amplifier

Reference Reading

- **Howe & Sodini:** Chapter 8.1, 8.3
- **Hambley** (posted online)**:** Chapter 12.2-12.5

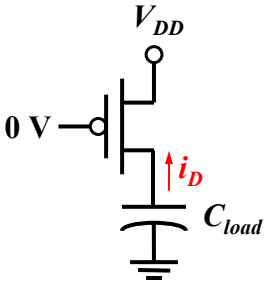
Notation

- Subscript convention (Lecture 2, Slide 11):
  - $V_{DS} \equiv V_D - V_S$, $V_{GS} \equiv V_G - V_S$, *etc.*
- Double-subscripts denote DC sources (Lecture 23, Slide 7):
  - V_{DD} , V_{CC} , I_{SS} , *etc.*
- To distinguish between DC and AC components of an electrical quantity, the following convention is used:
  - DC quantity: upper-case letter with upper-case subscript
    - I_D , V_{DS} , *etc.*
  - AC quantity: lower-case letter with lower-case subscript
    - i_d , v_{ds} , *etc.*
  - Total (DC + AC) quantity:

    lower-case letter with upper-case subscript
    - i_D , v_{DS} , *etc.*

P-Channel MOSFET Example

- In a digital circuit, a p-channel MOSFET in the ON state is typically used to charge a capacitor connected to its drain terminal:
  - gate voltage V_G = **0 V**
  - source voltage $V_S = V_{DD}$ (power-supply voltage)
  - drain voltage V_D initially at **0 V**, charging toward V_{DD}

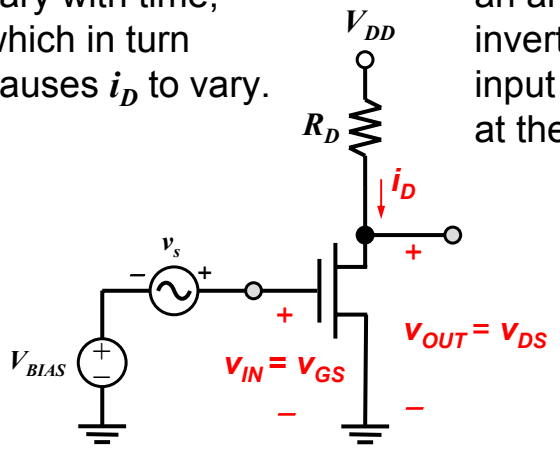


$$R_{eq} \cong \frac{3}{4}\frac{V_{DD}}{\left|I_{DSATp}\right|}\left(1-\frac{5}{6}\lambda_p V_{DD}\right)$$

$$I_{DSAT} = -\frac{k'_p}{2}\frac{W}{L}\left(V_{DD}-\left|V_{Tp}\right|\right)^2$$

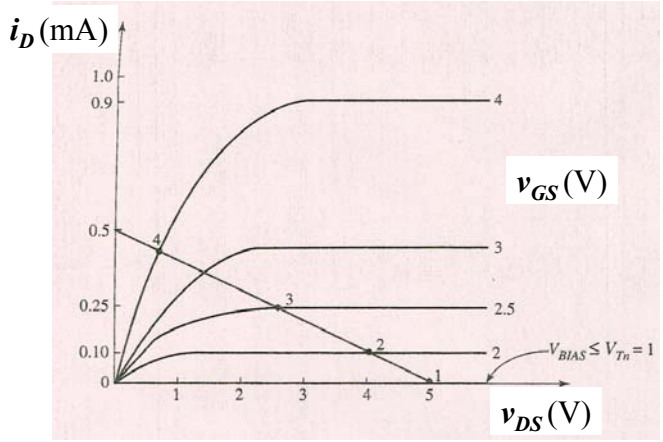
Common-Source (CS) Amplifier

- The input voltage v_s causes v_{GS} to vary with time, which in turn causes i_D to vary.
- The changing voltage drop across R_D causes an amplified (and inverted) version of the input signal to appear at the drain terminal.



Load-Line Analysis of CS Amplifier

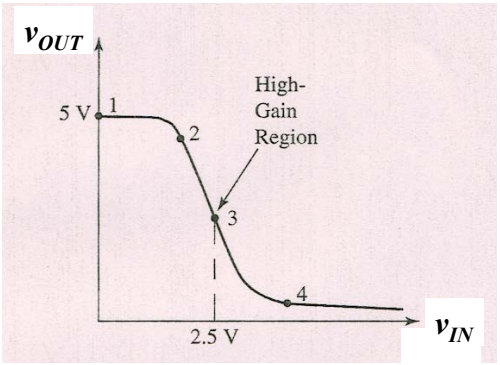
- The operating point of the circuit can be determined by finding the intersection of the appropriate MOSFET i_D *vs.* v_{DS} characteristic and the load line:



load-line equation:

$$V_{DD} = R_D i_D + v_{DS}$$

Voltage Transfer Function



Goal:
Operate the amplifier in the high-gain region, so that small changes in v_{IN} result in large changes in v_{OUT}

(1): transistor biased in cutoff region

(2): $v_{IN} > V_T$; transistor biased in saturation region

(3): transistor biased in saturation region

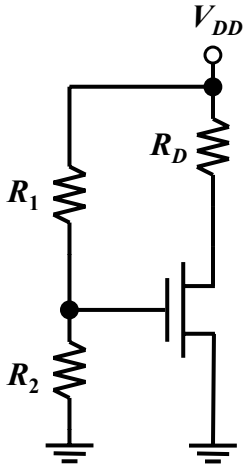
(4): transistor biased in "resistive" or "triode" region

Quiescent Operating Point

- The operating point of the amplifier for zero input signal ($v_s = 0$) is often referred to as the ***quiescent operating point*** or ***Q point***.
  - The Q point should be chosen so that the output voltage is approximately centered between V_{DD} and 0 V.
  - v_s varies the input voltage around the Q point.

  Note: The relationship between v_{OUT} and v_{IN} is not linear; this results in a distorted output voltage signal. If the input signal amplitude is very small, however, we can have amplification with negligible distortion.

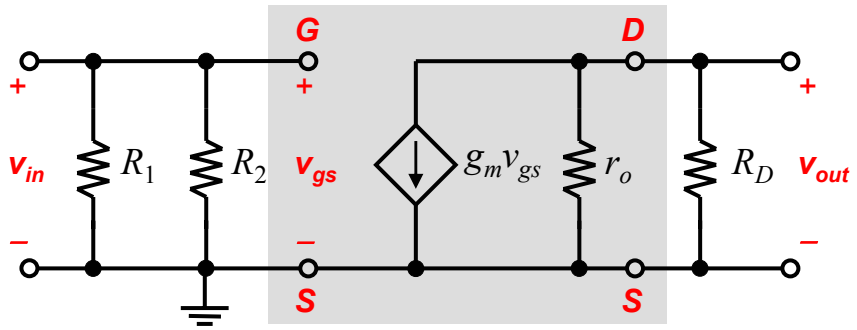
Bias Circuit Example



Rules for Small-Signal Analysis

- A DC supply voltage source acts as a short circuit
  - Even if AC current flows through the DC voltage source, the AC voltage across it is zero.
- A DC supply current source acts as an open circuit
  - Even if AC voltage is applied across the current source, the AC current through it is zero.

Small-Signal Equivalent Circuit



$$v_{out} = -g_m v_{gs}\left(r_o \parallel R_D\right)$$

voltage gain $$A_v = \frac{v_{out}}{v_{in}} = -g_m\left(r_o \parallel R_D\right)$$