Lecture #25

Midterm #2 Information

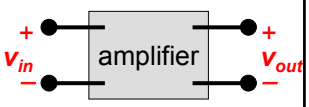
- Date: Monday November 3rd
- Topics to be covered:
  - capacitors and inductors
  - 1st-order circuits (transient response)
  - semiconductor material properties
  - pn junctions & their applications
  - MOSFETs; common-source amplifier
- Review session: Friday October 31st 2-4 PM

OUTLINE

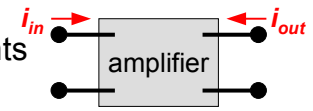
- The transconductance amplifier
  (from Howe & Sodini Chapter 8.1)
- Summary of MOSFET

Amplifier Types

1. Voltage amplifier
   input & output signals are voltages

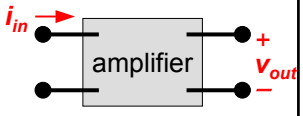


2. Current amplifier
   input and output signals are currents

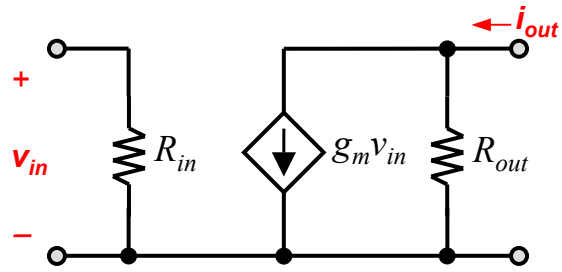


3. Transconductance amplifier
   input signal is voltage;
   output signal is current

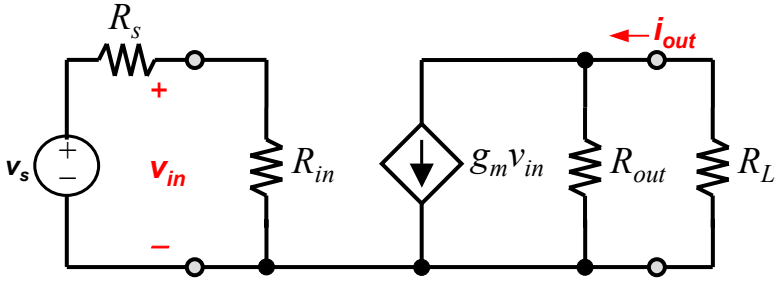
4. Transresistance amplifier
   input signal is current;
   output signal is voltage



Two-Port Amplifier Model for a transconductance amplifier



Effect of Source and Load Resistances

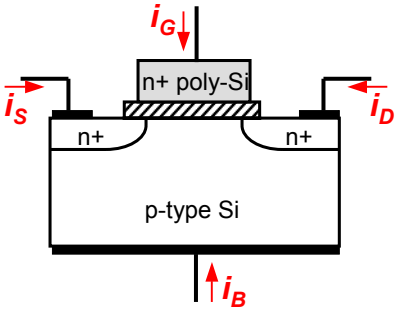


- Overall transconductance is degraded by the source resistance R_s and load resistance R_L

$$\frac{i_{out}}{v_s} = \left(\frac{R_{in}}{R_{in}+R_s}\right) g_m \left(\frac{R_{out}}{R_L+R_{out}}\right)$$

NMOSFET Summary: Current Flow

NMOSFET Structure

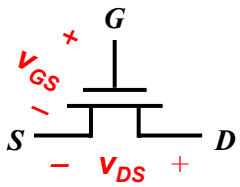


Gate current $i_G = 0$

Body current $i_B = 0$

→ $i_S = -i_D$

NMOSFET Circuit Symbol



If $V_{GS} \leq V_T$, $i_D = 0$

If $V_{GS} > V_T$, $i_D > 0$

Current is limited by either

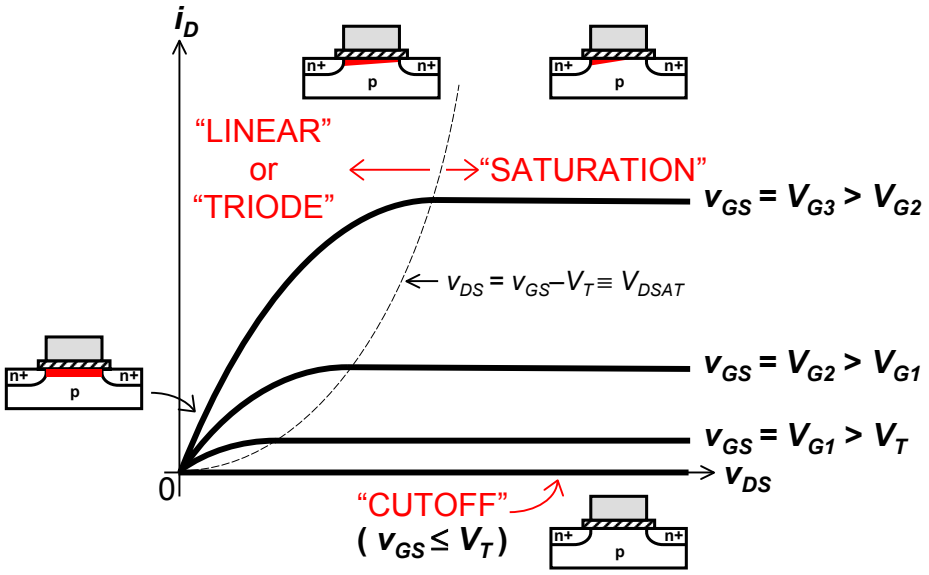
- the resistance of the inversion-charge layer, or
- velocity saturation

NMOSFET Summary: Modes of Operation

- When $V_{GS} \leq V_T$, an n-type channel is not formed.
  → No electrons flow from SOURCE to DRAIN
  "CUTOFF mode"

- When $V_{GS} > V_T$, an n-type channel ("inversion" layer of electrons at the surface of the semiconductor) is formed.
  → Electrons may flow from SOURCE to DRAIN ($i_D > 0$)
  If $V_{DS} < V_{GS}-V_T$, the inversion layer exists across the entire channel length, and current i_D increases with V_{DS}
  "LINEAR mode" or "TRIODE mode"
  If $V_{DS} \geq V_{GS}-V_T$, the inversion layer is pinched off at the drain end, and current i_D does not increase with V_{DS}
  "SATURATION mode"

NMOSFET Summary: *I-V* Characteristics



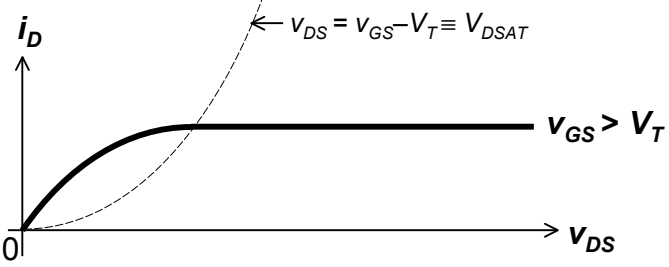
NMOSFET Summary: *I-V* Equations

"LINEAR" or "TRIODE"

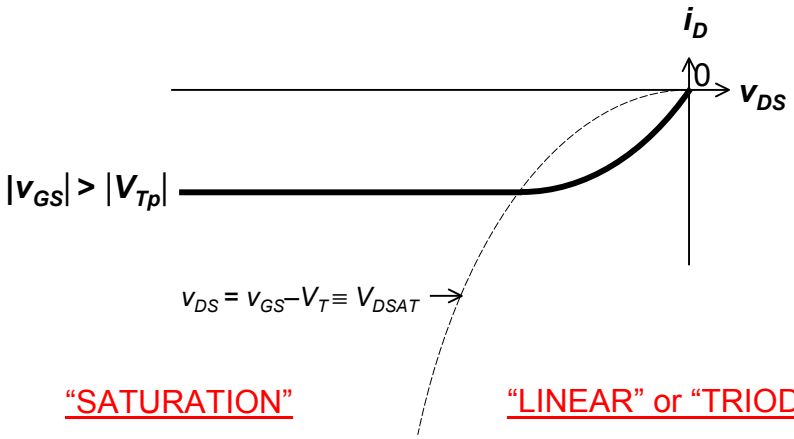
$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

"SATURATION"

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2$$



PMOSFET *I-V* Equations



"SATURATION" "LINEAR" or "TRIODE"

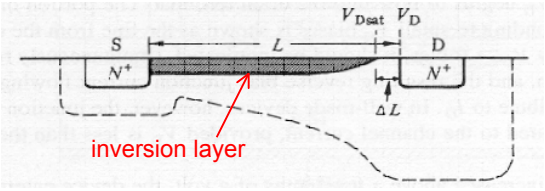
$$I_{DSAT} = -\frac{k'_p}{2}\frac{W}{L}\left(V_{GS} - V_{Tp}\right)^2 \qquad I_D = -k'_p\frac{W}{L}\left[V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right]V_{DS}$$

NMOSFET Summary: Non-Ideal Behavior

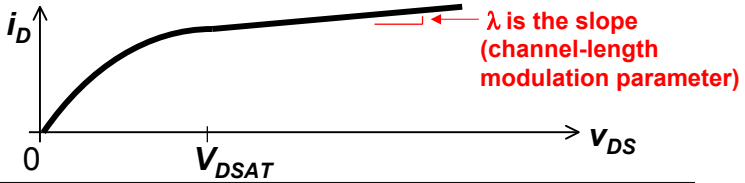
Channel-length modulation:

- The length of the pinch-off region, ΔL, increases with increasing V_{DS} above $V_{GS}-V_T$. It reduces the length of the inversion layer and hence the resistance of this layer.

cross-sectional view of channel:



→ i_D increases noticeably with V_{DS}, if L is small



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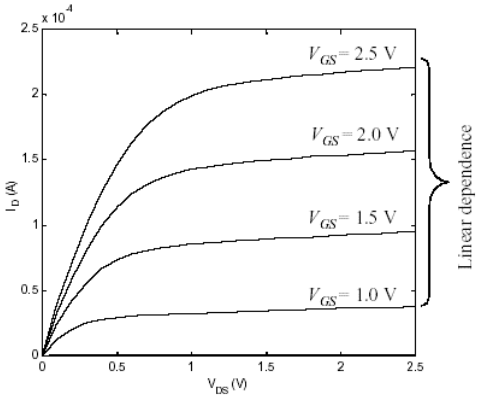
Velocity Saturation:

- In a very-short-channel MOSFET, i_D saturates because the carrier velocity is limited to ~10^7 cm/sec

  → i_D reaches a limit before pinch-off occurs



$$I_{DSAT} = WC_{ox}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]v_{sat}$$

where $V_{DSAT} = \frac{L}{\mu_n}v_{sat}$ < V_{GS}–V_T

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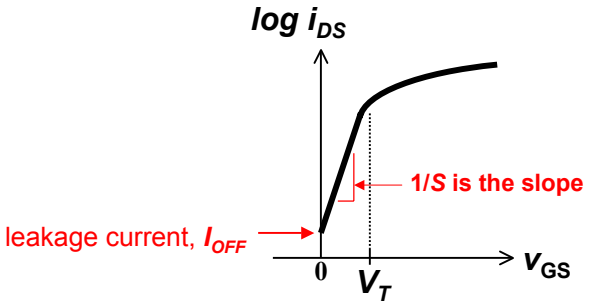
Subthreshold Leakage:

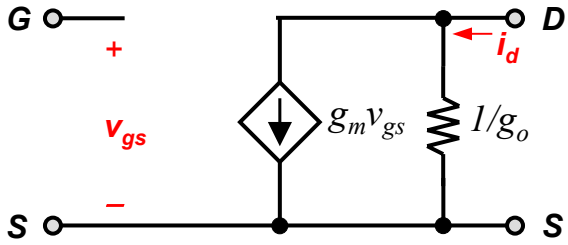
- For $V_{GS} \leq V_T$, i_D is exponentially dependent on V_{GS}:



- The leakage current specification sets the lower limit for the threshold voltage V_T

NMOSFET Summary: Circuit Models

- For analog circuit applications (where we are concerned only with *changes* in current and voltage signals, rather than their total values), the small-signal model is used:

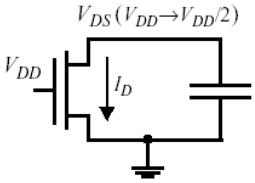


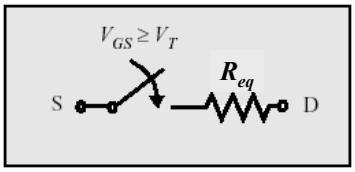
transconductance $g_m \cong \frac{W}{L} k_n' (V_{GS} - V_T)$

output conductance $g_o \cong \lambda I_D$ where V_{GS} **&** I_D are the DC bias (Q point) values

NMOSFET Summary: Circuit Models

- For digital circuit applications, the MOSFET is modeled as a resistive switch:





$$R_{eq} \cong \frac{3}{4} \frac{V_{DD}}{I_{DSATn}} \left(1 - \frac{5}{6} \lambda_n V_{DD}\right)$$

$$I_{DSATn} = \frac{k_n'}{2} \frac{W}{L} (V_{DD} - V_{Tn})^2$$