Lecture #26

ANNOUNCEMENTS

• Extra Office Hours this week:
  – Prof. King: Thursday 10/30 12-2 PM
  – Steve: Friday 10/31 12-2 PM
  – Farhana:
• Review session: Friday 10/31 2-4 PM, 120 Latimer

OUTLINE

• Logic functions
• NMOS logic gates
• The CMOS inverter

Reading

• Schwarz & Oldham: Chapters 11.2, 15.3
• Rabaey et al.: Chapter 5.2

Digital Signals

• For a digital signal, the voltage must be within one of two ranges in order to be defined:

  ![Digital Signal Diagram]

  \[V_{DD}, V_{OH}, V_{IH}, V_{IL}, V_{OL}, 0\text{ Volts} \]

  • Positive Logic:
    – “low” voltage \(\equiv\) logic state 0
    – “high” voltage \(\equiv\) logic state 1
### Logic Functions, Symbols, & Notation

<table>
<thead>
<tr>
<th>NAME</th>
<th>SYMBOL</th>
<th>NOTATION</th>
<th>TRUTH TABLE</th>
</tr>
</thead>
</table>
| “NOT”   | ![Diagram](NOT.png) | $F = \overline{A}$ | \[
|         |        |          | A | F | 0 | 1 |
|         |        |          | 1 | 0 |
| “OR”    | ![Diagram](OR.png)  | $F = A + B$ | \[
|         |        |          | A | B | F |
|         |        |          | 0 | 0 | 0 |
|         |        |          | 0 | 1 | 1 |
|         |        |          | 1 | 0 | 1 |
|         |        |          | 1 | 1 | 1 |
| “AND”   | ![Diagram](AND.png) | $F = A \cdot B$ | \[
|         |        |          | A | B | F |
|         |        |          | 0 | 0 | 0 |
|         |        |          | 0 | 1 | 0 |
|         |        |          | 1 | 0 | 0 |
|         |        |          | 1 | 1 | 1 |
| “NOR”   | ![Diagram](NOR.png) | $F = A + B$ | \[
|         |        |          | A | B | F |
|         |        |          | 0 | 0 | 1 |
|         |        |          | 0 | 1 | 0 |
|         |        |          | 1 | 0 | 0 |
|         |        |          | 1 | 1 | 0 |
| “NAND”  | ![Diagram](NAND.png) | $F = \overline{A} \cdot \overline{B}$ | \[
|         |        |          | A | B | F |
|         |        |          | 0 | 0 | 1 |
|         |        |          | 0 | 1 | 1 |
|         |        |          | 1 | 0 | 1 |
|         |        |          | 1 | 1 | 0 |
| “XOR”   | ![Diagram](XOR.png) | (exclusive OR) $F = A + B$ | \[
|         |        |          | A | B | F |
|         |        |          | 0 | 0 | 0 |
|         |        |          | 0 | 1 | 1 |
|         |        |          | 1 | 0 | 1 |
|         |        |          | 1 | 1 | 0 |
NMOS Inverter ("NOT" Gate)

Circuit:

\[ v_{DS} = v_{OUT} - i_D + v_{IN} - V_{DD} \]

Voltage-Transfer Characteristic:

\[ v_{GS} = v_{in} \leq V_T \]

Noise Margins

Definition of Input Levels

\[ V_{OL}, V_{IL}, V_{OH}, V_{IH} \]

Logic swing:

\[ V_{sw} = V_{OH} - V_{OL} \]

Definition of Noise Margins

\[ V_{OH}, V_{IL}, NM_H, NM_L \]

Noise margin high:

\[ NM_H = V_{OH} - V_{IH} \]

Noise margin low:

\[ NM_L = V_{IL} - V_{OL} \]
NMOS NAND Gate

- Output is low only if both inputs are high

\[\begin{array}{ccc}
V_{DD} & R_D & F \\
A & B & F \\
0 & 0 & 1 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}\]

NMOS NOR Gate

- Output is low if either input is high

\[\begin{array}{ccc}
V_{DD} & R_D & F \\
A & B & F \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 0 \\
\end{array}\]
**Disadvantages of NMOS Logic Gates**

- Large values of $R_D$ are required in order to
  - achieve a low value of $V_{OL}$
  - keep power consumption low

→ Large resistors are needed, but these take up a lot of space.

- One solution is to replace the resistor with an NMOSFET that is always on.

---

**The CMOS Inverter: Intuitive Perspective**

**CIRCUIT**

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>$G$</th>
<th>$S$</th>
<th>$D$</th>
<th>$V_{OUT}$</th>
</tr>
</thead>
</table>

**SWITCH MODELS**

- $V_{IN} = V_{DD}$
- $V_{OL} = 0$ V
- $V_{OH} = V_{DD}$

- $V_{IN} = 0$ V

Low static power consumption, since one MOSFET is always off in steady state.
**CMOS Inverter Voltage Transfer Characteristic**

- **A**: N: off, P: lin
- **B**: N: lin, P: on
- **C**: N: lin, P: sat
- **D**: N: sat, P: lin
- **E**: N: sat, P: sat

**CMOS Inverter Load-Line Analysis**

- $V_{IN} = V_{DD} + V_{GSp}$
- $V_{OUT} = V_{DD} + V_{DSP}$

- $I_{Dn} = -I_{Dp}$

- Increasing $V_{IN}$:
  - $V_{IN} = 0$ V
  - $V_{IN} = V_{DD}$
  - $V_{IN} = V_{DSn}$

- Increasing $V_{OUT}$:
  - $V_{DSP} = 0$

EECS40, Fall 2003  Lecture 26, Slide 11  Prof. King

EECS40, Fall 2003  Lecture 26, Slide 12  Prof. King
CMOS Inverter Load-Line Analysis: Region A

\[ V_{IN} \leq V_{Tn} \]

\[ I_{Dn} = -I_{Dp} \]

CMOS Inverter Load-Line Analysis: Region B

\[ V_{DD}/2 > V_{IN} > V_{Tn} \]

\[ I_{Dn} = -I_{Dp} \]
CMOS Inverter Load-Line Analysis: Region D

\[ V_{DD} - |V_Tp| > V_{IN} > V_{DD}/2 \]

\[ I_{Dn} = -I_{Dp} \]

CMOS Inverter Load-Line Analysis: Region E

\[ V_{IN} > V_{DD} - |V_Tp| \]

\[ I_{Dn} = -I_{Dp} \]