

Lecture #27

ANNOUNCEMENTS

- Extra Office Hours this week:
 - Prof. King: Thu. 10/30 1:15-2 PM
 - Steve: Fri. 10/31 12-2 PM
 - Farhana: Sat. 11/1 4-5 PM; Sun. 11/2 3-5 PM
(regular office hours cancelled next week)

OUTLINE

- The CMOS inverter (cont'd)
- CMOS logic gates
- The body effect

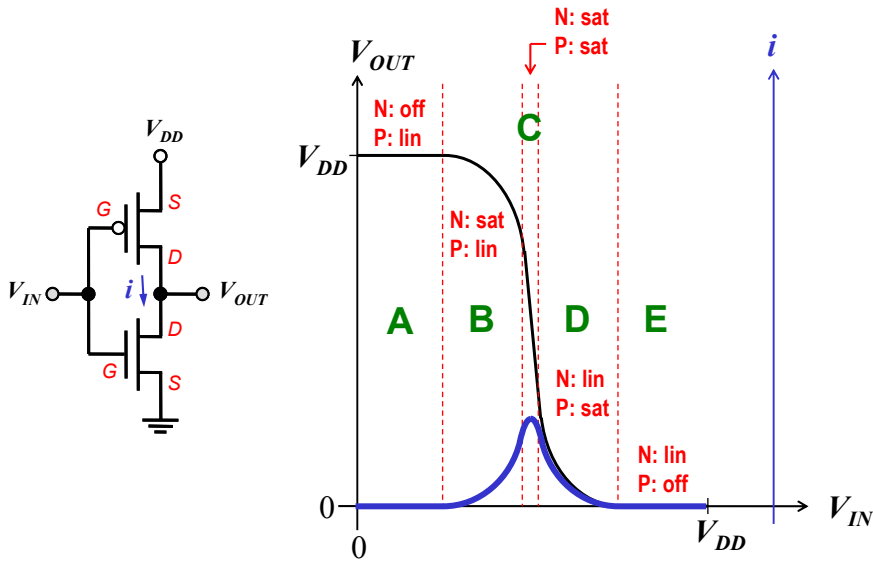
Reading (Rabaey *et al.*)

Chapter 5.5.1 (p.174); 6.2.1 (pp.199-202); Chapter 3.3.2 (pp.58-60)

Features of CMOS Circuits

- The output is always connected to V_{DD} or **GND** in steady state
 - Full logic swing; **large noise margins**
 - Logic levels are not dependent upon the relative sizes of the devices ("**ratioless**")
- There is no direct path between V_{DD} and **GND** in steady state
 - **no static power dissipation**

The CMOS Inverter: Current Flow during Switching

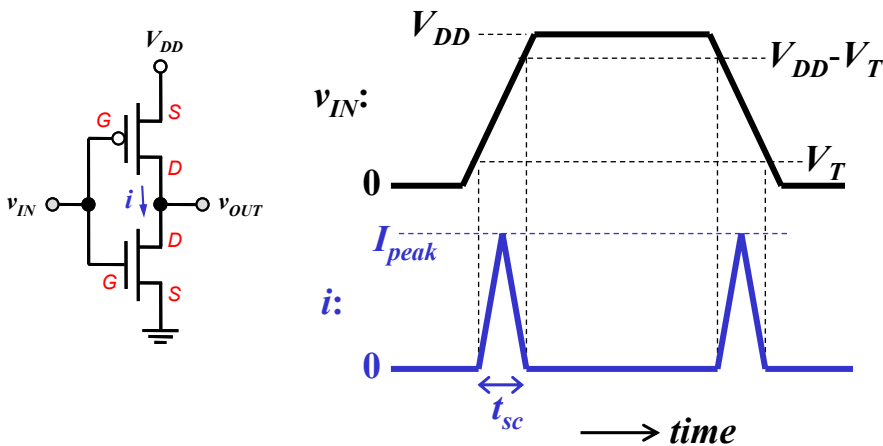


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Power Dissipation due to Direct-Path Current



Energy consumed per switching period: $E_{dp} = t_{sc} V_{DD} I_{peak}$

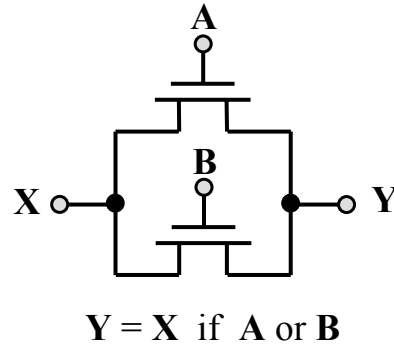
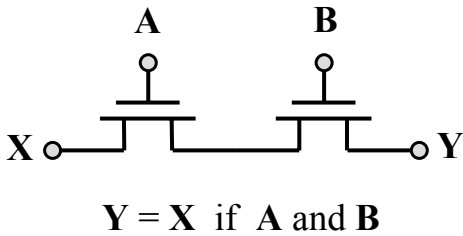
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N-Channel MOSFET Operation

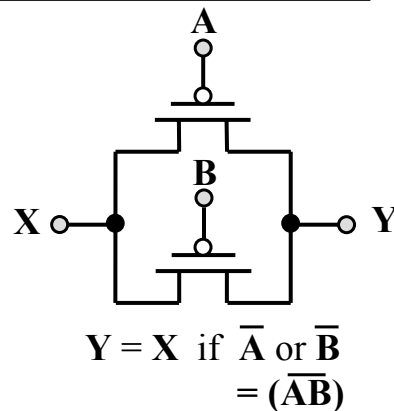
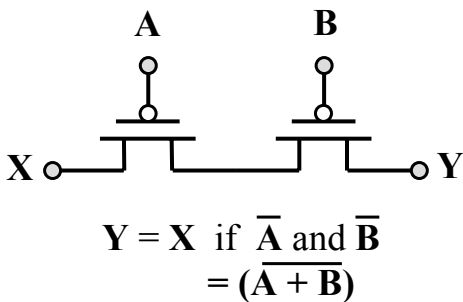
An NMOSFET is a closed switch when the input is high



NMOSFETs pass a “strong” 0 but a “weak” 1

P-Channel MOSFET Operation

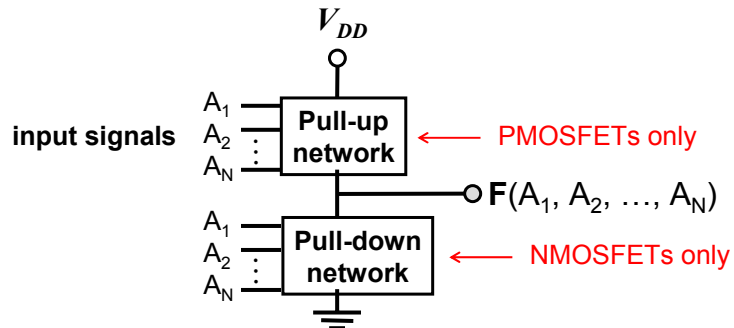
A PMOSFET is a closed switch when the input is low



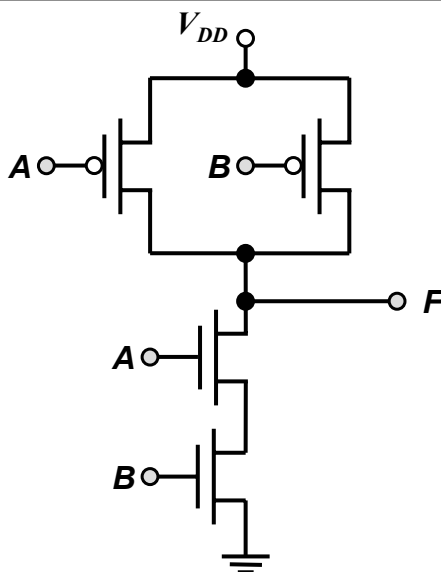
PMOSFETs pass a “strong” 1 but a “weak” 0

Pull-Down and Pull-Up Devices

- In CMOS logic gates, **NMOSFETs** are used to connect the output to **GND**, whereas **PMOSFETs** are used to connect the output to V_{DD} .
 - An NMOSFET functions as a **pull-down device** when it is turned on (gate voltage = V_{DD})
 - A PMOSFET functions as a **pull-up device** when it is turned on (gate voltage = **GND**)

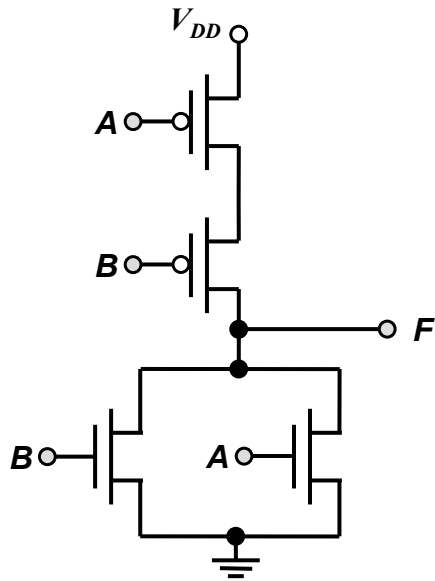


CMOS NAND Gate



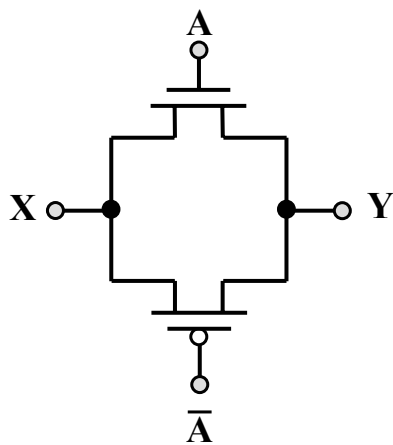
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NOR Gate



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

CMOS Pass Gate



$$Y = X \text{ if } A$$

The “Body Effect”

V_T is a function of V_{SB} :

$$V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

$$\text{where } \phi_F = \frac{kT}{q} \ln \left(\frac{N_B}{n_i} \right)$$

γ is the **body effect coefficient**

When the body-source pn junction is reverse-biased, $|V_T|$ increases. Usually, we want to minimize γ so that I_{Dsat} will be the same for all transistors in a circuit.

Example (0.25 μ m CMOS technology)

