Lecture #32

ANNOUNCEMENTS

- Midterm #2: $\bar{x}$ = 35.8 (71.6%); σ=6.9; hi=47.5; lo=13
- (Midterm#1: $\bar{x}$ = 44.4 (88.8%); σ=7.2; hi=50; lo=10)
- HW#9, Problem 3b: Assume t_p << 1 (negligible on timing diagram)

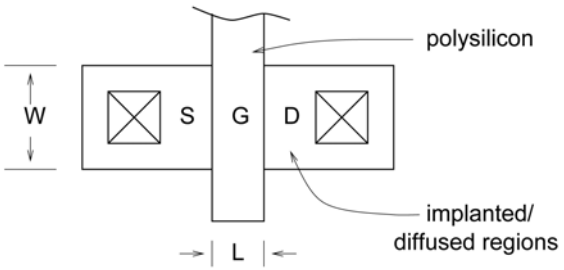
OUTLINE

- Computing the output capacitance
  - Propagation delay examples
- History of IC devices and technology

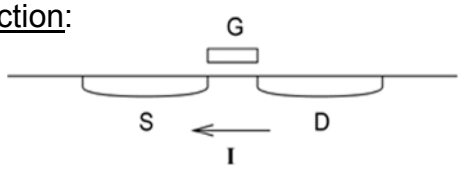
Reading (Rabaey *et al.*)**:** Chapter 5.4, pp. 158-163

MOSFET Layout and Cross-Section

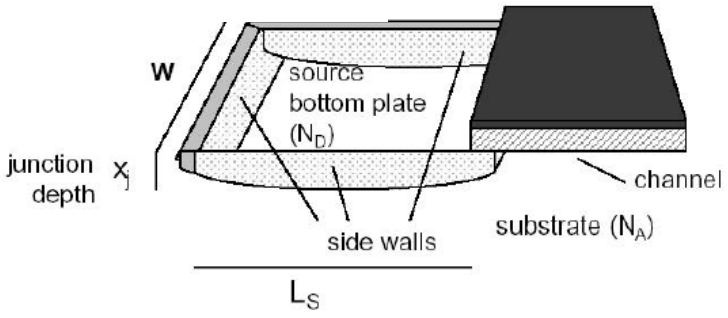
Top View:



Cross Section:



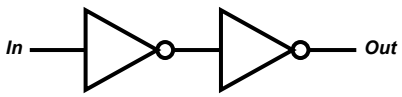
Source and Drain Junction Capacitance

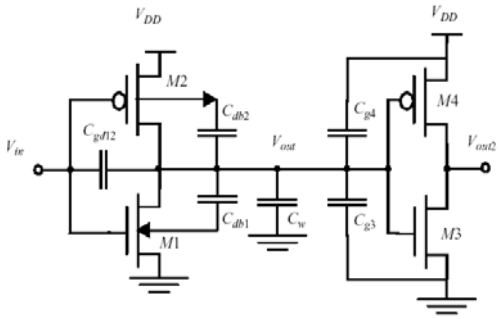


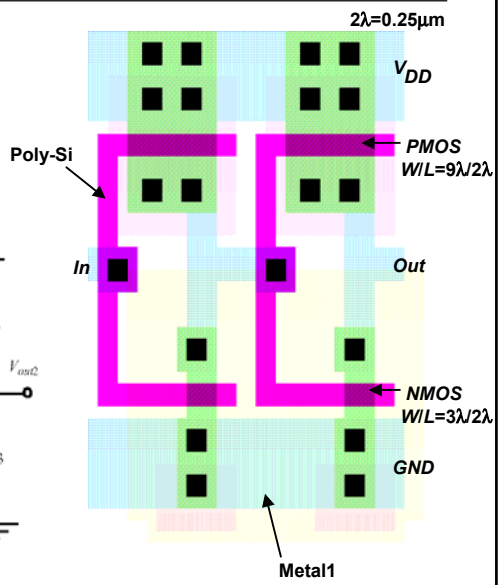
$$C_{source} = C_j \times (\text{AREA}) + C_{jsw} \times (\text{PERIMETER})$$
$$= C_j L_S W + C_{JSW}(2L_S + W)$$

Computing the Output Capacitance

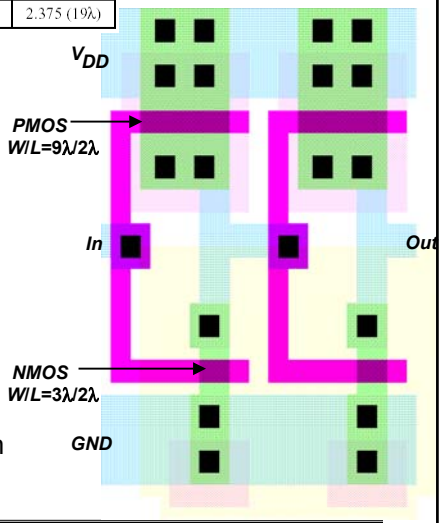
Example 5.4 (pp. 161-163)







	W/L	AD (μm^2)	PD (μm)	AS (μm^2)	PS (μm)
NMOS	0.375/0.25	0.3 (19 λ^2)	1.875 (15λ)	0.3 (19 λ^2)	1.875 (15λ)
PMOS	1.125/0.25	0.7 (45 λ^2)	2.375 (19λ)	0.7 (45 λ^2)	2.375 (19λ)



Capacitances for 0.25μm technology:

Gate capacitances:
- C_{ox}(NMOS) = C_{ox}(PMOS) = 6 fF/μm^2

Overlap capacitances:
- CGDO(NMOS) = C_{on} = 0.31fF/μm
- CGDO(PMOS)= C_{op} = 0.27fF/μm

Bottom junction capacitances:
- CJ(NMOS) = $K_{eqbpn}C_j$ = 2 fF/μm^2
- CJ(PMOS) = $K_{eqbpp}C_j$ = 1.9 fF/μm^2

Sidewall junction capacitances:
- CJSW(NMOS) = $K_{eqswn}C_j$ = 0.28fF/μm
- CJSW(PMOS) = $K_{eqbpp}C_j$ = 0.22fF/μm

C Term	Expression	Value (fF) H→L	Value (fF) L→H
C_{GD1}	$2\,C_{on}W_n$	0.23	0.23
C_{GD2}	$2\,C_{op}W_p$	0.61	0.61
C_{DB1}	$K_{eqbpn}AD_nC_j + K_{eqswn}PD_nC_{jsw}$	0.66	0.90
C_{DB2}	$K_{eqbpp}AD_pC_j + K_{eqswp}PD_pC_{jsw}$	1.5	1.15
C_{G3}	$(2\,C_{on})W_n + C_{ox}W_nL_n$	0.76	0.76
C_{G4}	$(2\,C_{op})W_p + C_{ox}W_pL_p$	2.28	2.28
C_w	from extraction	0.12	0.12
C_L	Σ	6.1	6.0

Examples of Propagation Delay

Product	CMOS technology generation	Clock frequency, *f*	Fan-out=4 inverter delay
Pentium II	0.25 μm	600 MHz	~100 ps
Pentium III	0.18 μm	1.8 GHz	~40 ps
Pentium IV	0.13 μm	3.2 GHz	~20 ps

Typical clock periods:
- high-performance μP: ~15 FO4 delays
- PlayStation 2: 60 FO4 delays

Early History of IC Devices and Technology

- 1940's: Vacuum-tube era
  - Vacuum tubes were used for radios, television, telephone equipment, and computers

  … but they were expensive, bulky, fragile, & energy-hungry

Lee De Forest, 1906

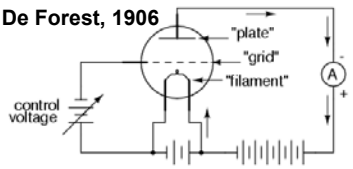
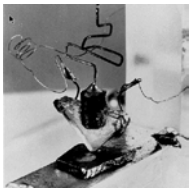


plate current can be controlled by the application of a small control voltage between the grid and filament!

→ Invention of the point-contact transistor
- **Walter Brattain, John Bardeen, and William Shockley, *Bell Labs*, 1947**
  Nobel Prize in Physics 1956

… reproducibility was an issue, however



→ Invention of the bipolar junction transistor
- **William Shockley, *Bell Labs*, 1950**
  - more stable and reliable; easier and cheaper to make

Discrete Electronic Circuits

- In 1954, *Texas Instruments* produced the first commercial silicon transistor.

~$2.50 each

- Before the invention of the integrated circuit, electronic equipment was composed of discrete components such as transistors, resistors, and capacitors. These components, often simply called “discretes”, were manufactured separately and were wired or soldered together onto circuit boards. Discretes took up a lot of room and were expensive and cumbersome to assemble, so engineers began, in the mid-1950s, to search for a simpler approach…

The Integrated Circuit (IC)

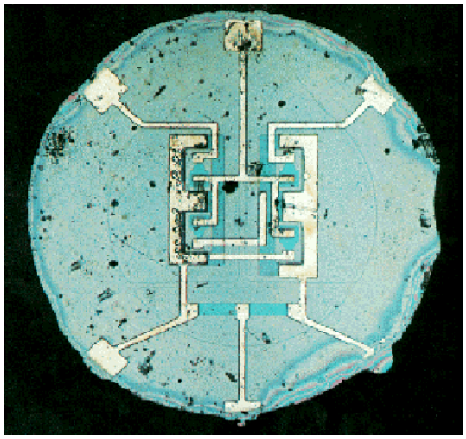
- An IC is built of interconnected electronic components in a single piece (“chip”) of semiconductor material.
- In 1958, Jack S. Kilby (*Texas Instruments*) showed that it was possible to fabricate a simple IC in germanium.

  Nobel prize in Physics 2000
- In 1959, Robert Noyce (*Fairchild Semiconductor*) described how an IC can be made in silicon using silicon dioxide as the insulator and aluminum for the metallic lines. Kilby and Noyce are considered to be co-inventors of the IC.

The first IC was made out of a thin slice of germanium and contains a bipolar transistor, a capacitor, and several resistors. It has four input/output terminals, a ground terminal, and wires of gold. The assemblage is held together with wax.

Kilby's first integrated circuit in germanium.

The First Planar IC



Fairchild Semiconductor, 1959

- ***This chip has four bipolar transistors*** *(the bright blue nose-cone-like features toward the center of the photo)* ***and five resistors*** *(the bright blue horizontal and vertical bars)****. The white bars are aluminum connectors, normally attached to the external world by wires*** *(not shown here)* ***soldered to the pads at the edge of the device.***

Actual size: 0.06 in. diameter

***Fairchild Semiconductor* and *Texas Instruments* both introduced commercial ICs in 1960.**

Field-Effect Transistors

- The field-effect transistor was invented before the bipolar junction transistor
  - J.E. Lilienfeld, U.S. Patent 1,745,175 (1930)
  - O. Heil, British Patent 439,457 (1935)

  … but it was not successfully demonstrated until 1960 by M. Atalla and D. Kahng at *Bell Labs*.
- In 1963, Frank Wanlass (*Fairchild Semiconductor*) introduced CMOS technology. The first CMOS integrated circuits were made by *RCA* in 1968.
- The MOSFET is smaller and simpler to fabricate than a bipolar junction transistor; therefore, more MOSFETs can be formed on a given-size chip. The need for high-density memory (DRAMs) in the 1970's caused MOS to become the dominant IC technology.

IC Manufacturing: Planar Processing

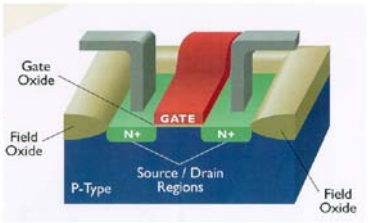
Process steps are sequentially applied to thin slices ("wafers") of silicon in order to fabricate simultaneously and interconnect billions of electronic devices (*e.g.* transistors) on the front surface.

Si wafer

Processing Steps

- oxidation
- anneal
- implantation
- deposition
- lithography
- etch

MOSFET



From a Few, to Billions

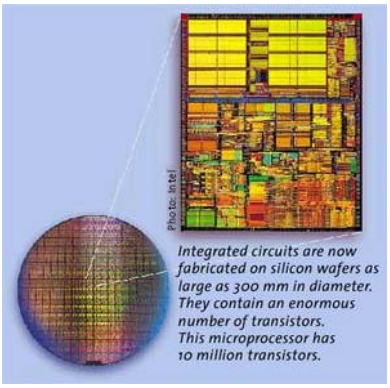
- By connecting a large number of components, each performing simple operations, an IC that performs very complex tasks can be built. The degree of integration has increased at an exponential pace over the past ~40 years.

  Gordon Moore was the first to note this evolution, in 1965.

  - **The number of devices on a chip doubles every 18 months, for the same price.**
    - → **30% reduction in cost/function per yr**
    - → **2X speed improvement every 3 yrs**

    "Moore's Law" still holds today.

  The largest ICs today contain ~10 billion transistors!



Integrated circuits are now fabricated on silicon wafers as large as 300 mm in diameter. They contain an enormous number of transistors. This microprocessor has 10 million transistors.

Modern IC Technology

- Increasing # of levels of wiring (Cu interconnects)
  ~10-level metal entering production

Photo from IBM Microelectronics Gallery:
Colorized scanning-electron micrograph of the copper interconnect layers, after removal of the insulating layers by a chemical etch

- Scaling MOSFETs to smaller dimensions
  - gate lengths below 20 nm have already been demonstrated by AMD, IBM, Intel, Toshiba, *etc.*

  → most advanced transistor designs are based on UC-Berkeley research (Prof.s Hu, King, Bokor)
- Approaching technology/economic limits (?)

EECS40: The Home Stretch

To complete this course, we will learn

- How are integrated circuits made?
  - → Overview of microfabrication technology
  - → CMOS fabrication process
- Where is the output capacitance which limits performance?
  - → CMOS layout and circuit extraction
  - → Interconnect modeling
- What are the future issues for IC devices and technology, and circuit design?
  - → State-of-the-art technology