Lecture #35

OUTLINE

• Device isolation methods
• Electrical contacts to Si
• Mask layout conventions
• Process flow examples
  – Resistor
  – N-channel MOSFET

Device Isolation Methods

(1) pn-junction isolation:

**Cross-Sectional View:**

device area 1  device area 2

\[ p \]  \[ p \]  \[ p \]

\[ n \]

\[ n \]

**Top View:**

\[ p \]  \[ p \]  

\[ p \]  \[ p \]

• The substrate is biased to ensure that the pn junctions are never forward biased
(2) Oxide isolation:

\[
\begin{array}{c}
\text{SiO}_2 \\
\text{SiO}_2 \\
n \\
\text{SiO}_2 \\
\text{SiO}_2 \\
p \\
p \\
\end{array}
\]

(3) Silicon-on-Insulator substrate:

\[
\begin{array}{c}
\text{Si} \\
\text{Si} \\
dielectric substrate (e.g. SiO}_2, \text{Al}_2\text{O}_3)
\end{array}
\]

Electrical Contacts to Si

- In order to achieve a low-resistance ("ohmic") contact between metal and silicon, the silicon must be heavily doped:

  \[
  \begin{array}{c}
  \text{Metal contact to n-type Si} \\
  \text{Metal contact to p-type Si}
  \end{array}
  \]

\[
\begin{array}{c}
\text{SiO}_2 \\
\text{SiO}_2 \\
\text{SiO}_2 \\
\text{SiO}_2 \\
\text{SiO}_2 \\
n^+ \\
p^+
\end{array}
\]

\[
\begin{array}{c}
\text{Al} \\
\text{Al}
\end{array}
\]

\[
\begin{array}{c}
N_d \geq 10^{20} \text{ cm}^{-3} \\
N_A \geq 10^{19} \text{ cm}^{-3}
\end{array}
\]

→ To contact the body of a MOSFET, locally heavy doping is used.
Mask Layout

- Typically, multiple lithography steps are needed in order to fabricate an integrated circuit.
  - Each lithography step utilizes a mask with the desired pattern for a specific layer.
- Computer-aided design (CAD) tools are used to generate the masks
  - The desired pattern for each layer is drawn, and can be overlaid with the patterns for other layers, to make sure that they are properly aligned to each other.

**Layout Example:**
MOSFET gate pattern aligned to “active area” pattern

**Process layers:**
- “Active” area
- Gate (poly-Si)

What if the physical mask looks like this?

Most of the area of the exposure field is dark

“dark-field” mask

Layout is all color, with the exception of a few holes

→ very inconvenient to draw and to display
Dark-Field / Light-Field Convention

A dark-field mask blocks our view of underlying layers

...but if we draw the “negative” (or “complement”) of masks that are dark-field, the CAD layout is much easier, and the overlaid layers are easier to visualize

Rather than this:

Draw only the “holes” on the layout, i.e. the clear areas

To indicate that the CAD layout is the negative of the mask, label it “dark field”. “Clear field” indicates a “positive” mask.

Process Flow Example #1: Resistor

Three-mask process:

Starting material: p-type wafer with \( N_A = 10^{16} \text{ cm}^{-3} \)

Step 1: grow 500 nm of SiO\(_2\)

Step 2: pattern oxide using the oxide mask (dark field)

Step 3: implant phosphorus and anneal to form an n-type layer with \( N_D = 10^{20} \text{ cm}^{-3} \) and depth 100 nm

Step 4: deposit oxide to a thickness of 500 nm

Step 5: pattern deposited oxide using the contact mask (dark field)

Step 6: deposit aluminum to a thickness of 1 \( \mu \text{m} \)

Step 7: pattern using the aluminum mask (clear field)

Layout:

- Oxide mask (dark field)
- Contact mask (dark field)
- Al mask (clear field)
Step 2: Pattern oxide

Step 3: Implant & Anneal

Step 4: Deposit 500 nm oxide

Step 5: Pattern oxide

Step 7: Pattern metal
Importance of Layer-to-Layer Alignment

Example: metal line to contact hole

→ marginal contact

→ no contact!

→ safety margin to allow for misalignment

Example of Design Rule:
If the minimum feature size is $2\lambda$, then the safety margin for overlay error is $\lambda$.

Design Rules are needed:
- Interface between designer and process engineer
- Guidelines for designing masks

N-channel MOSFET

Schematic Cross-Sectional View

Layout (Top View)

4 lithography steps are required:
1. active area
2. gate electrode
3. contacts
4. metal interconnects
Process Flow Example #2: nMOSFET

1) Thermal oxidation (~10 nm “pad oxide”)  

2) Silicon-nitride ($\text{Si}_3\text{N}_4$) deposition by CVD (~40nm)  

3) Active-area definition (lithography & etch)  

4) Boron ion implantation (“channel stop” implant)  

5) Thermal oxidation to grow oxide in “field regions”  

6) $\text{Si}_3\text{N}_4$ & pad oxide removal  

7) Thermal oxidation (“gate oxide”)  

8) Poly-Si deposition by CVD  

9) Poly-Si gate-electrode patterning (litho. & etch)  

10) P or As ion implantation to form $n^+$ source and drain regions
11) SiO₂ CVD
12) Contact definition (litho. & etch)
13) Al deposition by sputtering
14) Al patterning by litho. & etch to form interconnects

Visualizing Layouts and Cross-Sections with SIMPLer

SIMPL is a CAD tool created by Prof. Neureuther’s group
- allows IC designers to visualize device cross-sections corresponding to a fabrication process and physical layout.

A Berkeley undergraduate student, Harlan Hile, created a mini-version of SIMPL (called SIMPLer) for EECS40.
- It’s a JAVA program -> can be run on any computer, as well as on a web server.
- You can access it directly at
  http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.html