Lecture #36

ANNOUNCEMENT

- Students in the Thursday 5-8PM lab session should contact the TA, to arrange to take Quiz #2

OUTLINE

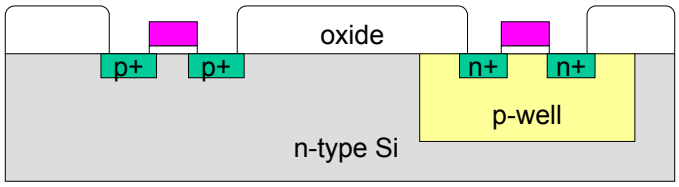
- CMOS process flow
- Circuit extraction from layout

CMOS Technology

Challenge: Build both NMOS & PMOS transistors on a single silicon chip

- **NMOSFETs need a p-type substrate**
- **PMOSFETs need an n-type substrate**

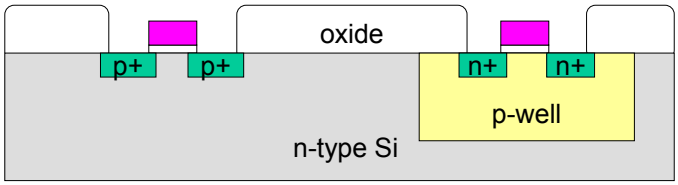
→ Requires extra process steps!



Conceptual CMOS Process Flow

n-type wafer

*Create "p-well"



Grow thick oxide

*Remove thick oxide in transistor areas ("active region")

Grow gate oxide

Deposit & *pattern poly-Si gate electrodes

*Dope n channel source and drains (need to protect PMOS areas)

*Dope p-channel source and drains (need to protect NMOS areas)

Deposit insulating layer (oxide)

*Open contact holes

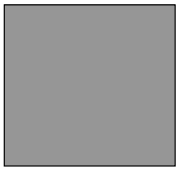
→ At least 3 more masks, as compared to NMOS process

Deposit and *pattern metal interconnects

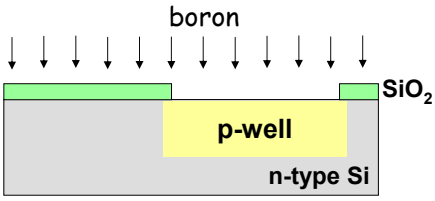
Additional Process Steps Required for CMOS

1. Well Formation

Top view of p-well mask
(dark field)



Cross-sectional view of wafer



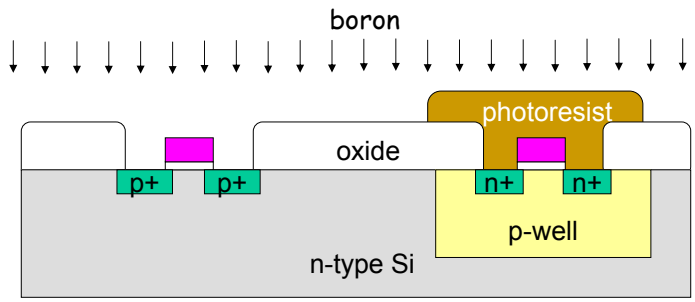
- **Before transistor fabrication, we must perform the following process steps:**
  1. grow oxide layer; pattern oxide using p-well mask
  2. implant phosphorus; anneal to form deep p-type regions

2. Masking the Source/Drain Implants

"Select p-channel" ⟶ We must protect the n-channel devices during the boron implantation step, and

"Select n-channel" ⟶ We must protect the p-channel devices during the arsenic implantation step

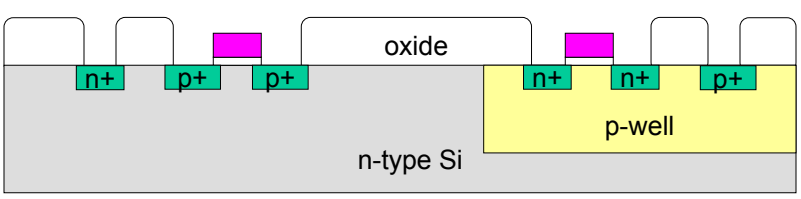
Example: Select p-channel



Forming Body Contacts

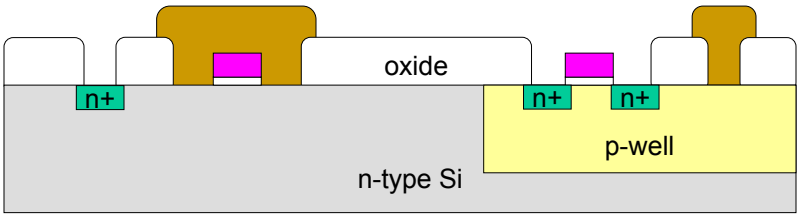
Modify oxide mask and "select" masks:

1. Open holes in original oxide layer, for body contacts
2. Include openings in select masks, to dope these regions

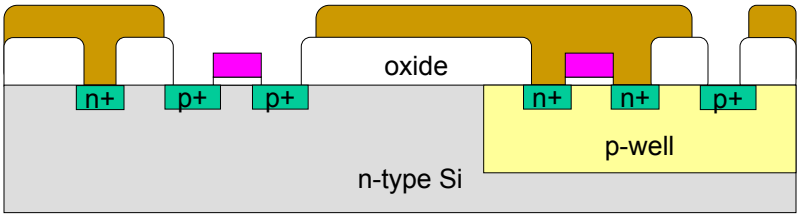


Select Masks

N-select:



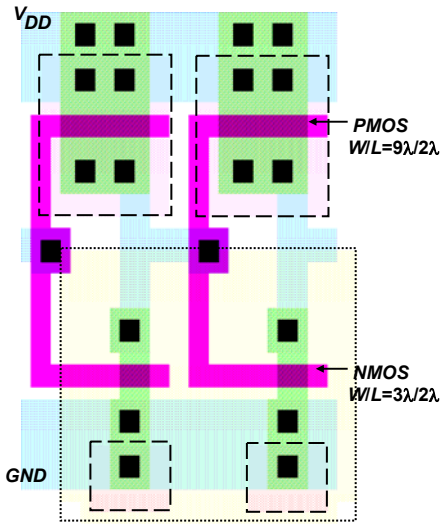
P-select:



CMOS Inverter Layout

Note body contacts:

- p-well to GND
- n-substrate to V_{DD}



P-well mask (dark field)

Active (clear field)

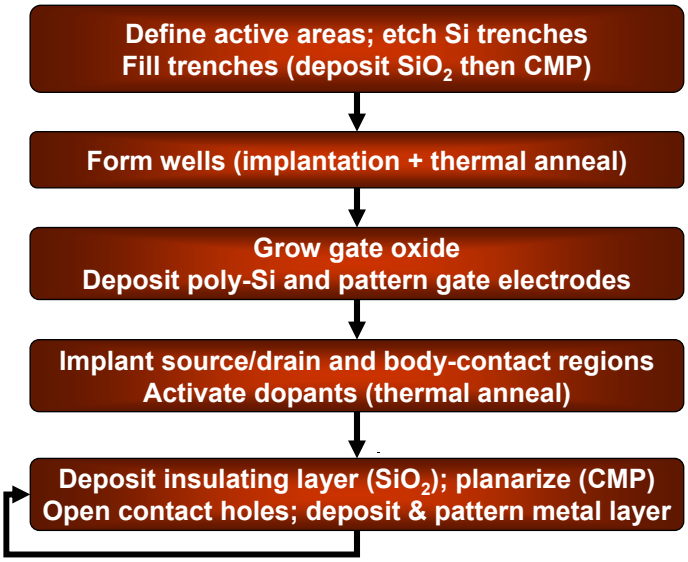
Gate (clear field)

Select mask (dark field & clear field)

Contact (dark field)

Metal (clear field)

Modern CMOS Process at a Glance



Circuit Extraction from Layouts

Procedure:

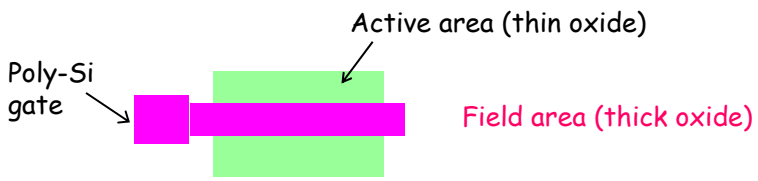
1) Inspect layout and identify obvious devices:
   - NMOSFETs
   - PMOSFETs
   - wires (metal or poly-Si)

2) Identify other (often undesired) circuit components:
   - resistances (*e.g.* associated with long wires)
   - capacitances

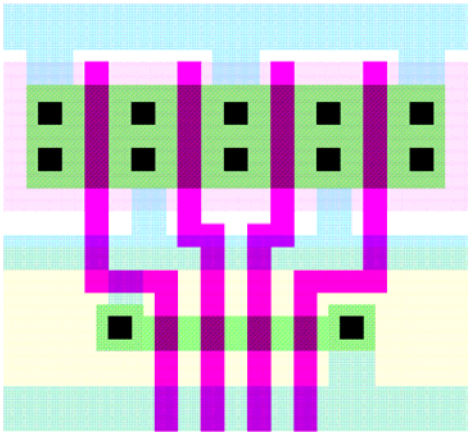
3) Draw schematic (V_{DD} at top, GND at bottom)

Identifying a MOSFET

Poly-Si line crossing over an "active" region → **MOSFET!**



If the active area is located within p-well region → **NMOS**

If the active area is NOT located in p-well region → **PMOS**

Example: Circuit Extraction from Layout