ANNOUNCEMENTS

• Prof. King’s Office Hour on Wed 11/26 changed to 3-4PM
• In order to receive extra credit for your Tutebot project, you must endow it with added functionality.
  Examples: reaction to light, heat, sound; edge avoidance; capability to “learn” where objects are (memory)
  Simply adding LEDs is not sufficient to earn extra credit!

OUTLINE

» Interconnect parameters
» Interconnect modeling

Reading (Rabaey et al.)
Chapter 4: pp. 104-127
Chapter 5: pp. 172-173

Interconnects

• An interconnect is a thin-film wire that electrically connects 2 or more components in an integrated circuit.

• Interconnects can introduce parasitic (unwanted) components of capacitance, resistance, and inductance. These “parasitics” detrimentally affect
  – performance (e.g. propagation delay)
  – power consumption
  – reliability

• As transistors are scaled down in size and the number of metal wiring layers increases, the impact of interconnect parasitics increases.
  → Need to model interconnects, to evaluate their impact
Interconnect Resistance & Capacitance

Metal lines run over thick oxide covering the substrate → contribute RESISTANCE & CAPACITANCE to the output node of the driving logic gate.

Wire Resistance

\[ R_{\text{wire}} = \frac{\rho L}{H W} = R_s \frac{L}{W} \]

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet Res. ((\Omega/mm))</th>
</tr>
</thead>
<tbody>
<tr>
<td>n, p well diffusion</td>
<td>1000 to 1500</td>
</tr>
<tr>
<td>n+, p+ diffusion</td>
<td>50 to 150</td>
</tr>
<tr>
<td>n+, p+ diffusion   with silicidal</td>
<td>3 to 5</td>
</tr>
<tr>
<td>polysilicon</td>
<td>150 to 200</td>
</tr>
<tr>
<td>polysilicon with silicidal</td>
<td>4 to 5</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 to 0.1</td>
</tr>
<tr>
<td>Tungsten (W)</td>
<td>5.5 \times 10^{-8}</td>
</tr>
<tr>
<td>Copper (Cu)</td>
<td>1.7 \times 10^{-8}</td>
</tr>
<tr>
<td>Gold (Au)</td>
<td>2.2 \times 10^{-8}</td>
</tr>
<tr>
<td>Silver (Ag)</td>
<td>1.6 \times 10^{-8}</td>
</tr>
</tbody>
</table>
Typical values of $R_n$ and $R_p$ are $\sim 10 \, k\Omega$, for $W/L = 1$

... but $R_n$, $R_p$ are much lower for large transistors (used to drive long interconnects with reasonable $t_p$)

Compare with the resistance of a 0.5$\mu$m-thick Al wire:

$R = \rho / H = (2.7 \, \mu\Omega\cdot\text{cm}) / (0.5 \, \mu\text{m}) = 5.4 \times 10^{-2} \, \Omega$

**Example**: $L = 1000 \, \mu\text{m}$, $W = 1 \, \mu\text{m}$

$R_{\text{wire}} = R \cdot (L / W)$

$= (5.4 \times 10^{-2} \, \Omega / (1000/1)) = 54 \, \Omega$

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**Wire Capacitance: The Parallel Plate Model**

**Relative Permittivities**

<table>
<thead>
<tr>
<th>Material</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free space</td>
<td>1</td>
</tr>
<tr>
<td>Aerogels</td>
<td>1.5</td>
</tr>
<tr>
<td>Polymers (organic)</td>
<td>3-4</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>3.9</td>
</tr>
<tr>
<td>Glass-epoxy (PC board)</td>
<td>5</td>
</tr>
<tr>
<td>Silicon Nitride Si$_3$N$_4$</td>
<td>7.5</td>
</tr>
<tr>
<td>Alumina (package)</td>
<td>9.3</td>
</tr>
<tr>
<td>Silicon</td>
<td>11.7</td>
</tr>
</tbody>
</table>

$C_{\text{pp}} = \frac{\varepsilon_{\text{di}} \cdot W \cdot L}{t_{\text{di}}}$
Parallel-Plate Capacitance Example

- Oxide layer is typically ~500 nm thick
- Interconnect wire width is typically ~0.5 µm wide (1st level)
  ⇒ capacitance per unit length = 345 fF/cm = 34.5 aF/µm

Example: \( L = 30 \) µm
  ⇒ \( C_{pp} \approx 1 \) fF (compare with \( C_n \sim 2 \) fF)

Fringing-Field Capacitance

Wire capacitance per unit length:

\[
C_{wire} \approx C_{pp} + C_{fringe} = \frac{W \varepsilon_{di}}{t_{di}} + \frac{2\pi \varepsilon_{di}}{\log\left(t_{di} / H\right)}
\]

For \( W / t_{di} < 1.5 \), \( C_{fringe} \) is dominant
Modeling an Interconnect

Problem: Wire resistance and capacitance to underlying substrate is spread along the length of the wire

"Distributed RC line"

We will start with a simple model...

Lumped RC Model

Model the wire as single capacitor and single resistor:

- $C_{wire}$ is placed at the end of the interconnect → adds to the gate capacitance of the load
- $R_{wire}$ is placed at the logic-gate output node → adds to the MOSFET equivalent resistance
Cascaded CMOS Inverters w/ Interconnect

Using “lumped RC” model for interconnect:

\[ \tau_D = R_{dr} C_{intrinsic} + (R_{dr} + R_{wire})(C_{wire} + C_{fanout}) \]

\[ = R_{dr} C_{intrinsic} + (R_{dr} + R_{wire})C_{fanout} + (R_{dr} + R_{wire})C_{wire} \]

Effect of Interconnect Scaling

\[ R_{wire} C_{wire} = \left[ \frac{\rho L}{WH} \varepsilon_{di} (WL) + \frac{2\pi \varepsilon_{di} L}{\log(t_{di} / H)} \right] \propto \rho \varepsilon_{di} L^2 \]

- Interconnect delay scales as square of \( L \)
  \[ \Rightarrow \text{minimize interconnect length!} \]

- If \( W \) is large, then it does not appear in \( R_{wire} C_{wire} \)
  - Capacitance due to fringing fields becomes more significant as \( W \) is reduced; \( C_{wire} \) doesn’t actually scale with \( W \) for small \( W \)