Lecture #37

ANNOUNCEMENTS

- Prof. King's Office Hour on Wed 11/26 changed to 3-4PM
- In order to receive extra credit for your Tutebot project, you must endow it with added functionality.

  Examples: reaction to light, heat, sound; edge avoidance;
  capability to "learn" where objects are (memory)

  Simply adding LEDs is not sufficient to earn extra credit!

OUTLINE

» Interconnect parameters
» Interconnect modeling

Reading (Rabaey *et al*.)
Chapter 4: pp. 104-127
Chapter 5: pp. 172-173

Interconnects

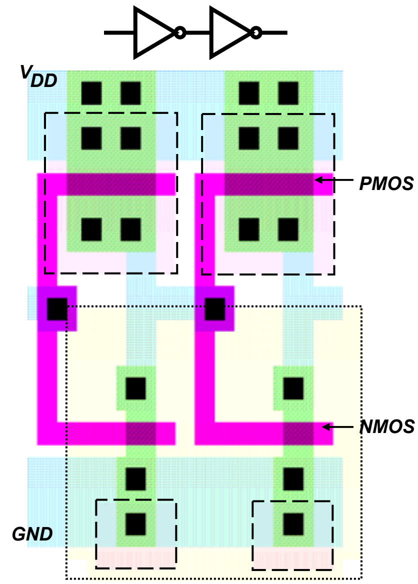
- An ***interconnect*** is a thin-film wire that electrically connects 2 or more components in an integrated circuit.
- Interconnects can introduce parasitic (unwanted) components of capacitance, resistance, and inductance. These ***"parasitics"*** detrimentally affect
  - performance (*e.g.* propagation delay)
  - power consumption
  - reliability
- As transistors are scaled down in size and the number of metal wiring layers increases, the impact of interconnect parasitics increases.

  → Need to model interconnects, to evaluate their impact

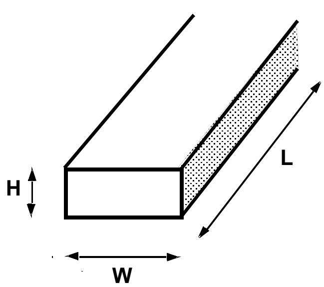
Interconnect Resistance & Capacitance

Metal lines run over thick oxide covering the substrate

→ **contribute RESISTANCE & CAPACITANCE to the output node of the driving logic gate**



Wire Resistance



$$R_{wire} = \frac{\rho L}{H\,W} = R_s \frac{L}{W}$$

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Material	Sheet Res. (Ω/❐)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

Interconnect Resistance Example

Typical values of R_n and R_p are **~10 kΩ**, for W/L = 1

… but R_n, R_p are much lower for large transistors (used to drive long interconnects with reasonable t_p)

Compare with the resistance of a 0.5μm-thick Al wire:

$R_\square = \rho / H = (2.7\ \mu\Omega\text{-cm}) / (0.5\ \mu m) = 5.4 \times 10^{-2}\ \Omega / \square$

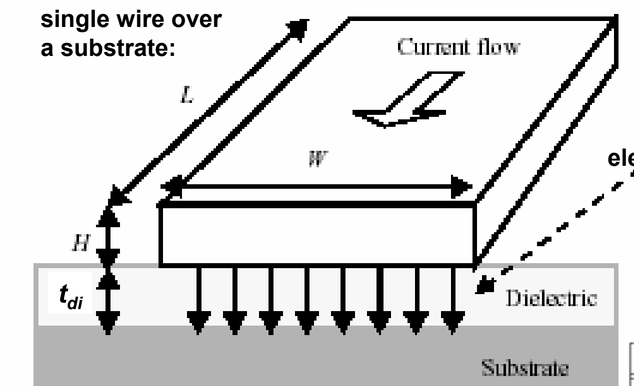
Example: $L = 1000\ \mu m$, $W = 1\ \mu m$

$\rightarrow R_{wire} = R_\square (L / W)$

$= (5.4 \times 10^{-2}\ \Omega / \square)(1000/1) = \mathbf{54\ \Omega}$

Wire Capacitance: The Parallel Plate Model

single wire over a substrate:



$$C_{pp} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Relative Permittivities

Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Parallel-Plate Capacitance Example

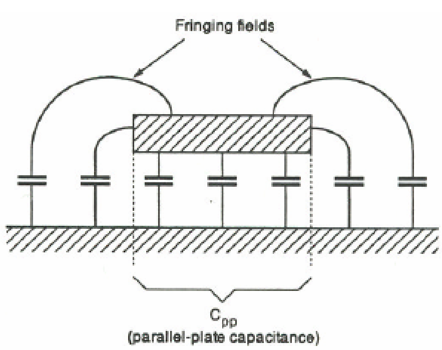
- Oxide layer is typically ~500 nm thick
- Interconnect wire width is typically ~0.5 μm wide (1st level)

  ⇒ capacitance per unit length = 345 fF/cm = 34.5 aF/μm

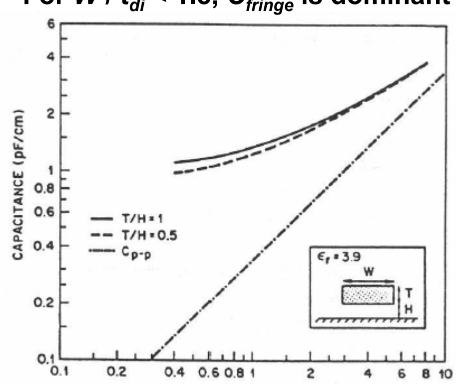
Example: L = 30 μm

→ $C_{pp} \cong 1$ fF (compare with C_n~ 2 fF)

Fringing-Field Capacitance



For W / t_{di} < 1.5, C_{fringe} is dominant



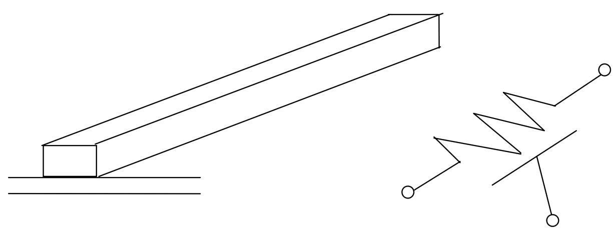
Wire capacitance per unit length:

$$c_{wire} \cong c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)} \qquad w = W - \frac{H}{2}$$

Modeling an Interconnect

Problem: Wire resistance and capacitance to underlying substrate is spread along the length of the wire

"Distributed RC line"

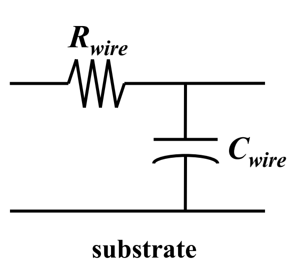


We will start with a simple model…

Lumped RC Model

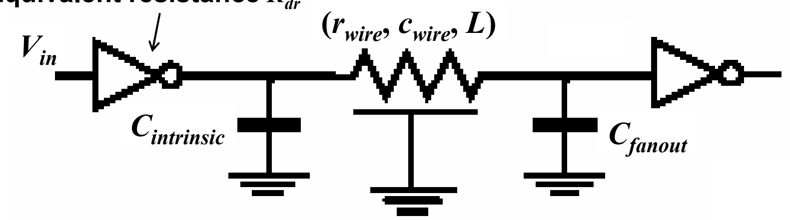
Model the wire as single capacitor and single resistor:

- C_{wire} is placed at the end of the interconnect
  → adds to the gate capacitance of the load
- R_{wire} is placed at the logic-gate output node
  → adds to the MOSFET equivalent resistance

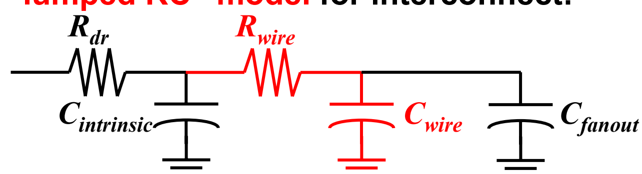


Cascaded CMOS Inverters w/ Interconnect

Equivalent resistance R_{dr}



Using "lumped RC" model for interconnect:



$$\tau_D = R_{dr}C_{intrinsic} + (R_{dr} + R_{wire})\left(C_{wire} + C_{fanout}\right)$$

$$= R_{dr}C_{intrinsic} + (R_{dr} + R_{wire})C_{fanout} + (R_{dr} + R_{wire})C_{wire}$$

Effect of Interconnect Scaling

$$R_{wire}C_{wire} = \left[\rho\frac{L}{WH}\right]\left[\frac{\varepsilon_{di}}{t_{di}}(WL) + \frac{2\pi\varepsilon_{di}L}{\log(t_{di}/H)}\right] \propto \rho\varepsilon_{di}L^2$$

- Interconnect delay scales as <u>square</u> of *L*

  $\Rightarrow$ minimize interconnect length!

- If *W* is large, then it does not appear in $R_{wire}C_{wire}$
  - Capacitance due to fringing fields becomes more significant as *W* is reduced; C_{wire} doesn't actually scale with *W* for small W