Problem 1

a) For gate 1, \( F = (A \cdot B) + C \), for gate 2 \( F = (A + B) \cdot (C + D) \)

b) For gate 1, minimum propagation delay for a high \( \rightarrow \) low transition is 2/3 delays.
   The maximum propagation delay for a high \( \rightarrow \) low transition is 2 delays.
   For gate 2, minimum propagation delay for a high \( \rightarrow \) low transition is 1 delay.
   The maximum propagation delay for a high \( \rightarrow \) low transition is 2 delays.

c) For gate 1, minimum propagation delay for a low \( \rightarrow \) high transition is 3/2 delays.
   The maximum propagation delay for a low \( \rightarrow \) high transition is 2 delays.
   For gate 2, minimum propagation delay for a low \( \rightarrow \) high transition is 1 delay.
   The maximum propagation delay for a low \( \rightarrow \) high transition is 2 delays.

d) For a minimum high to low transition for gate 1, the following initial inputs work:
   \( A = B = C = 0, A = C = 0 \) & \( B = 1, B = C = 0 \) & \( A = 1 \)
   For changes in inputs, \( A = B = C = 1 \)
   For a minimum high to low transition for gate 2, the following initial inputs work:
   \( A = B = C = D = 0, A = B = 0 \) & \( C \) & \( D \) anything, \( C = D = 0 \) & \( A \) & \( B \) anything
   For changes in inputs, \( A = B = C = D = 1 \)
   For a minimum low to high transition for gate 1, the following initial inputs work:
   \( A = B = C = 1, C = 1 \) & \( A \) & \( B \) anything, \( A = B = 1 \) & \( C \) anything
   For changes in inputs, \( A = B = C = 0 \)
   For a minimum low to high transition for gate 2, the following initial inputs work:
   \( A = B = C = D = 1, A = C = 1 \) & \( B \) & \( D \) anything, \( A = D = 1 \) & \( B \) & \( C \) anything,
   \( B = C = 1 \) & \( A \) & \( D \) anything, \( B = D = 1 \) & \( A \) & \( C \) anything
   For changes in inputs, \( A = B = C = D = 0 \)

e) For a maximum high to low transition for gate 1, the same initial inputs work.
   For changes in inputs, \( A = B = 1 \) & \( C = 0 \)
   For a maximum high to low transition for gate 2, the same initial inputs work.
   For changes in inputs, \( A = C = 1 \) & \( B = D = 0, A = C = 0 \) & \( B = D = 1 \)
   For a maximum low to high transition for gate 1, the same initial inputs work.
   For changes in inputs, \( B = C = 0 \) & \( A = 1, A = C = 0 \) & \( B = 1 \)
   For a maximum low to high transition for gate 2, the same initial inputs work.
   For changes in inputs, \( A = B = 0 \) & \( (C = 1 \) or \( D = 1), C = D = 0 \) & \( (A = 1 \) or \( B = 1) \)

Problem 2

a) For either a low edge or a high clock edge, only one half of the latch is active at a
time. The longest delay is then given by the longest delay through any one side of
the latch, which is 2 inverter delays.

b) The timing diagrams are given below, the first set being for lumped logic and
pipelined logic. The latch interior values were not required but are included for
your own benefit.