EECS 40, Fall 2007
Prof. Chang-Hasnain

Homework #8

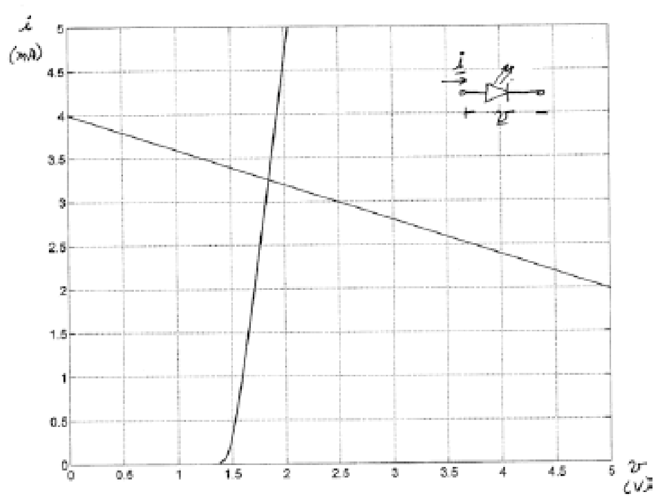
Due at 5 pm in 240 Cory on Thursday, 11/15/07
Total Points: 100

- Put (1) your name and (2) discussion section number on your homework.
- You need to put down all the derivation steps to obtain full credits of the problems. Numerical answers alone will at best receive low percentage partial credits.
- No late submission will be accepted except those with prior approval from Prof. Chang-Hasnain.
- Problems of this HW are from Hambley 4th Edition

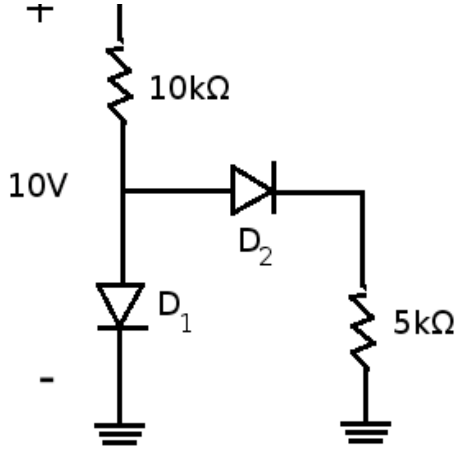
Large Signal Modeling of Diodes

1. (Load Line Analysis) P10.24 (10 points)

P10.24 If we remove the diode, the Thévenin equivalent for the remaining circuit consists of a 10-V source in series with a 2.5-kΩ resistance. The load line is



At the intersection of the characteristic and the load line, we have $v \cong 1.85$ V and $i \cong 3.25$ mA.



2. (DC Models Diode) (12 points)

For the circuit on the left, calculate the currents and voltages of each diode

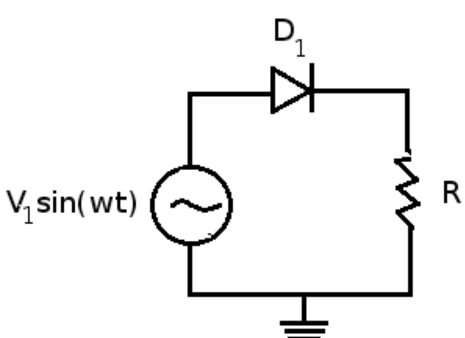
(a) assuming ideal diodes. (6 pts)

(b) assuming the constant voltage drop model (0.6 V) (6pts)

a) Guess D1 on, D2 on. Then i1 = 10V/10k□ = 1mA, and i2 = 0A. The voltage across D1 and D2 is 0V for each. Positive currents and 0V drop is consistent with the ideal diode model. (Could also say D2 is off, but with the same voltage).

b) Guess both diodes to be on. Then V1 = .6, and V2 = .6. So voltage drop across the 10k□resistor must be 9.4V. Therefore i_{tot} = 9.4 / 10k□= 0.94mA. The voltage drop across the 5k□must be 0 so i2 = 0A, and i1 = i_{tot} = 0.94mA. This is consistent with the constant voltage drop model.

3. (Rectifier Circuits)

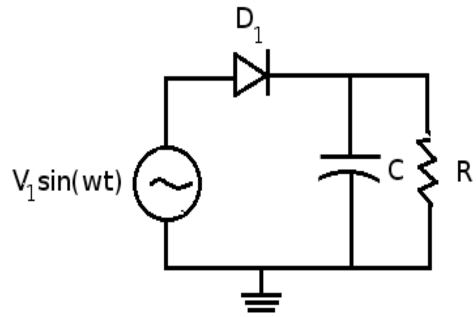


You have a device which requires DC voltage. However, you only have an AC voltage source. You try to design a rectifier circuit. In this question, you may assume the diode to be ideal (27 pts total)

(a) Your first approach is the circuit on the left. sketch the voltage at the diode and at the resistor as a function of time. There are two problems associated with this circuit. Which are those?

One problem is that the voltage is zero for large periods of time (corresponding to the negative half of the wave). Another is that it has a large AC component (ie ripple). See figure 10.24 on page 486.

(b) To improve on these problems, you come up with the following circuit. Sketch the voltage drop at the resistor qualitatively, assuming a large capacitance (you do not need the actual values to do that).



See figure 10.26 on page 487. (You can replace the linear decay with an exponential decay, if you like).

(c) Still considering the circuit on the right, assume now R=1kΩ, C=100uF, and f=60Hz. Calculate the approximate lowest value of the voltage drop at the resistor as a function of V_1, and briefly comment on why your approximation holds.

Vmin = Vm – Vr (fig 10.26) where Vm is the maximal voltage (V1) and Vr is the peak-to-peak ripple voltage defined on page 488. $V_r \approx i_L T/C$. $i_L \approx (V1-V_r/2)/R$ so $V_r*C/T = V_1/R - V_r/(2R)$ □ Vr=(V1/R)/(C/T+1/2R). Plugging in values we get Vr = 0.1538 V1 and Vmin = V1 – Vr = .846V1.
Alternatively we could further approximate by noting 1/2R << C/T and neglect the 1/2R term (this is equivalent to using iL = V1/R rather than $(V1-V_r/2)/R$), giving Vr ≈ V1(T/RC). Then plugging in would yield V_r = .17, and Vmin = V1-Vr ≈ .83 V1.
Either approximation is fine.
Note that we should check that our approximation that the capacitance is large holds. The requirement that RC >> T is met, so the linear approximation for decay is reasonable.

(d) Assume now you want to assure that the voltage drop across the resistor is never lower than 0.9V1. What value for C do you need to choose if R and f are fixed?

Peak-to-peak ripple voltage V_R should be .1V1. i_L will be (Vin – V_R/2) /R = Vin(.95)/(1kΩ) = 9.5*10^-4 Vin , and T = 1/60 s. Therefore using C =i_L T/V_R, we get 9.5*10^-3 /60 F = 158uF.

If we used the same approximation as in the second part of (a) then we'd have required T/RC <= .1 so using T = 1/60 s and R=1kΩ, find C >= 10T/R = .17*10^-3F = 1.7*10^4F = 170uF.

Either of these is fine.

(e) You now use a diode-bridge full-wave rectifier. Draw the configuration with the smoothing capacitor and the load resistor at the output.

The figure should look like that on page 490, except with a large capacitor in parallel with the load resistor.

(f) Repeat problem (d) with the configuration found in (e).

Now the capacitor discharges for only half a cycle, so we need $C=i_L T / (2 V_R)$. Again we replace i_L with V_m/R and now $V_R = .1$ Vin. So C = 79mF or 85uF, depending on what you got in (d).

4. (Clipper Circuits) (14 pts)

You have a sinusoidal input voltage adhering to 5V sin(□ t).

(a) Design a clipper circuit using diodes (assume the constant voltage drop model with 0.6V) and Zener diodes (ideal) that clips voltages above 4V, and also clips the signal during half of the time window during which the input is negative. (8 pts)

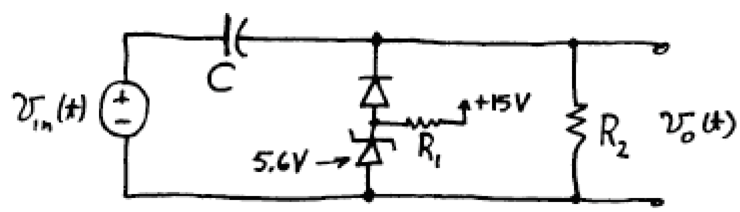
Before we begin, we must simplify the second condition. The input has period 2□/ □. The segments of time during which the input are negative are from [-□/□,0] mod 2□/□. The easiest way to clip half this time period is to clip the values that occur between [-3□/4□, -□/4□]. These correspond to a voltage of less than -5/(√2)V.
Therefore we wish to clip voltages above 4 volts and below -3.54 volts. We do this with a circuit like that in Figure 10.30 on page 492, except that our Zener diodes have break-down voltages 3.4V and 2.94V (from left to right).

(b) Explain the functionality of the designed circuit. Discuss voltage drops and currents of the diodes in the different phases of operation. (6 pts)

The circuit clips outputs above 4volts and below -3.54V. When voltage is above 4V then the left Zener diode breaks down and current flows across, causing a drop of 4 V (.6 on the left ideal diode and 3.4 on the left Zener diode). When voltage is below 4V but above -3.54 then no current flows across either branch, and the diodes both serve as open circuits. When the voltage is below -3.54 then the right Zener diode breaks down and current flows through the right branch, with a drop of -.6 on the right ideal diode and -2.94 on the Zener diode, or a total drop of 3.54.

5. (Clamp Circuits) P10.76

P10.76 A suitable circuit is:



We must choose R_1 to ensure that the 5.6-V Zener is in the breakdown region at all times and choose the time constant $R_2C >> T$, where T is the period of the input waveform.

The idea behind this solution is as follows: you need a 5.6 V battery (everyone should be able to get that far. How do we make such a batter using a Zener diode? Send current through it in the wrong direction. Then you have a 5.6V battery. We just put this in the circuit. The picture above needs a slight modification—the other terminal of the Zener diode should be grounded.

Small Signal Modeling of Diodes

6. P10.78 (5pts)

P10.78 The small signal equivalent circuit of a diode is a resistance known as the dynamic resistance. The dynamic resistance is the reciprocal of the slope of the i_D versus v_D characteristic at the operating point.

7. P10.79 (5 pts)

P10.79 Dc sources voltage sources are replaced by short circuits in a small-signal equivalent circuit. By definition the voltage across a dc voltage source is constant. Thus, even if there is ac current flowing through the dc source the ac voltage across it is zero as is the case for a short circuit.

8. P10.80

P10.80 We should replace dc current sources by open circuits in a small-signal equivalent circuit. The current through a dc current source is constant. Thus, the ac current must be zero even if we apply an ac voltage. Zero current for a non-zero applied voltage implies that we have an open circuit.

9. P10.83

P10.83 We are given $v_D(t) = 5 + 0.01\cos(\omega t)$ V and $i_D(t) = 3 + 0.2\cos(\omega t)$ mA. The dynamic resistance is the ratio of the ac voltage amplitude to the ac current amplitude.

$$r_D = \frac{v_d}{i_d} = \frac{0.01}{0.2 \times 10^{-3}} = 50\ \Omega$$

The Q-point results if we set the ac signals to zero. Thus, we have

$$V_{DQ} = 5\text{ V} \quad \text{and} \quad I_{DQ} = 3\text{ mA}$$