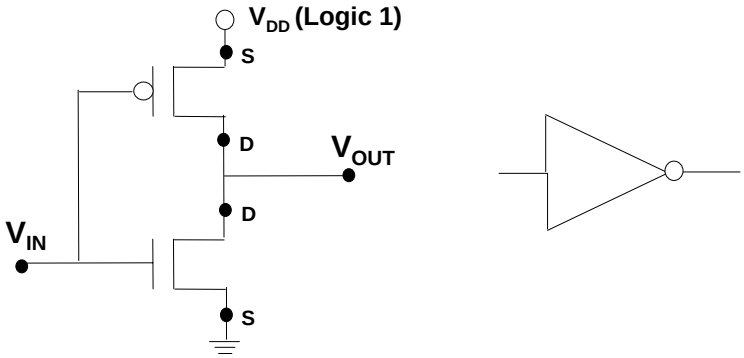
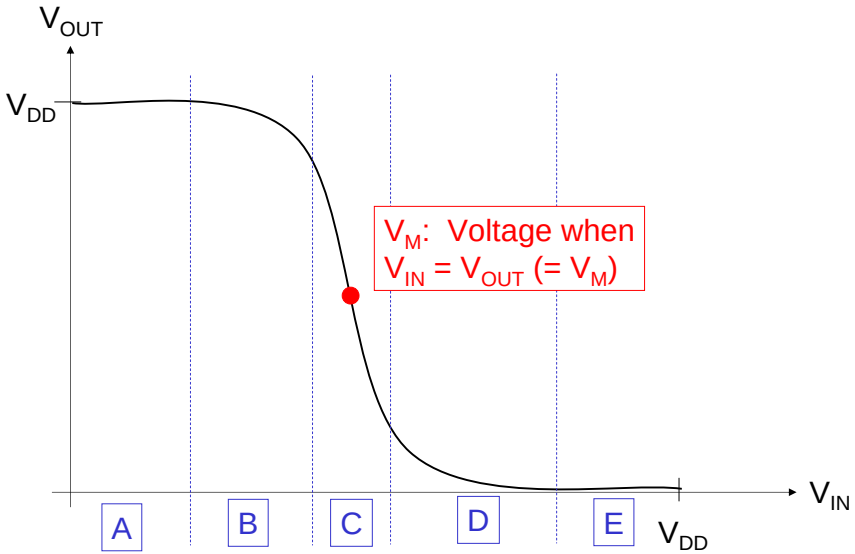
CMOS INVERTER

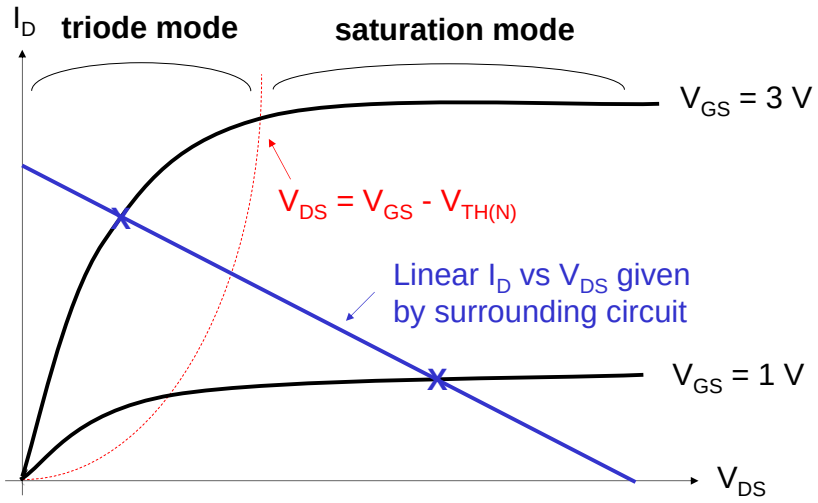
CMOS means Complementary MOS:
NMOS and PMOS working together in a circuit



CMOS INVERTER RESPONSE



LAST TIME: SINGLE TRANSISTOR CIRCUIT



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ANALYSIS OF INVERTER CIRCUT

Obtain:

1) the **<u>two</u> nonlinear** I_D vs. V_{DS} equations for the transistors: $I_{D(N)}$ vs. $V_{DS(N)}$ and $I_{D(P)}$ vs. $V_{DS(P)}$
2) A **linear** relationship between $I_{D(N)}$ and $I_{D(P)}$ (e.g., via KCL)
3) An **independent linear** relationship between $V_{DS(N)}$ and $V_{DS(P)}$ (e.g. via KVL)

Using the above, write:

$I_{D(P)}$ vs. $V_{DS(P)}$ in terms of $I_{D(N)}$ vs. $V_{DS(N)}$ (or vice-versa)

Solve the two transistor equations simultaneously.

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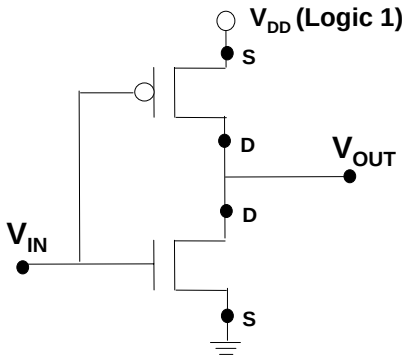
ANALYSIS OF INVERTER CIRCUIT: UNLOADED



1) Transistor equations:
$I_{D(N)} = f_N(V_{DS(N)})$
$I_{D(P)} = f_P(V_{DS(P)})$

2) $I_{D(P)}+I_{D(N)} = 0$

3) $V_{DS(N)}-V_{DS(P)} = V_{DD}$

Rewrite 1) as
$I_{D(N)} = -f_P(V_{DS(N)})-V_{DD})$

Find simultaneous solution to:

$I_{D(N)} = f_N(V_{DS(N)})$ $\qquad$ $I_{D(N)} = -f_P(V_{DS(N)})-V_{DD})$

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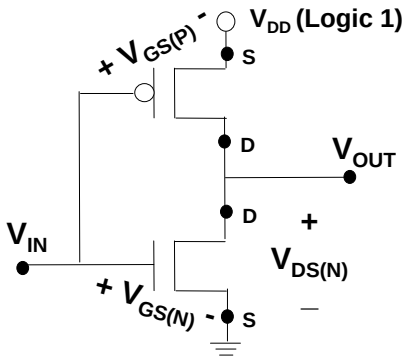
ANALYSIS OF INVERTER CIRCUIT: UNLOADED



Also note:

$V_{GS(N)} = V_{IN}$
$V_{GS(P)} = V_{IN} - V_{DD}$

$V_{OUT} = V_{DS(N)}$

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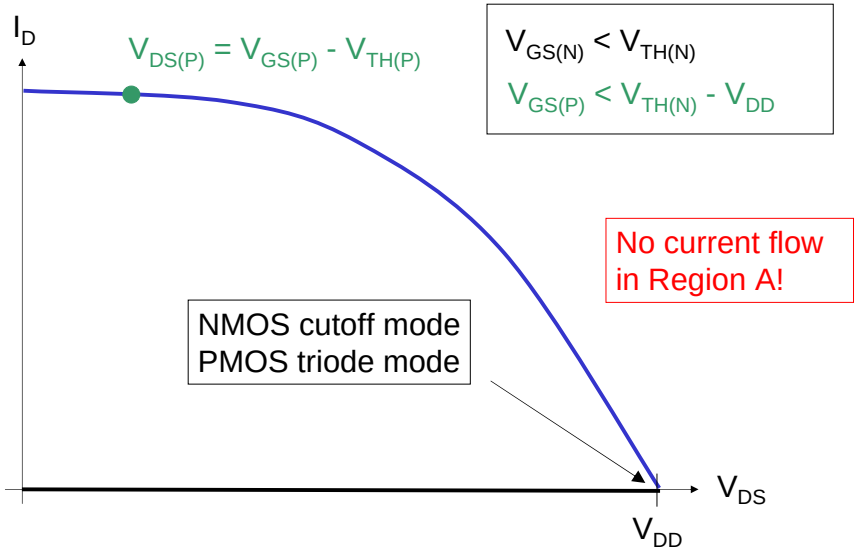
CMOS INVERTER: REGION A



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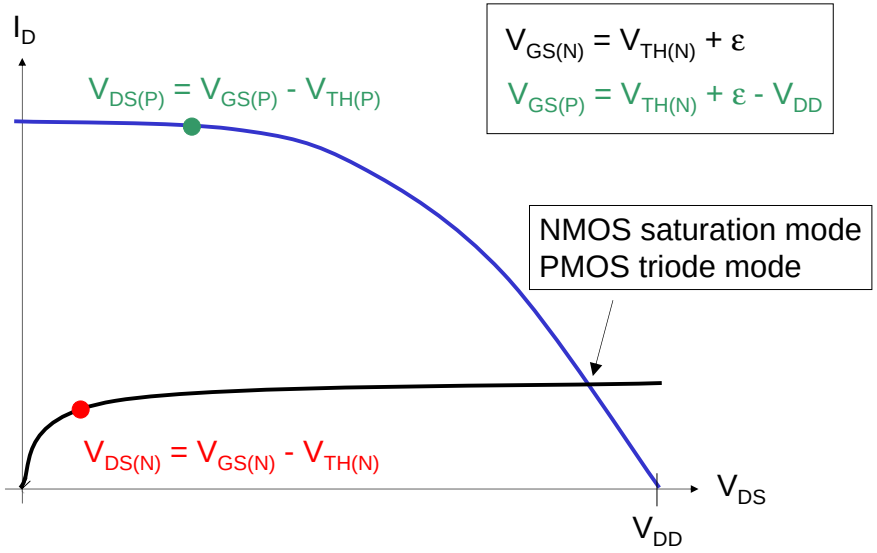
CMOS INVERTER: REGION B



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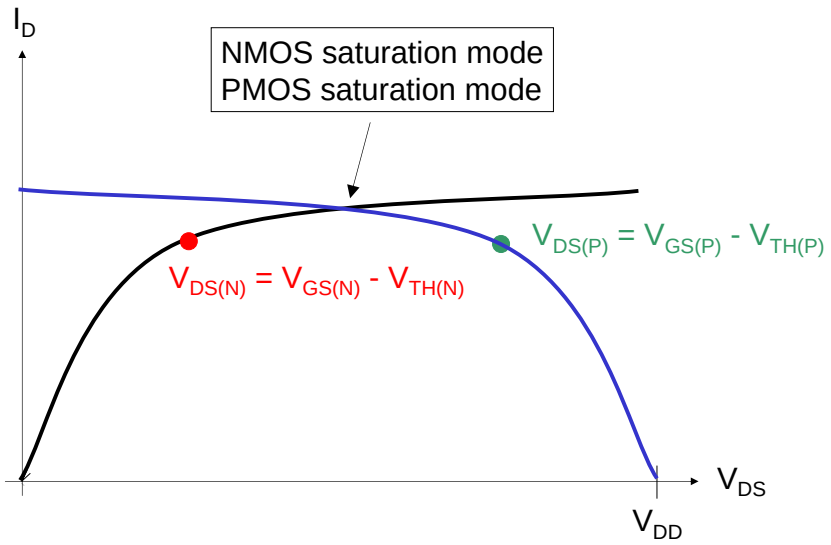
CMOS INVERTER: REGION C



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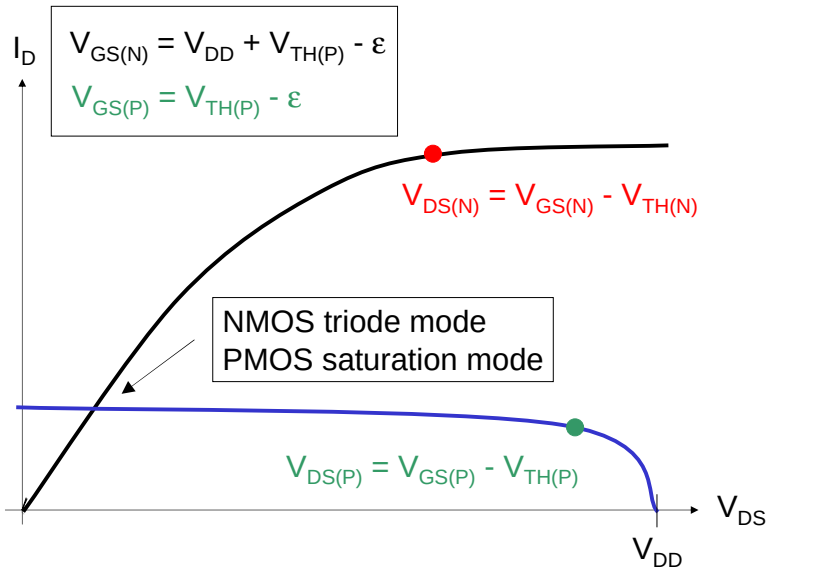
CMOS INVERTER: REGION D



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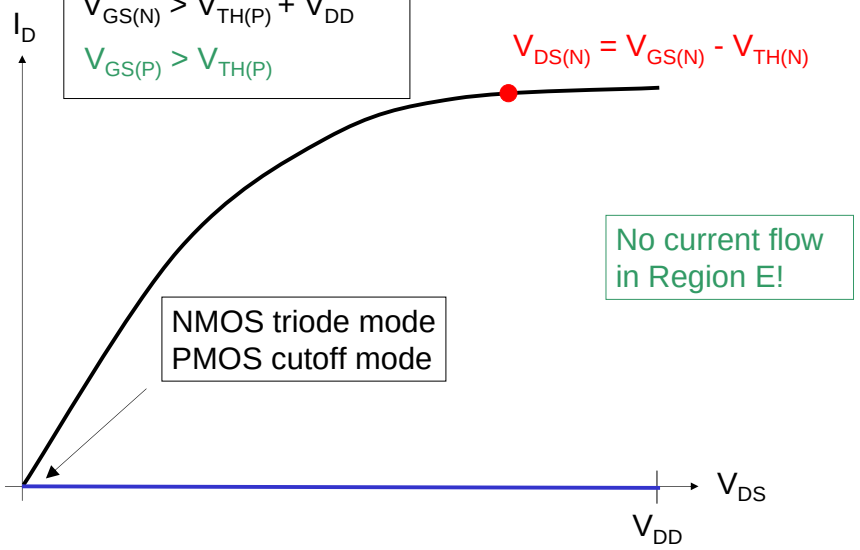
CMOS INVERTER: REGION E

$V_{GS(N)} > V_{TH(P)} + V_{DD}$

$V_{GS(P)} > V_{TH(P)}$



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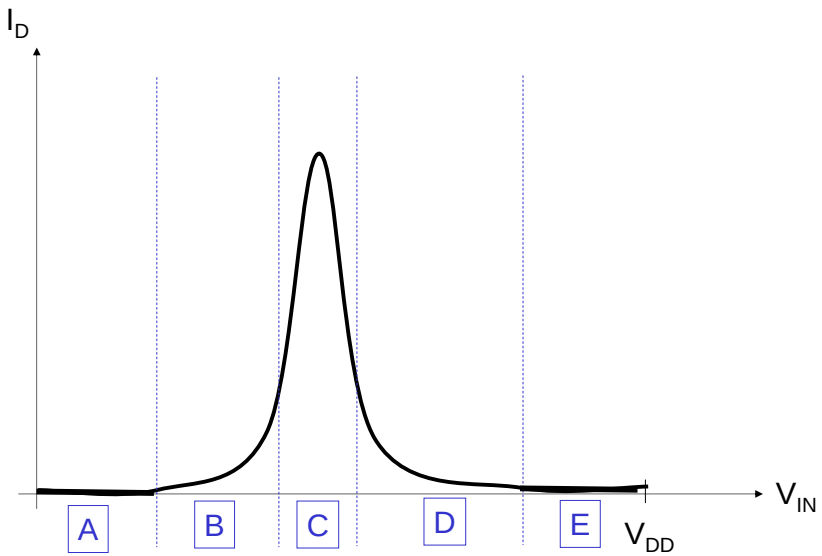
CMOS INVERTER RESPONSE: CURRENT FLOW



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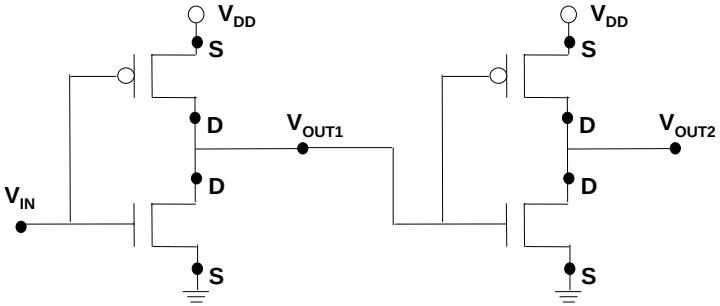
- No I_D current flow in Regions A and E if nothing attached to output; current flows only during logic transition
- If resistor or diode attached to output, current will flow through PMOS when input is low (output is high)
- If another inverter (or other CMOS logic) attached to output, transistor gate terminals of attached stage do not permit current: current flows only during logic transition



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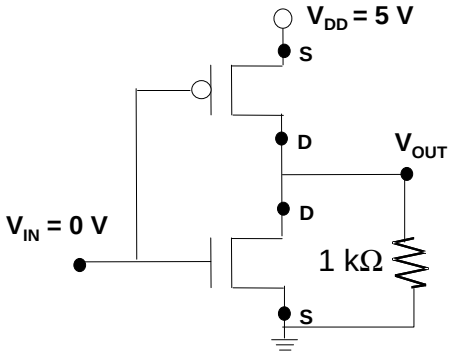
EXAMPLE: RESISTIVE LOAD



Find the power absorbed by the resistor and the inverter.

Power absorbed by inverter:
$P = I_{D(P)}V_{DS(P)} + I_{D(N)}V_{DS(N)}$

Let W/L μ C_{OX} = 1 mA,
$V_{TH(N)} = -V_{TH(P)}$ = 1 V,
λ = 0.

1) Transistor equations:

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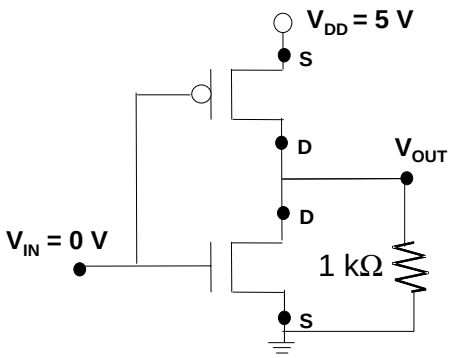
EXAMPLE: RESISTIVE LOAD



2) $I_{D(N)}$ and $I_{D(P)}$ relationship:

3) $V_{DS(N)}$ and $V_{DS(P)}$ relationship:

4) Substitute into PMOS transistor equation:

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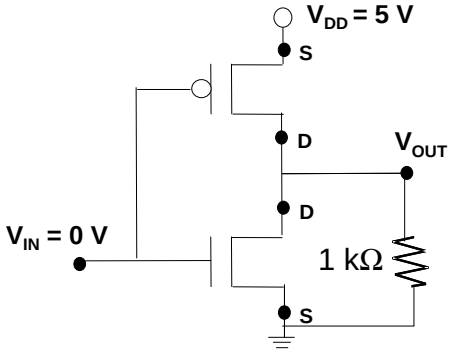
EXAMPLE: RESISTIVE LOAD



5) Solutions:

$V_{DS(P)}$ =

$I_{D(P)}$ =

Power absorbed by inverter: $I_{D(P)}V_{DS(P)} + I_{D(N)}V_{DS(N)}$ =

Power absorbed by resistor: $R\ I^2$ =

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