Administrivia

- HW #5 changes
- HW #6
  - Will be up by tonight, 5 problems
  - Due next Wednesday (08/06)
  - Will be a good review for the midterm
- Return HWs 4 and 5 on Monday (08/04)
- Return HW 3 and corrected HWs 1 and 2 on Friday (08/01)
- Midterm II next Wednesday, 08/06/03!
- Practice problems up by tonight
- Review session?

Last time...

- CMOS voltage transfer characteristic
  - SUGGESTION: Go over lecture 16 STEP-BY-STEP
  - Ask questions in discussion and office hours!

This time...

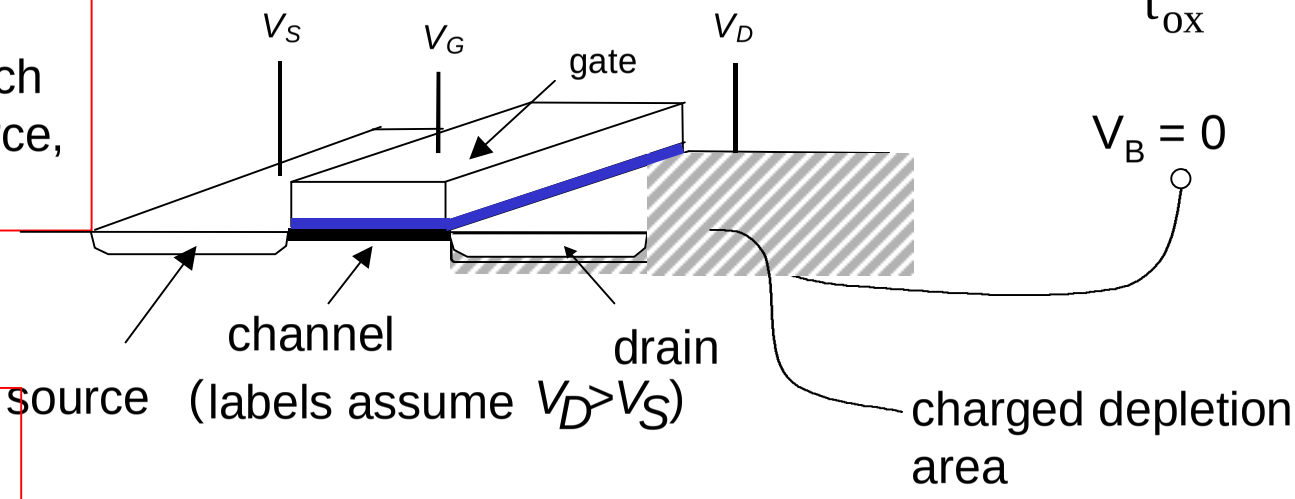
- CMOS inverter propogation delay analysis
  - Complete our propogation delay model
  - Understand MOS capacitances
  - Switch-RC model of the CMOS inverter
  - Understand τ_{LH} and τ_{HL}
- CMOS layouts and fabrication steps
- Extract capacitances, W and L from layout/crossection
- References: Lectures 18 and 19 (Fall 1999) and Lecture 21 (Spring 2003)

MOSFET Capacitances

Node connected to the gate:

Capacitance C_G is between gate and the underlying channel, which is connected to the source, $C_{GS} = C_G$

$$C_G = C_{ox} \times W \times L = \frac{\varepsilon_{ox} WL}{t_{ox}}$$



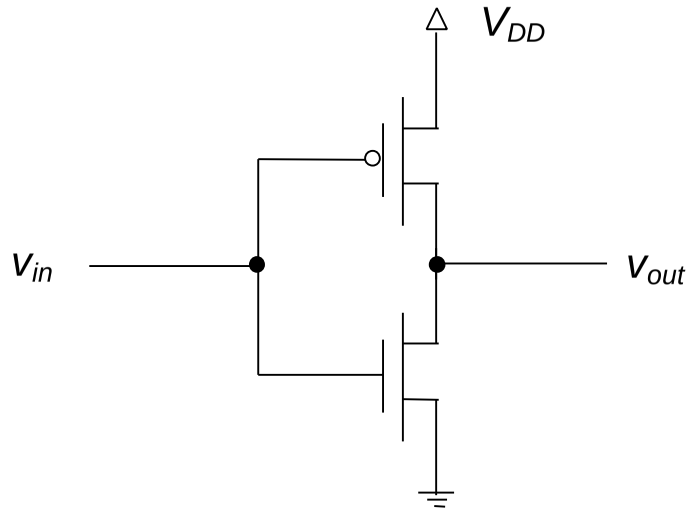
And C_{DB} is capacitance between drain electrode and body (bulk).

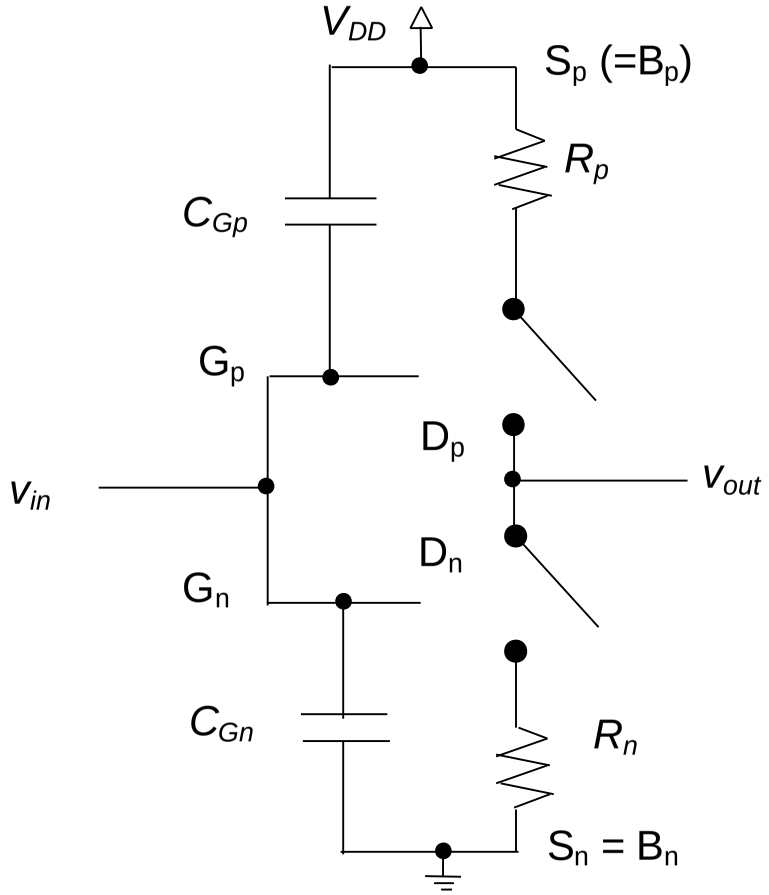
Node connected to the drain (or source):

- pn junction capacitance between drain and bulk is C_{DB}
- capacitance C_{SB} is shorted out since $V_S = V_B$ in digital circuits

The CMOS Inverter

Symbolic circuit





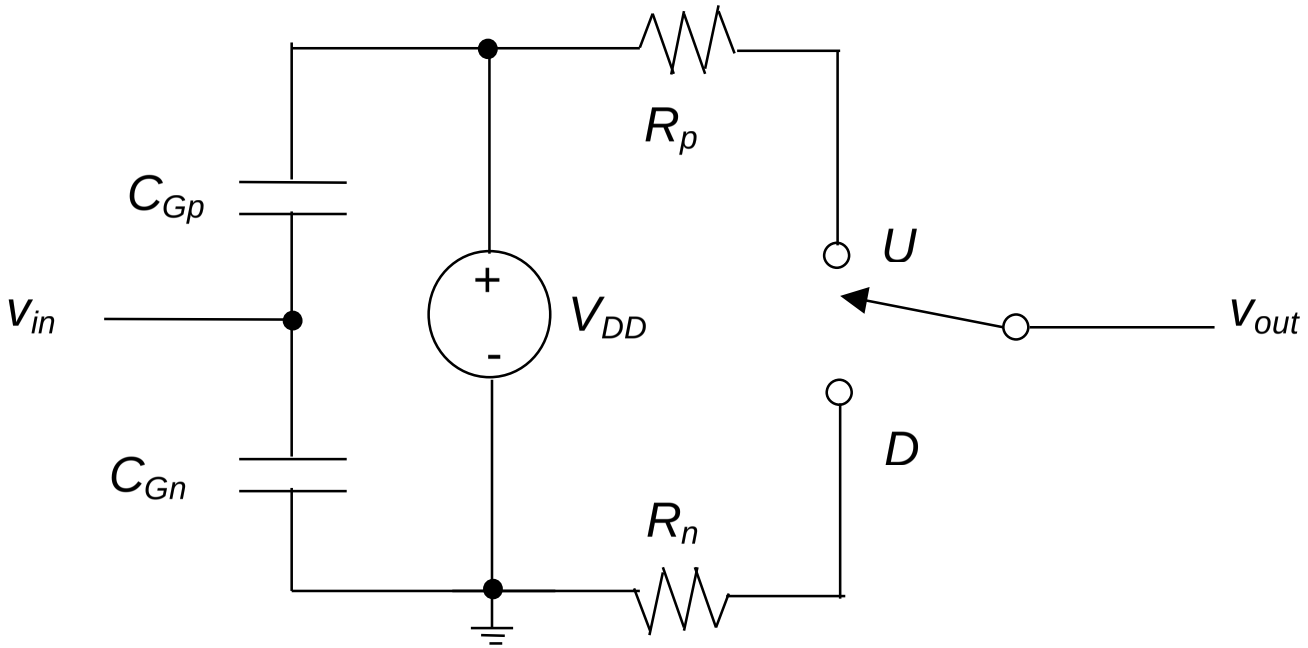
First Order CMOS Inverter Model

The switches are "ganged" (move together) since they have the same trip voltages

NMOS is closed when $v_{in} > V_{Th}$; PMOS is open

PMOS is closed when $v_{in} < V_{Tl}$; NMOS is open

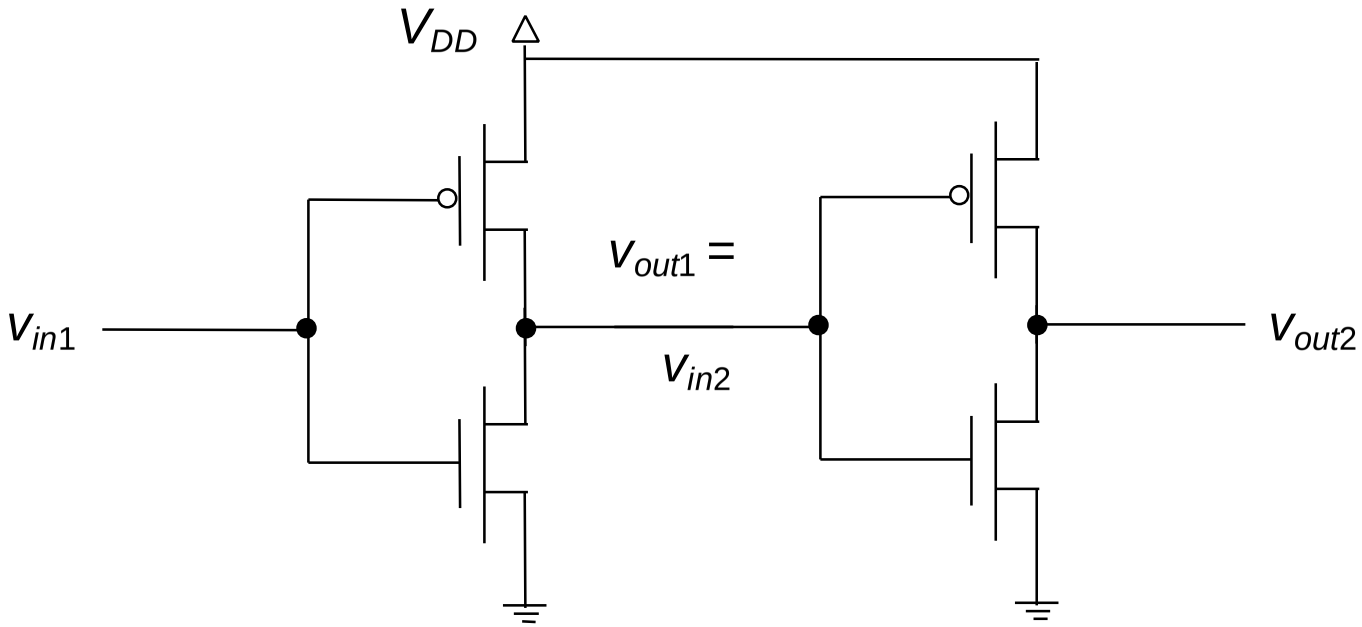
Reduce to a single switch (Fig. 2.10, R&R)



"Cascaded" CMOS Inverters

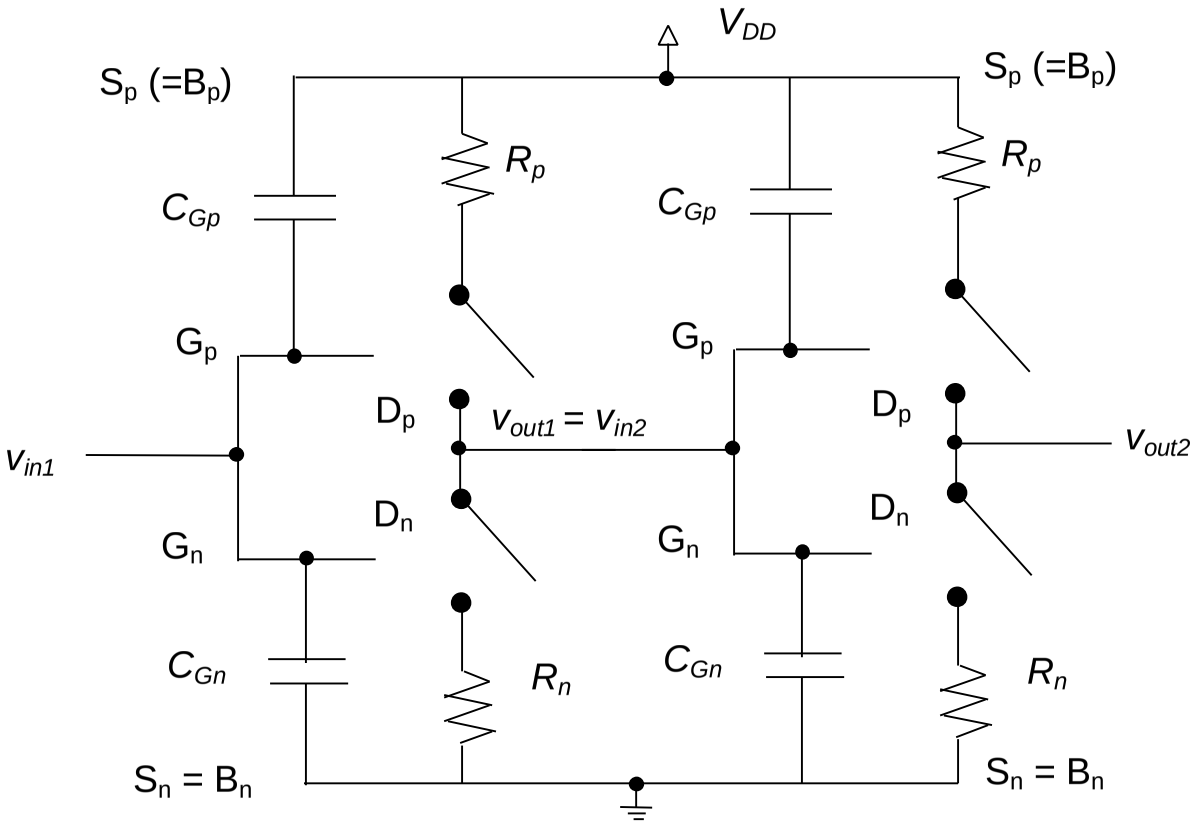
What's connected to the v_{out} node?

Representative "load" … possibly another CMOS inverter



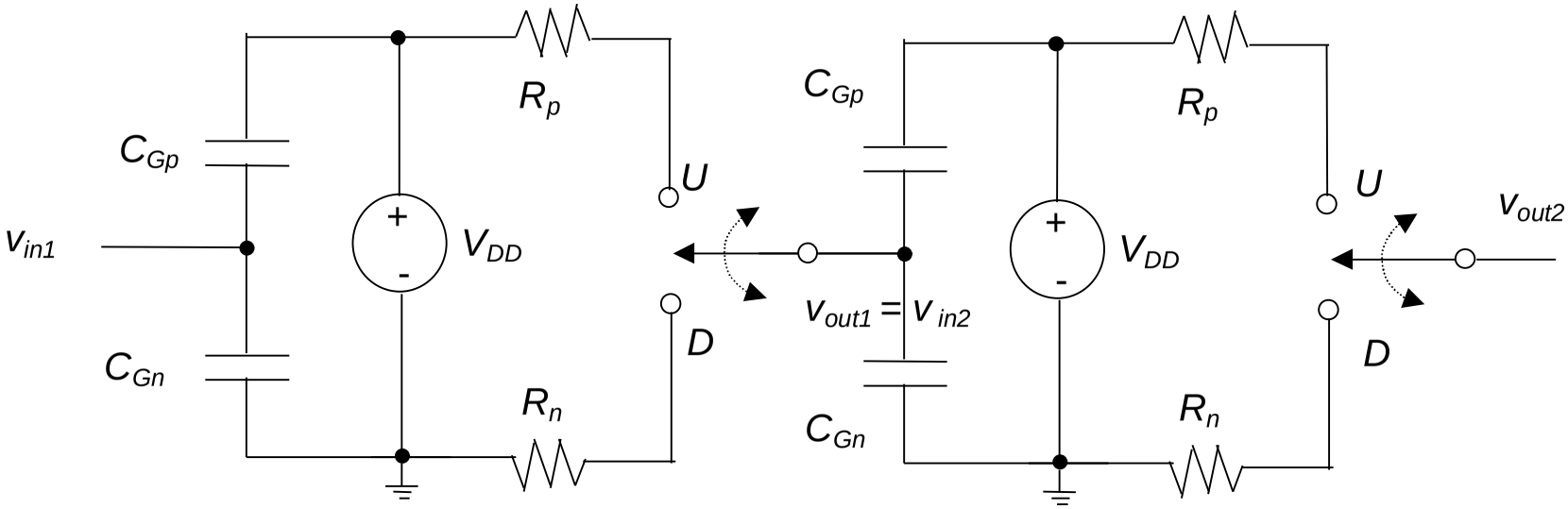
Cascaded Identical CMOS Inverter Circuit Model

Drain-bulk capacitances are omitted (at first), as is interconnect resistance and cap.



Simpler Representation

NMOS and PMOS transistors have the same logic thresholds, but operate in a complementary fashion → reduce to a single switch per inverter

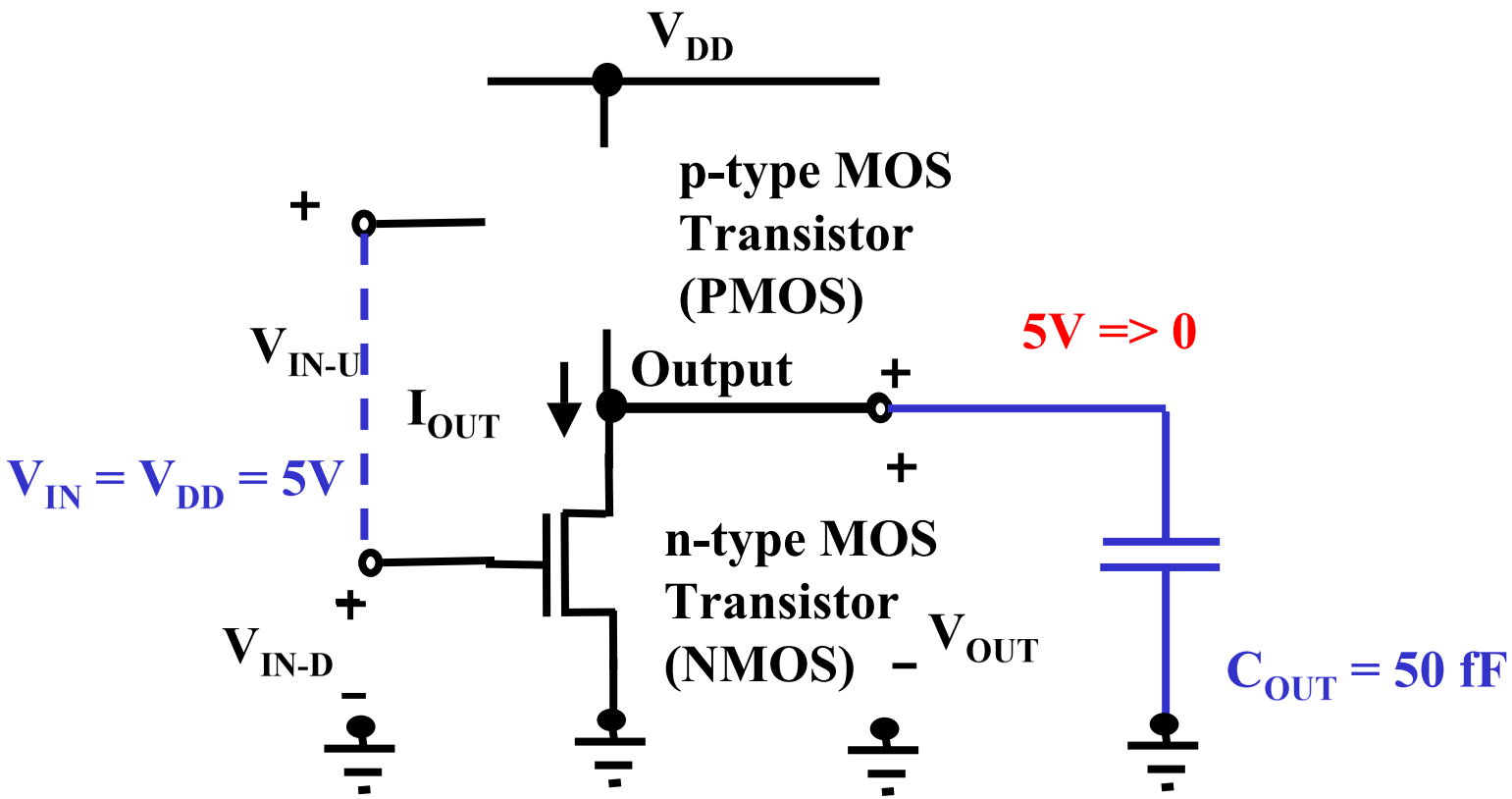


Transitions of interest:

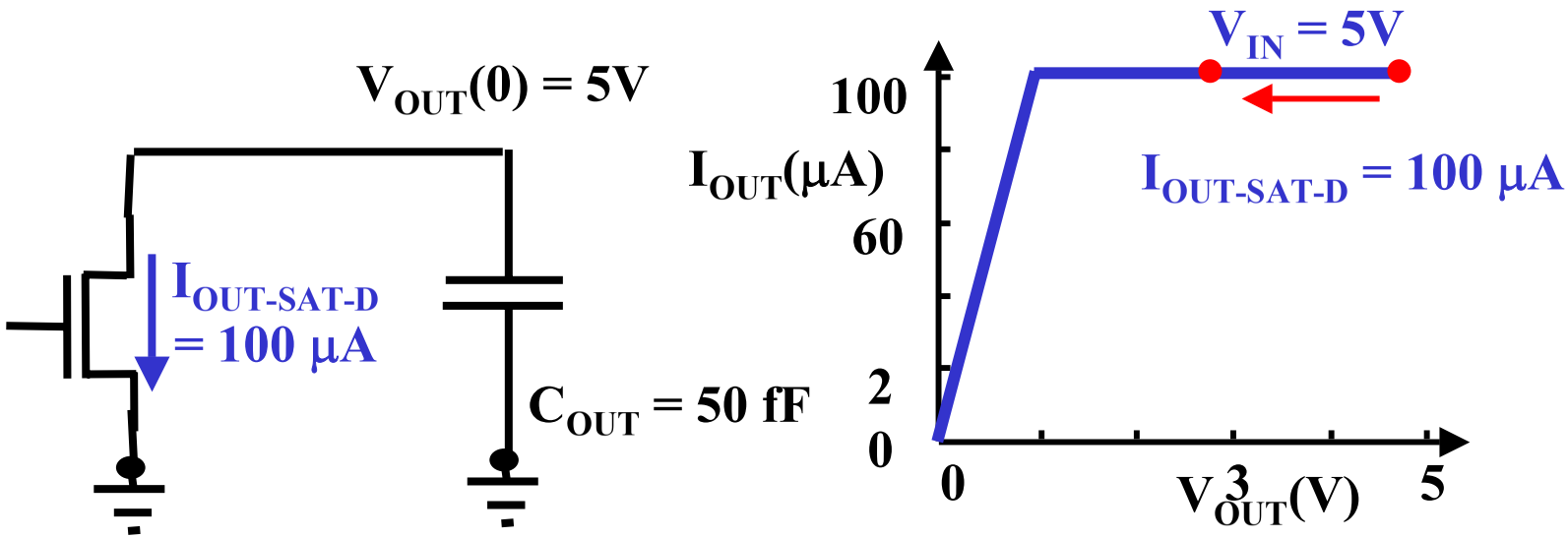
1. v_{in1} increases above V_{Th} : switch for inverter 1 moves to "D" position from previous "U" position

2. v_{in1} decreases below V_{Tl} : switch for inverter 1 moves to "U" position from previous "D" position

Transient Gate Problem: Discharging and Charging Capacitance on the Output



Output Propagation Delay High to Low

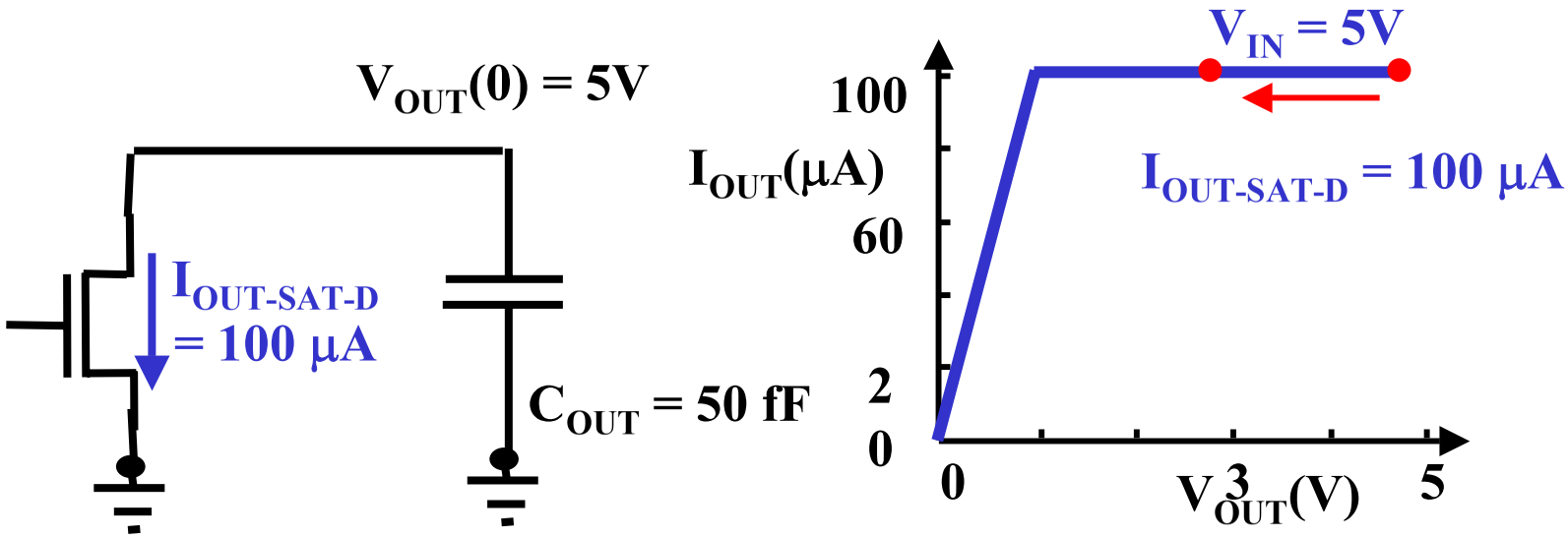


When V_{IN} goes High V_{OUT} starts decreases with time

Assume that the necessary voltage swing to cause the next downstream gate to begin to switch is $V_{DD}/2$ or 2.5V.

That is the propagation delay τ_{HL} for the output to go from high to low is the time to go from V_{DD} = 5V to to $V_{DD}/2$ =2.5V

Output Propagation Delay High to Low (Cont.)



When $V_{OUT} > V_{OUT\text{-}SAT\text{-}D}$ the available current is $I_{OUT\text{-}SAT\text{-}D}$

For this circuit when $V_{OUT} > V_{OUT\text{-}SAT\text{-}D}$ the available current is constant at $I_{OUT\text{-}SAT\text{-}D}$ and the capacitor discharges.

The propagation delay is thus

$$\Delta t = \frac{C_{OUT}\Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = \frac{50\,fF \cdot 2.5V}{100\,\mu A} = 1.25ns$$

Switched Equivalent Resistance Model

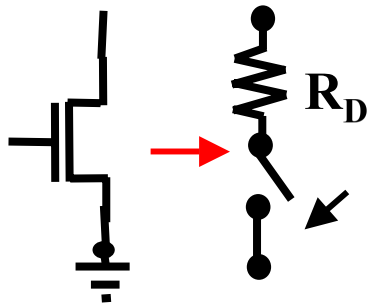
The above model assumes the device is an ideal constant current source.

1) This is not true below $V_{OUT\text{-}SAT\text{-}D}$ and leads to in accuracies.

2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting $0.69R_DC$ equal to the Δt found above

$$\Delta t = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_DC_{OUT}$$

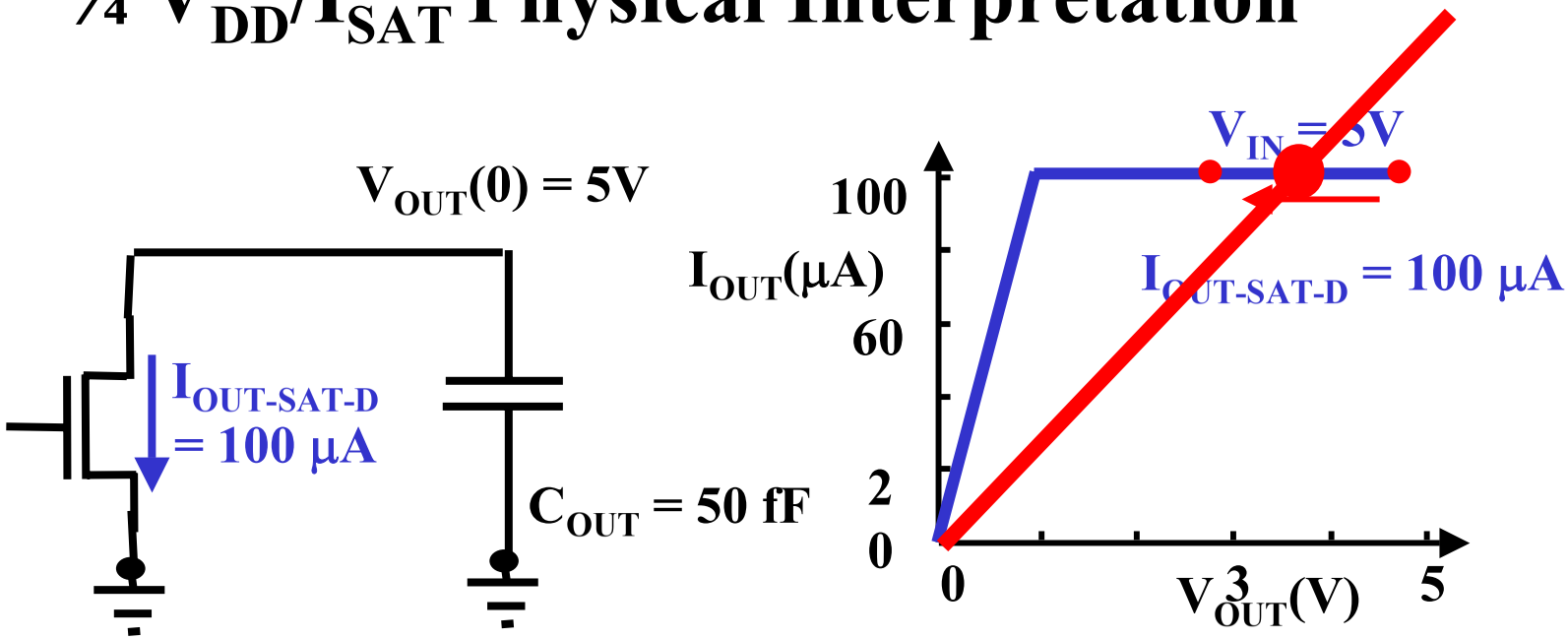


This gives

$$R_D = \frac{V_{DD}}{2\cdot(0.69)I_{OUT-SAT-D}} \approx \frac{3}{4}\frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4}\frac{5V}{100\mu A} = 37.5k\Omega$$

Each device can now be replaced by this equivalent resistor.

¾ V_{DD}/I_{SAT} Physical Interpretation



¾ V_{DD} is the average value of V_{OUT}

Approximate the NMOS device curve by a straight line from (0,0) to ($I_{OUT-SAT-D}$, ¾ V_{DD}).

Interpret the straight line as a resistor with

$$1/(\text{slope}) = R = ¾\ V_{DD}/I_{SAT}$$

Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

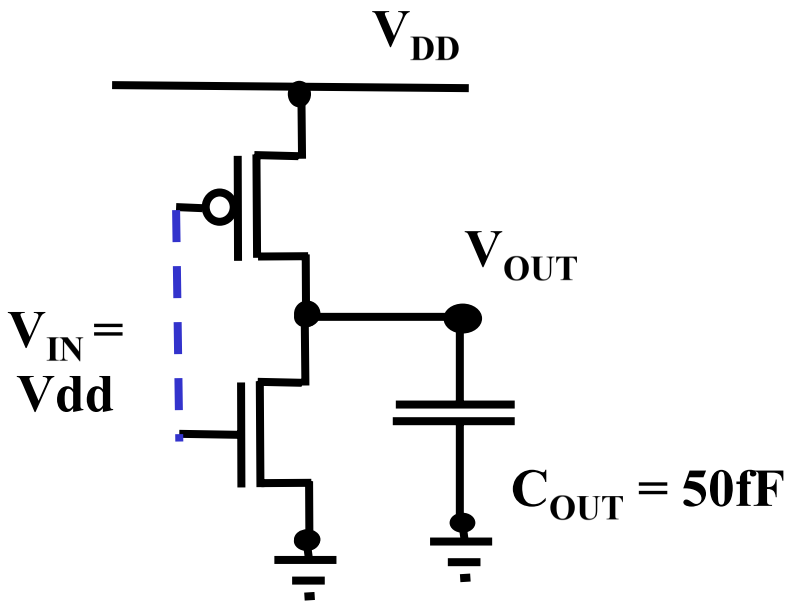
Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

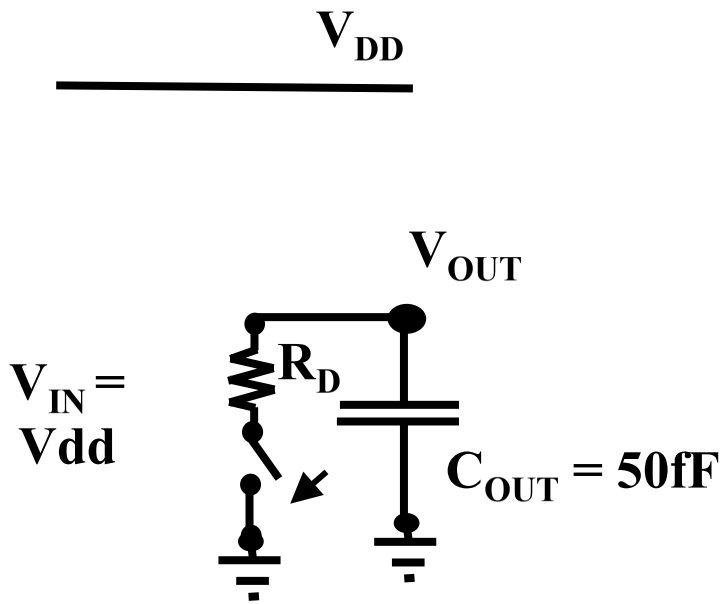
The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume $R_D = R_U = 10\ k\Omega$

Inverter Propagation Delay

Discharge (pull-down)





$$\Delta t = 0.69 R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345\ ps$$

Discharge (pull-up)

$$\Delta t = 0.69 R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345\ ps$$

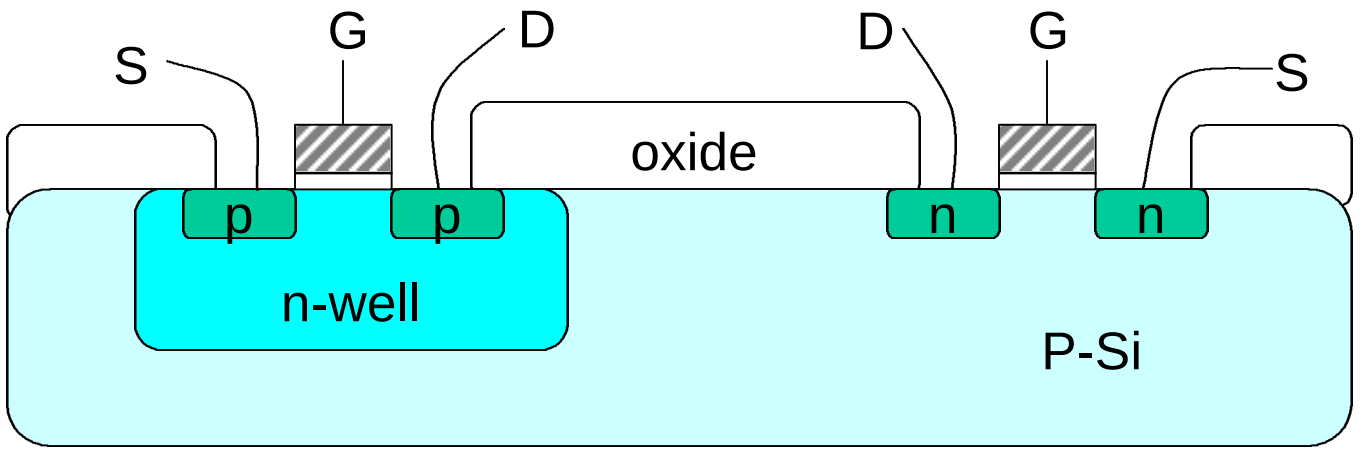
CMOS

Challenge: build both NMOS and PMOS on a single silicon chip

NMOS needs a p-type substrate

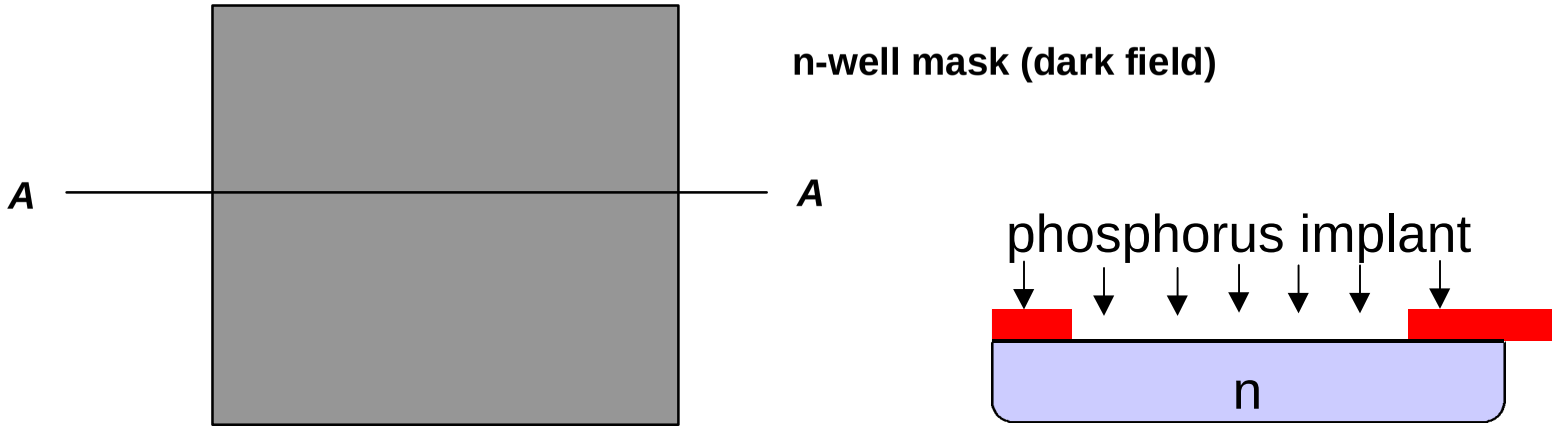
PMOS needs an n-type substrate

Requires extra process steps



Additional Steps for CMOS

Well Formation



Process (before transistor fabrication)

1. start with p-type wafer; grow 250 nm oxide
2. pattern oxide with n-well mask
3. implant with phosphorus and anneal to form a 3 μm-deep n-type region

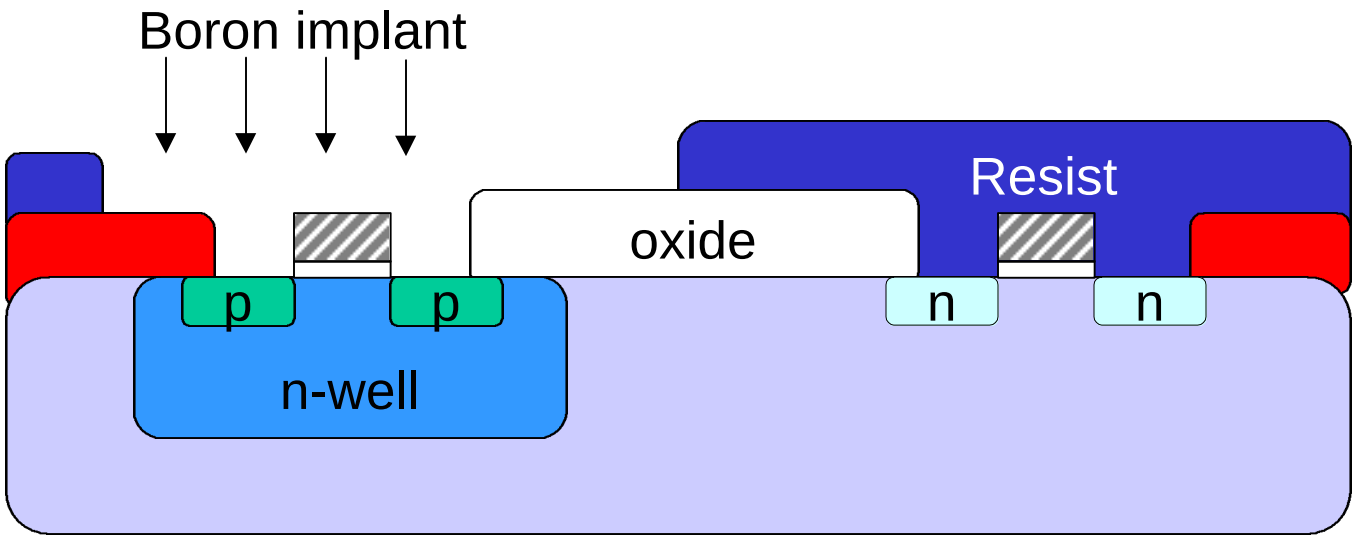
FIRST ADDITIONAL COMPLICATION:

We must mask source-drain implants

"Select P-Channel" ↘ We must protect n-channel device during boron implant **and**

"Select N-Channel" ↗ We must protect p-channel device during As implant)

Example: Select P ch



Moreover, it looks like reverse of the well mask, i.e., a "clearfield well mask" would work for the "select n-channel" mask.

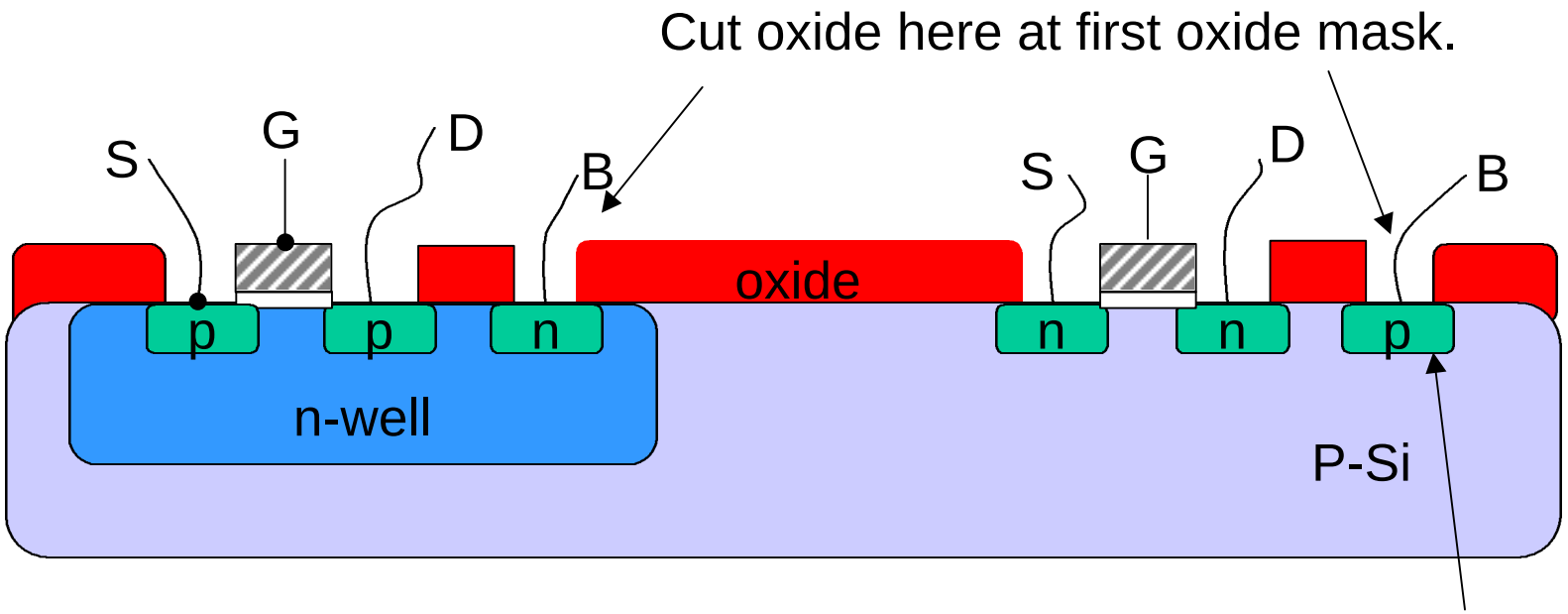
AND ONE MORE COMPLICATION:

We need contacts to “body” or well and body of p-region

Easy to do – just modify “select” masks and oxide masks, i.e.,

① Create thin oxide spots for contact in original oxide mask, and

②Allow openings in select masks to dope these regions



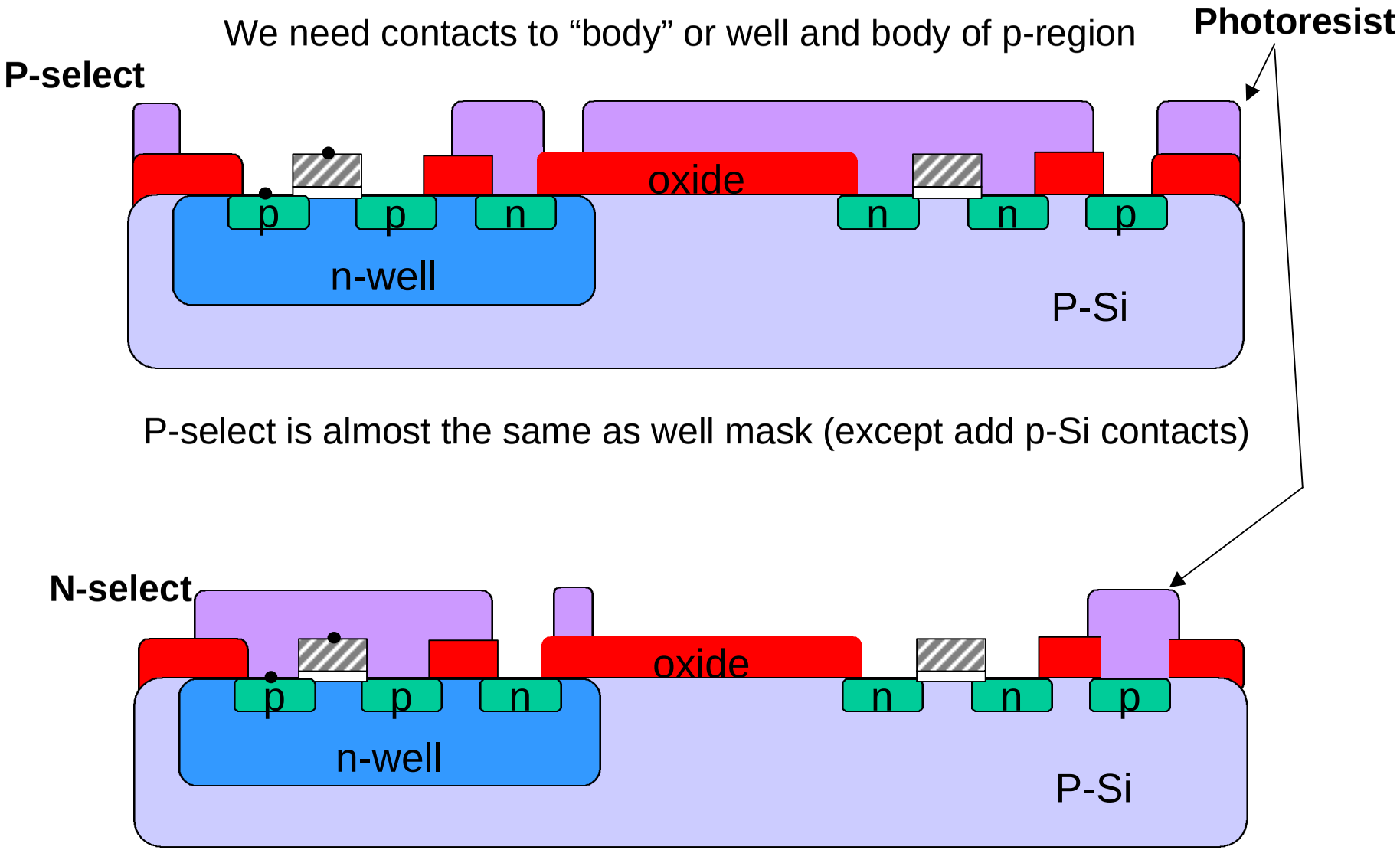
p implant area in substrate is to make electrical contact by Al wire easier

How to get n-regions implanted selectively with arsenic?

Could simply invert polarity of select mask at contacts.

Cross-sections for Select Masks

We need contacts to “body” or well and body of p-region

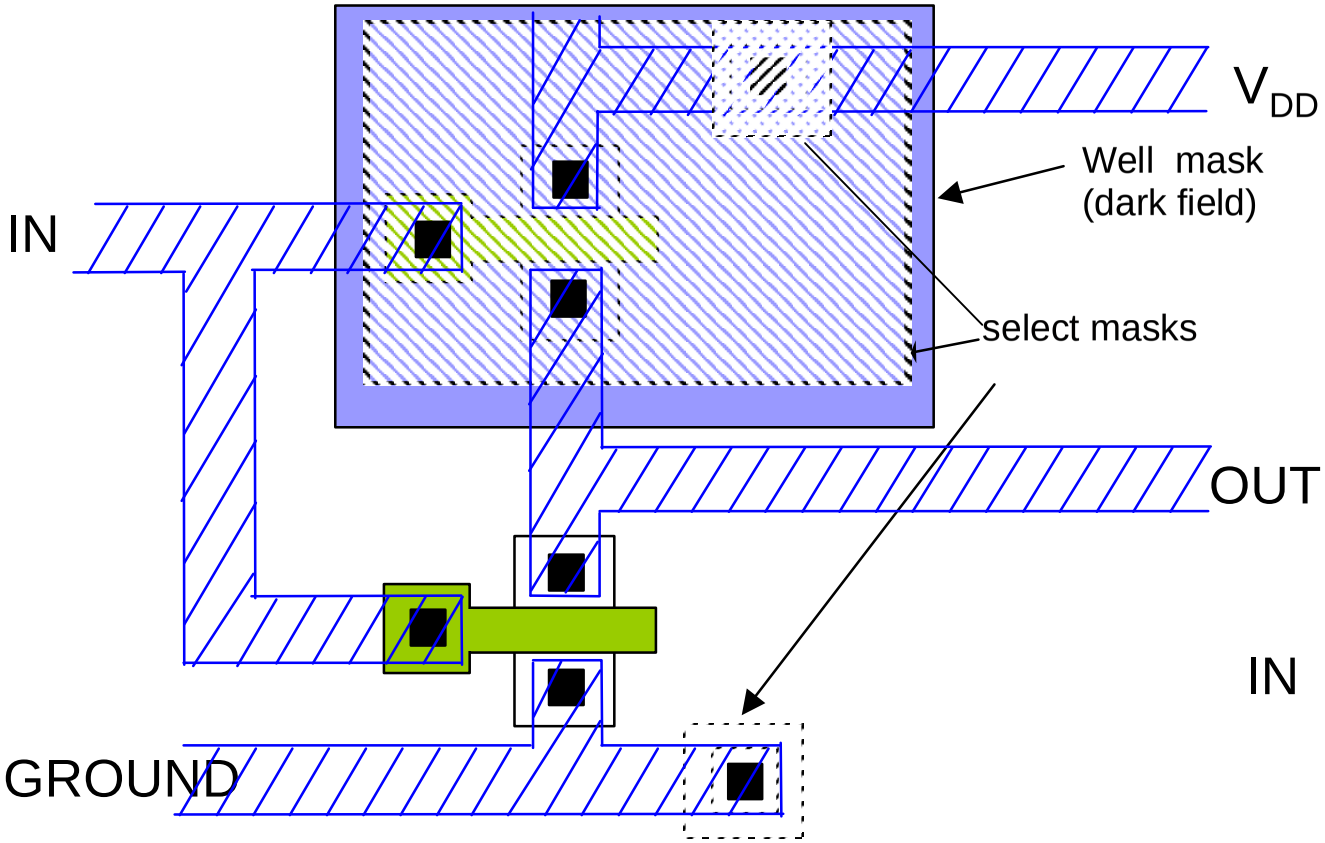


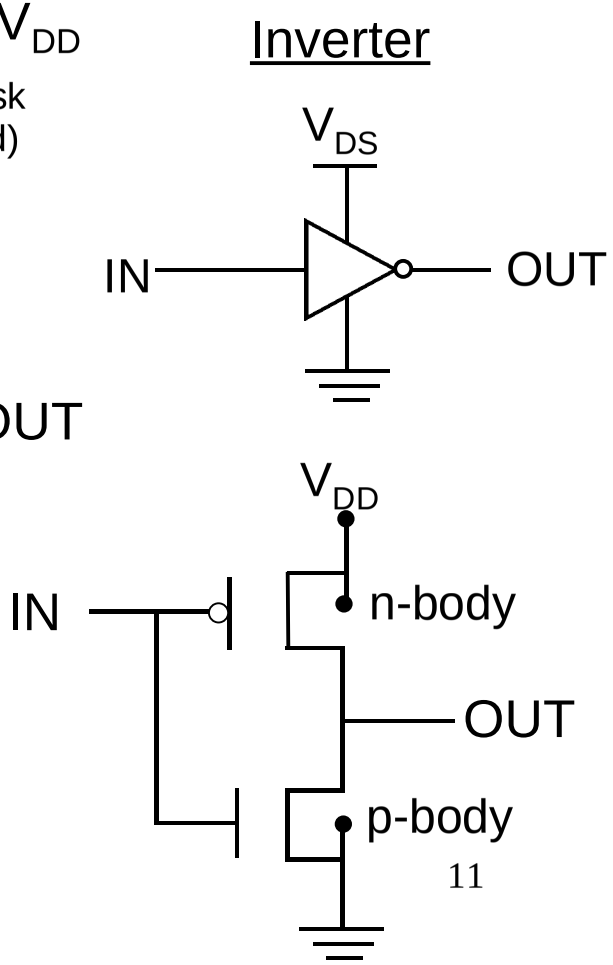
P-select is almost the same as well mask (except add p-Si contacts)

N-select is almost dark-field of well mask (except add n-Si contacts)

Basic CMOS Process

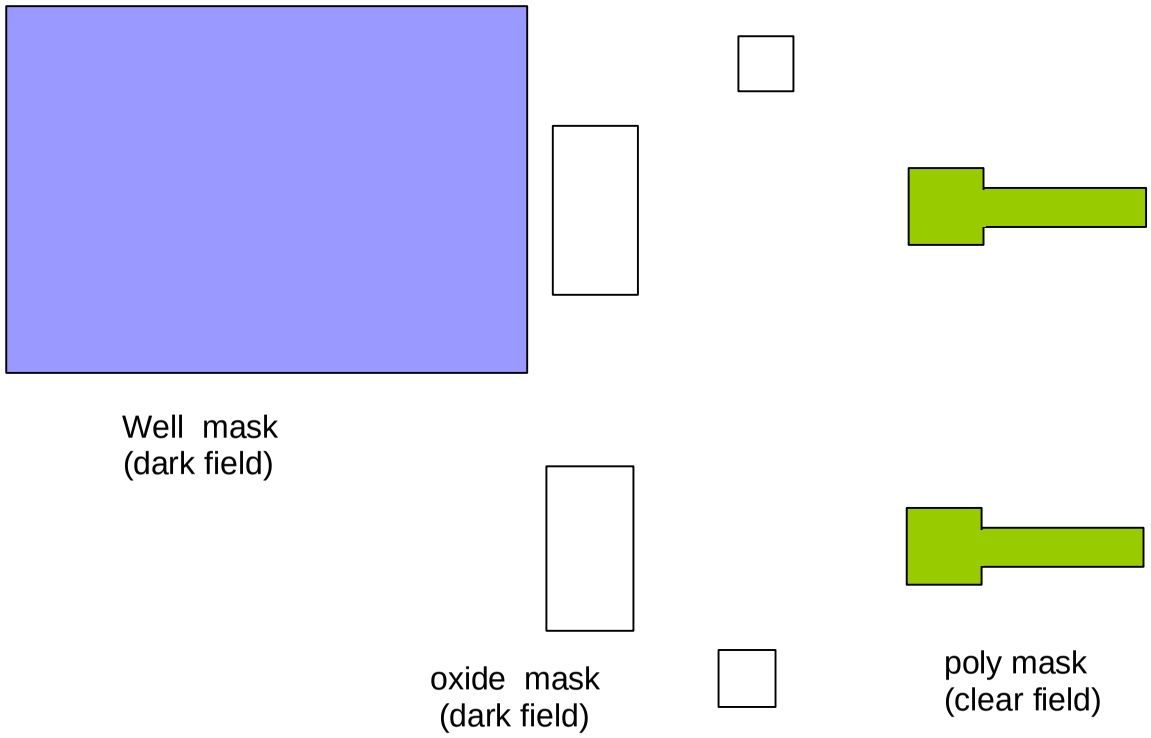
Well mask + select mask(s) + NMOS process





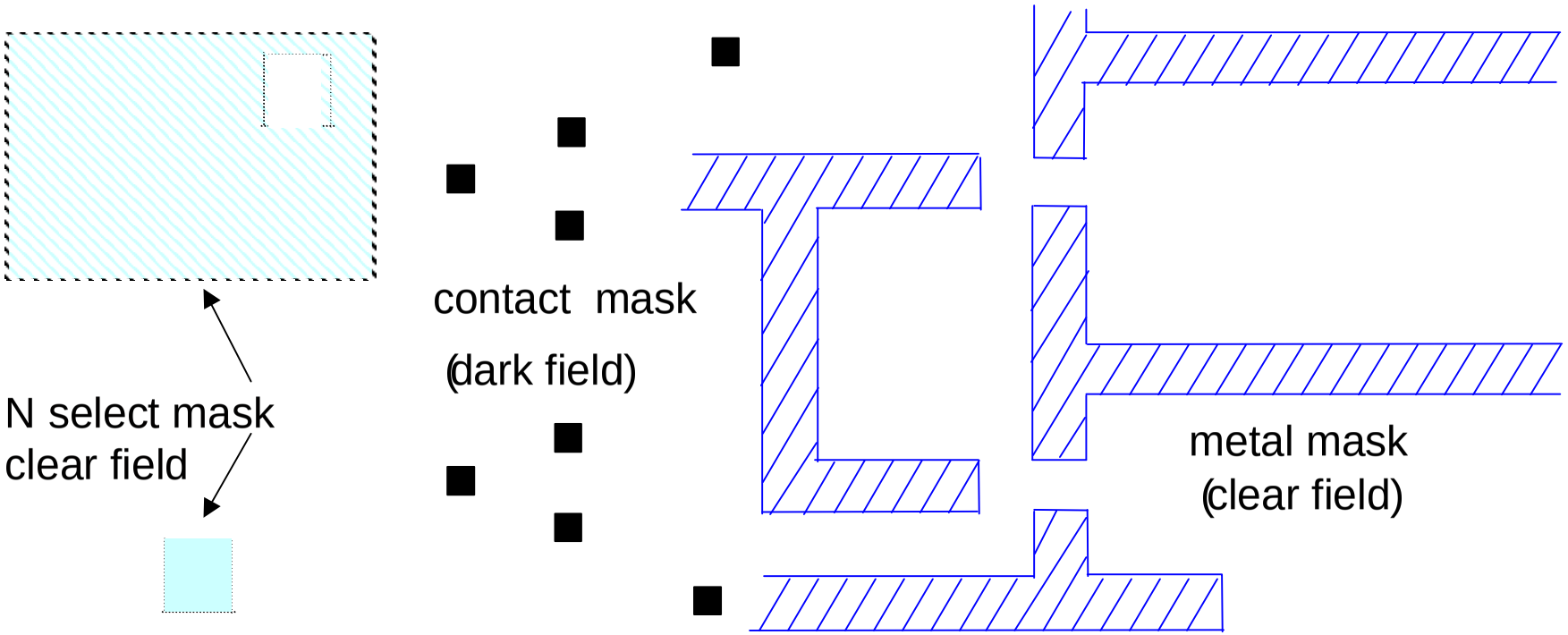
Separate Masks

Well, oxide, and polysilicon masks



Separate Masks (cont.)

Select masks, contact mask, and metal mask



CMOS Process Sequence

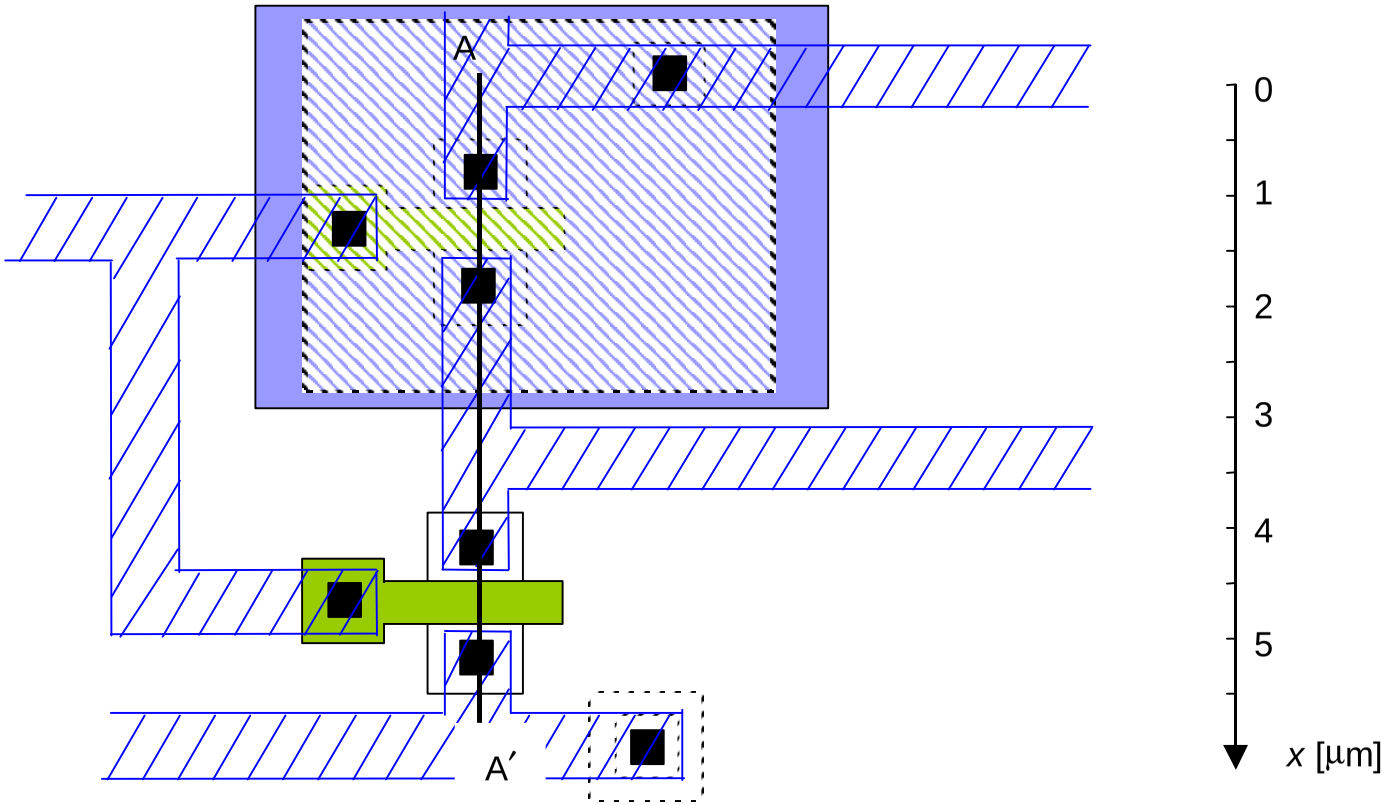
1. **p-type starting material; grow 500 nm of oxide**
2. **pattern oxide with well mask**
3. **implant phosphorus and anneal (“well drive in”) to a depth of 3 μm**
4. **strip off oxide**
5. **grow 500 nm of oxide**
6. **pattern with oxide mask**
7. **grow 5 nm of oxide**
8. **deposit 500 nm of n^+ polysilicon**
9. **pattern with poly mask**
10. **spin on resist**
11. **pattern with the select mask (dark field)**
12. **implant boron; strip off resist**
13. **spin on resist**
14. **pattern with the select mask (clear field)**

Same pattern except for well and substrate contacts

CMOS Process Sequence (cont.)

15. implant arsenic; strip off resist and anneal implants to form source and drain regions
16. deposit 500 nm of oxide
17. pattern using contact mask (dark field)
18. deposit 1 μm of aluminum
19. pattern using metal mask (clear field)

CMOS Cross Sections



Conclusion

- Completed our propogation delay model
- Switch-RC model of the CMOS inverter
- τ_{LH} and τ_{HL} calculations
- CMOS layouts and fabrication steps
- References: Lectures 18 and 19 (Fall 1999) and Lecture 21 (Spring 2003)

Next time...

- Barring unforseen circumstances: GUEST LECTURE BY PROF. TSU JAE-KING
- HW #5 due!
- START PREPARING FOR MIDTERM!