

Lecture 19

Last time:

Transistor Fabrication

NMOS = n-channel Metal Oxide Semiconductor Field Effect Transistor

CMOS is a process that uses both NMOS and PMOS devices (complementary)

CMOS adds masks to the process (more cost) but advantages include low power consumption and noise immunity (more later)

Today - back to Reed and Rohrer, Ch. 2

- Equivalent Circuits for NMOS and PMOS
- Simple "zeroth-order model and refinements
- CMOS inverter

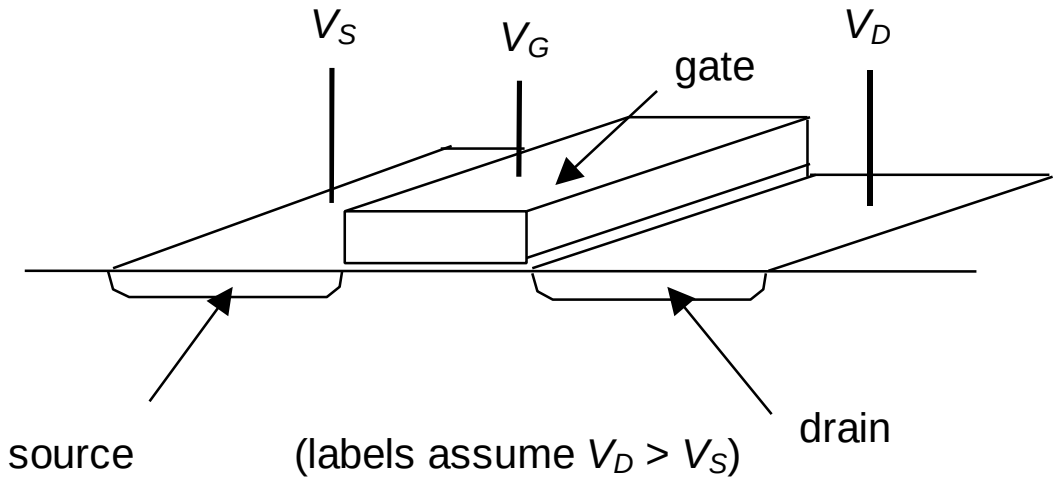
MOSFET Terminology

Label the three electrical terminals on the top surface:

Gate: controls whether the switch is conducting or not

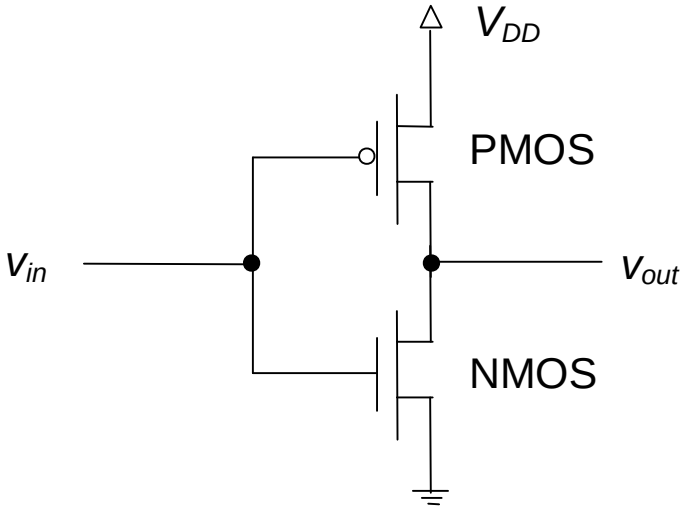
Source: NMOS: the lower potential of the two n regions, often GND
PMOS: the higher potential of the two n regions, often V_{DD}

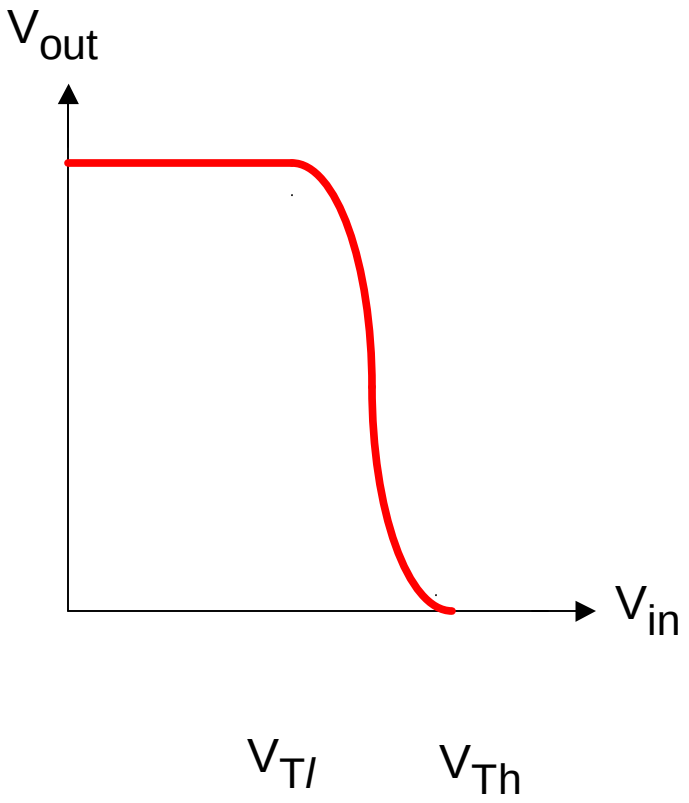
Drain: NMOS: the higher potential of the two n regions
PMOS: the lower potential of the two n regions



CMOS TRANSFER CURVE (Vout vs Vin)

On the home-problem set you found the transfer curve to be of the form:

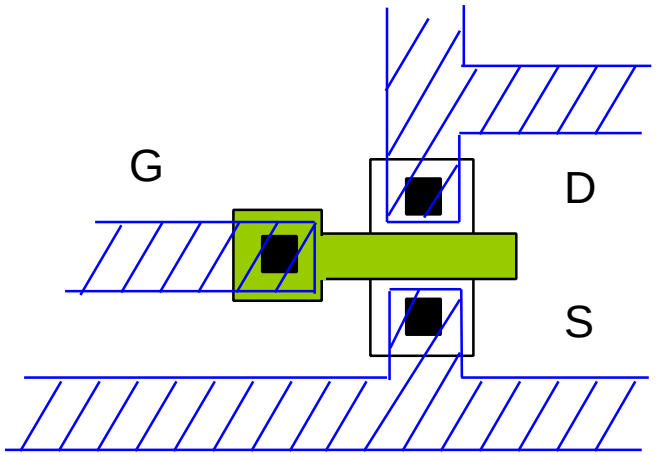


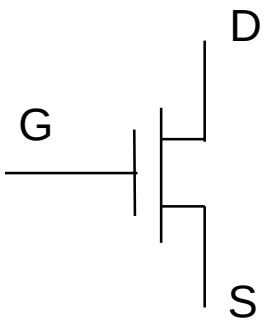


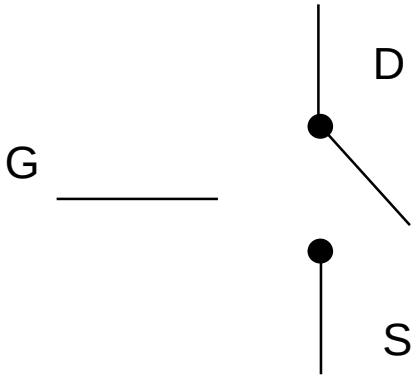
For $V_{in} < V_{T/}$ NMOS off , PMOS on

For $V_{in} > V_{Th}$ NMOS on , PMOS off

NMOS Transistor "Switch Model"







Switching thresholds:

Define for "default" digital circuit connection,

V_S **= 0 V (ground)**

$V_G = v_{in}$ **(input voltage)**

NOTE: Textbook uses V_{th} and V_{tl} for "thresholds" instead of dealing with a single V_T and equations.

Switch is *closed* (Drain (D) is shorted to Source (S)) when $v_{in} > V_{Th}$

Switch is *open* (Drain (D) is disconnected from Source (S)) when $v_{in} < V_{Tl}$

Logic Threshold Voltages

***Low* logic threshold V_{Tl}**

Typically around 25% of the supply voltage for CMOS

Interpretation: NMOS transistor is "off" for input voltages less than V_{Tl}

***High* logic threshold V_{Th}**

Typically around 75% of the supply voltage for CMOS

Interpretation: NMOS transistor is "on" and conducting for inputs greater than V_{Th}

What about "in-between" voltages?

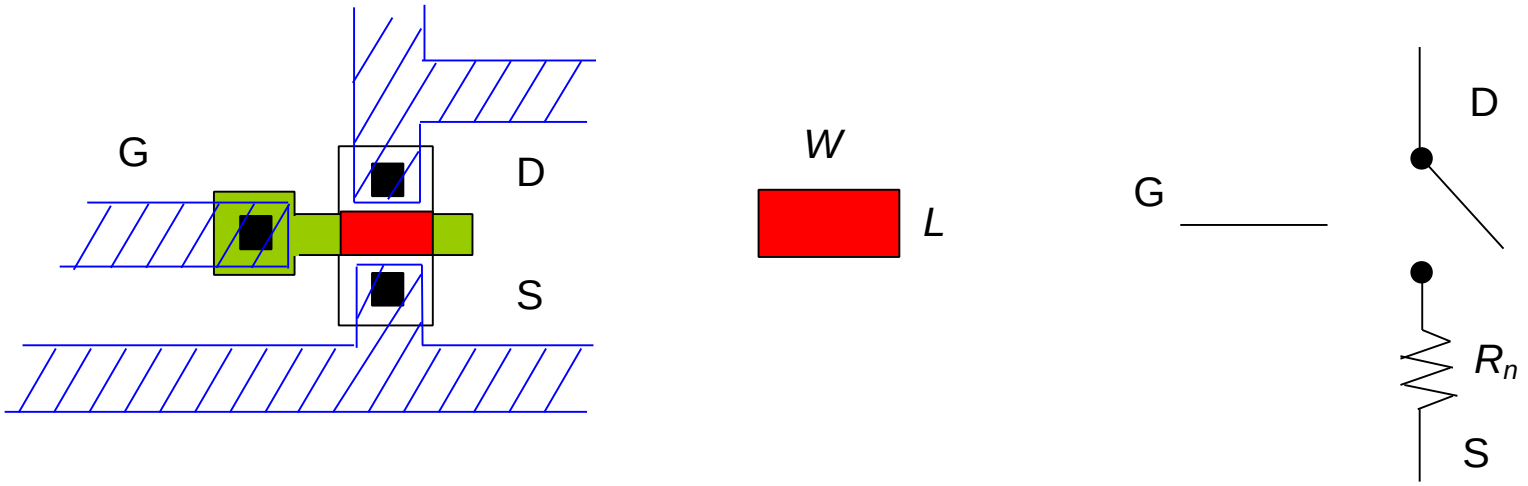
$$V_{tl} < V < V_{th}$$

NMOS remains in last state ("off" or "on")

NMOS Model Refinement #1

Closed NMOS transistor is not a perfect conductor

→ add an equivalent resistor R_n that reflects this phenomenon

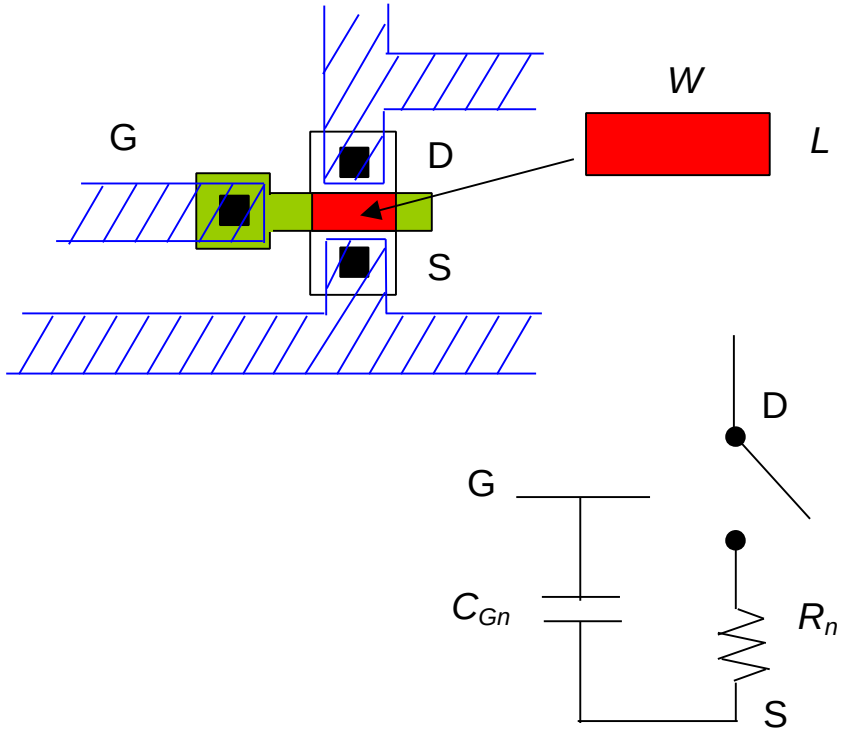


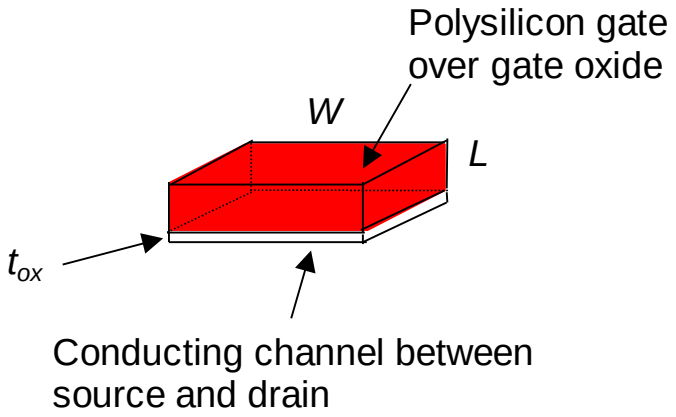
R_n* is inversely proportional to the channel width *W
Why?

NMOS Model Refinement #2

Input capacitance C_{Gn} (book uses C_n)

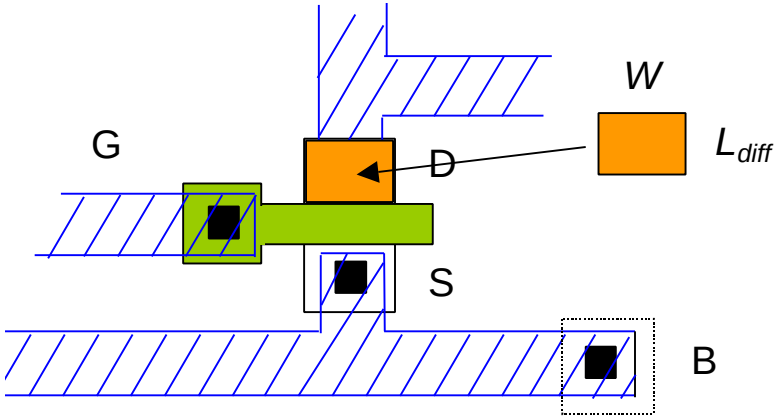
Gate has area W x L, gate oxide has thickness t_{ox}: $C_{Gn} = \varepsilon_{ox}[WL / t_{ox}]$



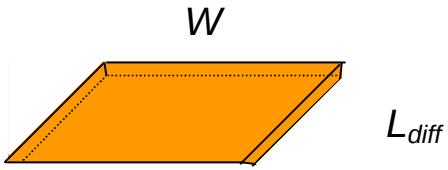


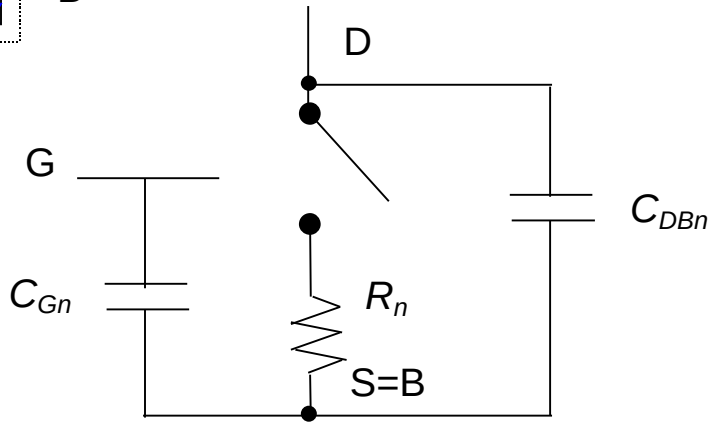
NMOS Model Refinement #3

Capacitance between drain and substrate: C_{DBn}



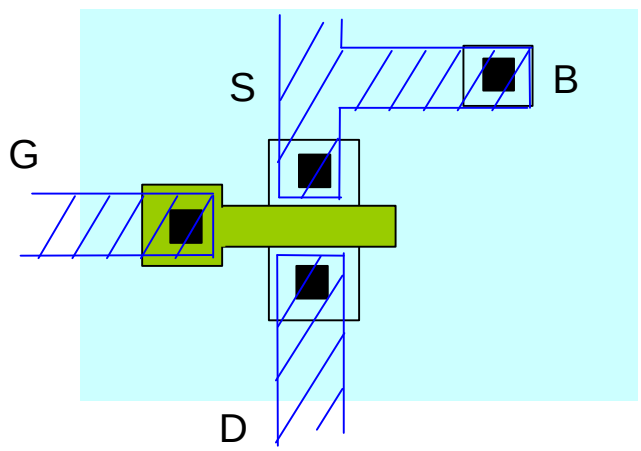
Junction capacitance between drain and bulk region (connected to source)

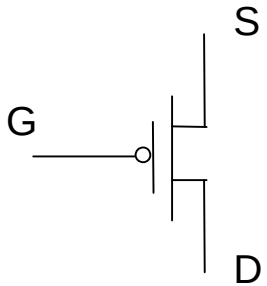


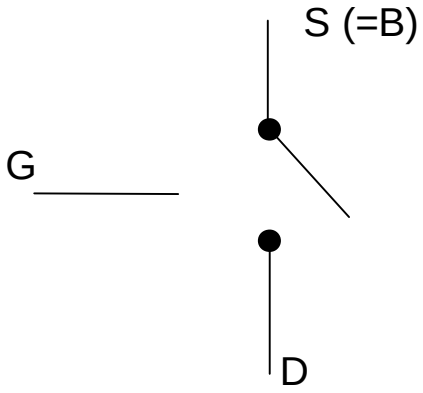


PMOS Transistor Switch Model

"Complementary" operation compared to NMOS







Switching thresholds for PMOS for "default" digital circuit connection

$V_S = V_B = V_{DD}$ = supply voltage (e.g., 3 V)

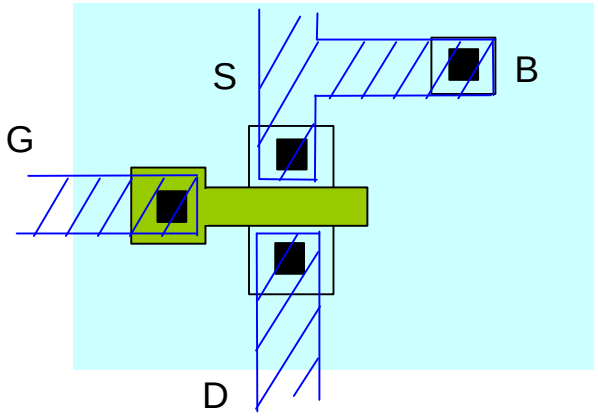
$V_G = = v_{in}$ (input voltage)

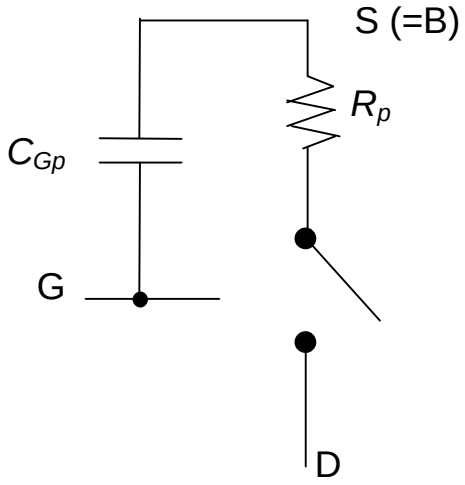
Switch is *closed* (Drain (D) is shorted to Source (S)) when $v_{in} < V_{Tl}$

Switch is *open* (Drain (D) is disconnected from Source (S)) when $v_{in} > V_{Th}$

PMOS Model Refinements #1 and #2

PMOS transistor has an equivalent resistance R_p when closed and we can add the gate capacitance between gate and source

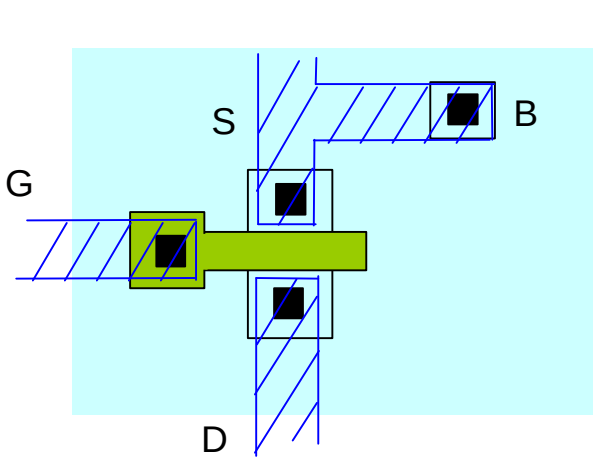


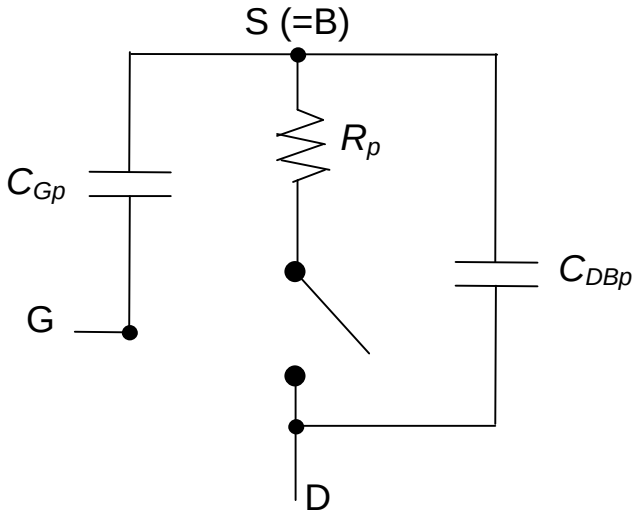


$C_{Gp} = \varepsilon_{ox}[WL / t_{ox}]$ … (*W* and *L* are for the PMOS)

PMOS Model Refinements #3

PMOS transistor has a depletion capacitance between the drain and the well (B contact … which is connected to the source)

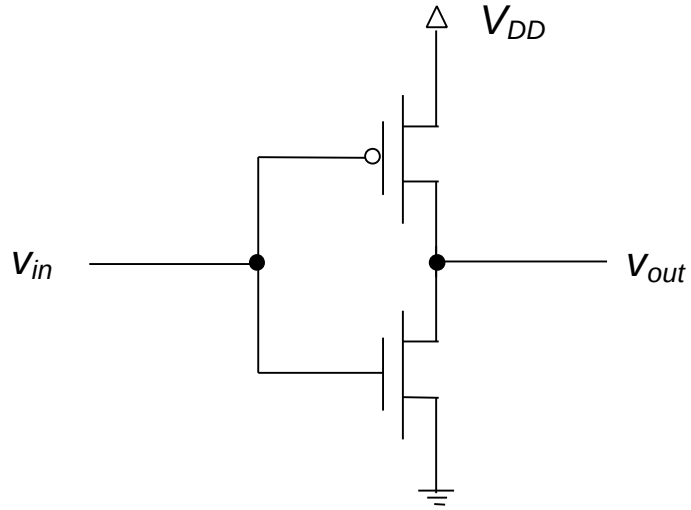


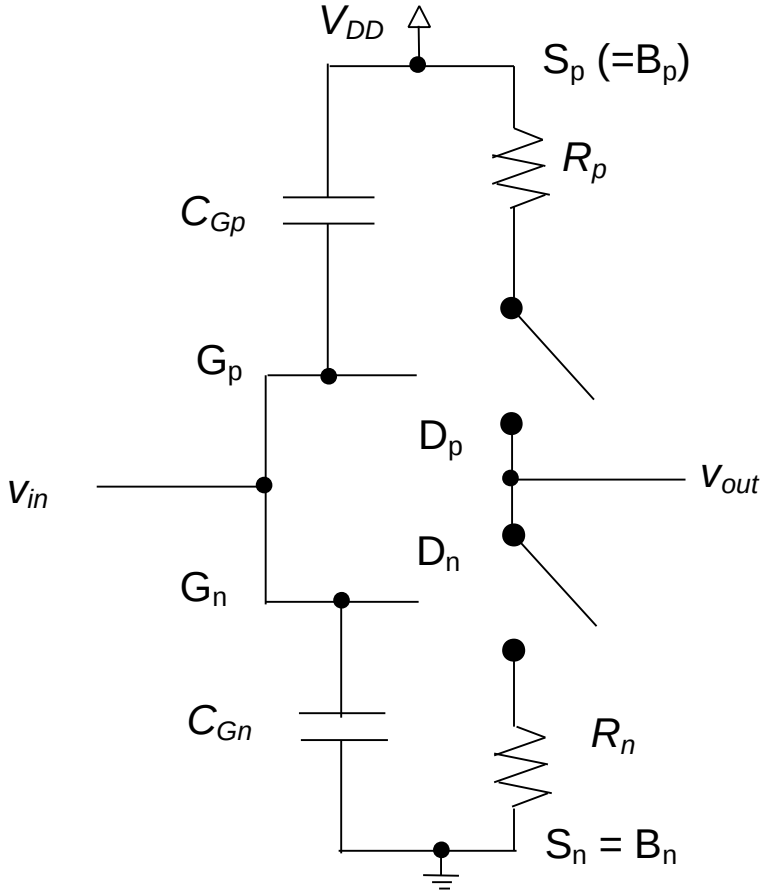


Put PMOS and NMOS transistors "in series" between supply and ground → performs inversion on input signal

The CMOS Inverter

Symbolic circuit





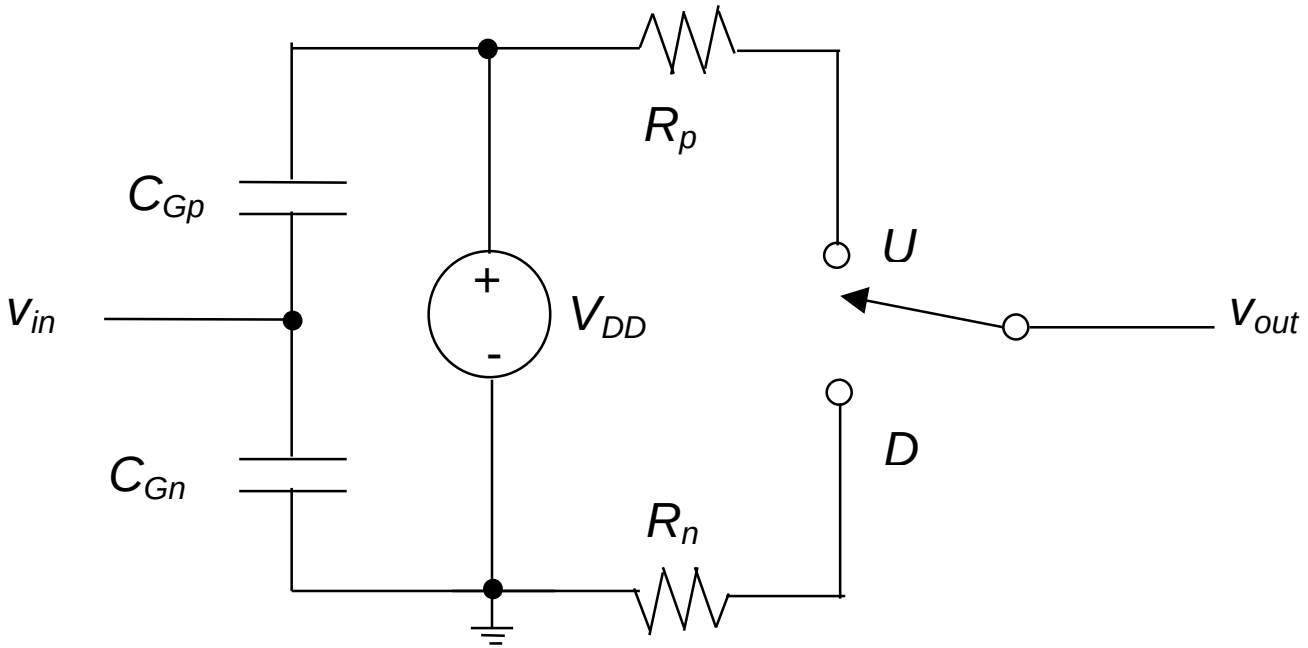
First Order CMOS Inverter Model

The switches are "ganged" (move together) since they have the same trip voltages

NMOS is closed when $v_{in} > V_{Th}$; PMOS is open

PMOS is closed when $v_{in} < V_{Tl}$; NMOS is open

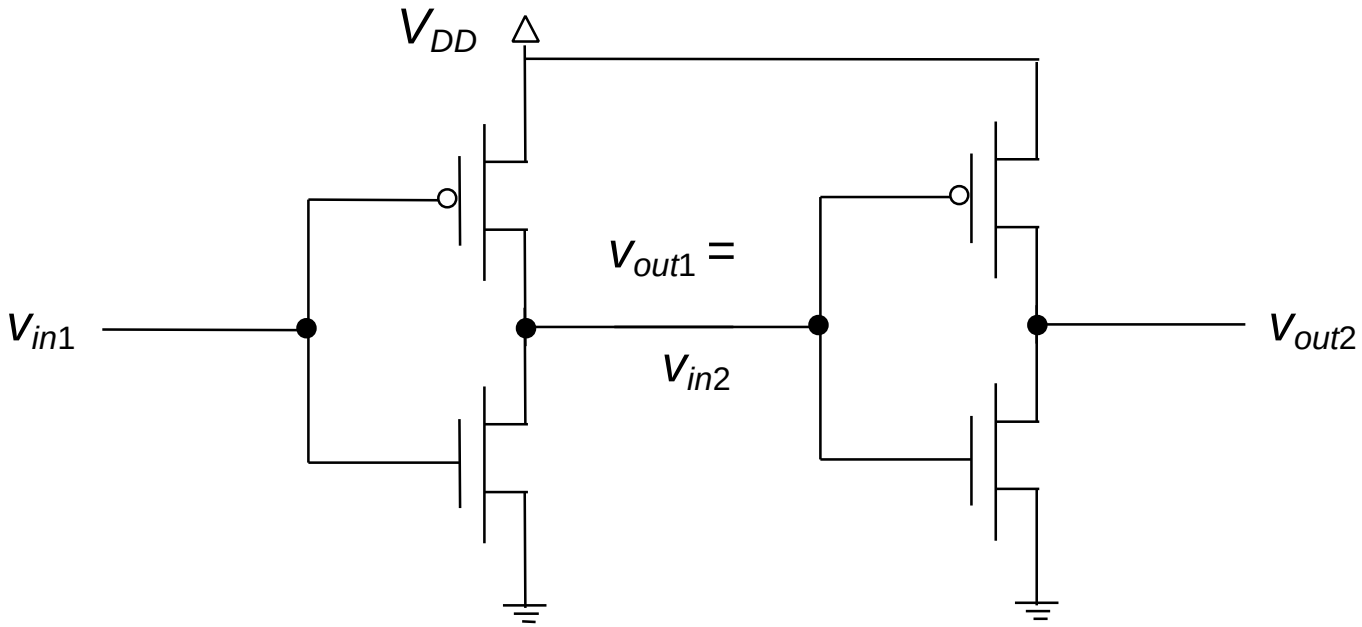
Reduce to a single switch (Fig. 2.10, R&R)



"Cascaded" CMOS Inverters

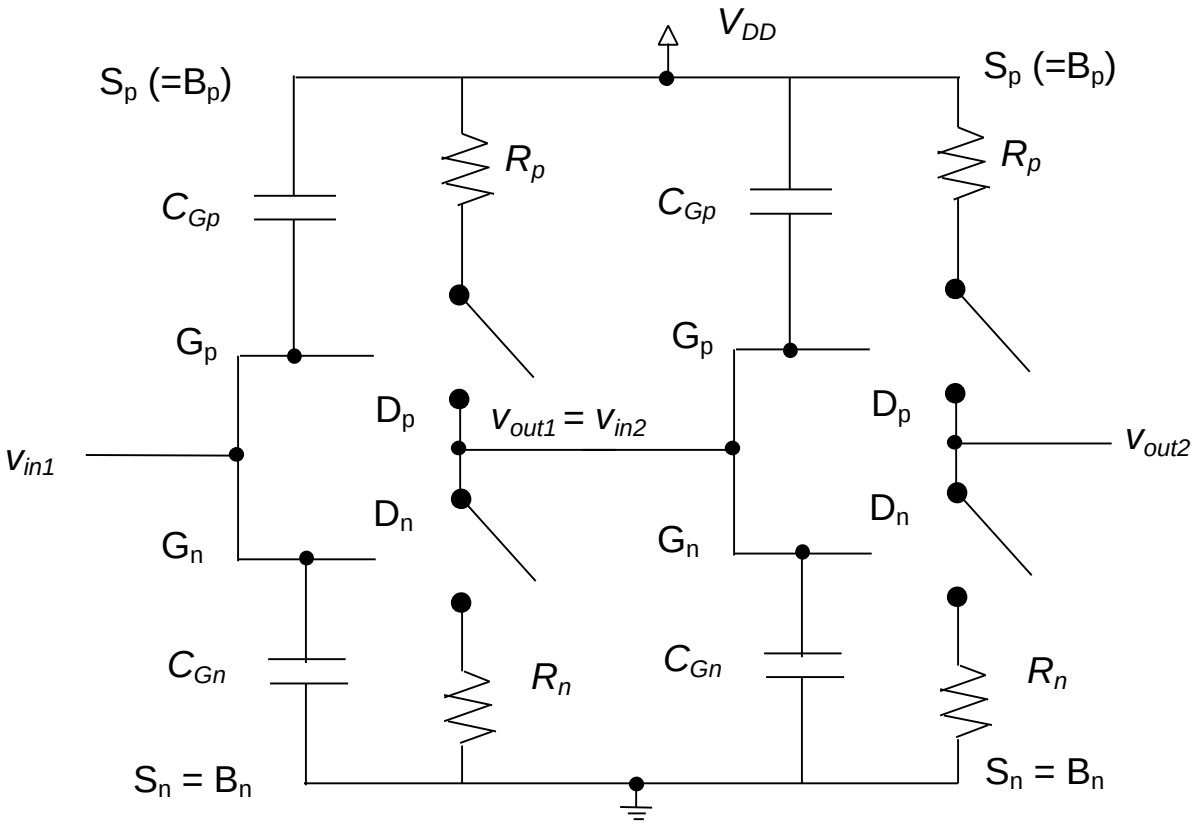
What's connected to the v_{out} node?

Representative "load" … possibly another CMOS inverter



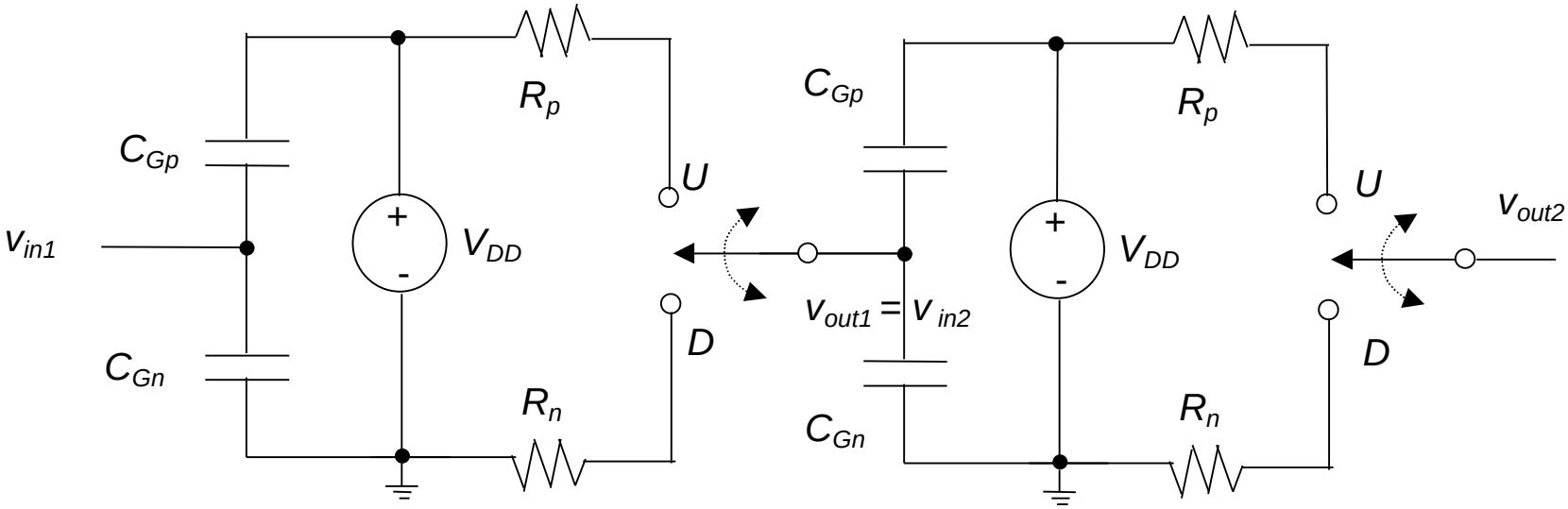
Cascaded Identical CMOS Inverter Circuit Model

Drain-bulk capacitances are omitted (at first), as is interconnect resistance and cap.



Simpler Representation

NMOS and PMOS transistors have the same logic thresholds, but operate in a complementary fashion → reduce to a single switch per inverter



Transitions of interest:

1. v_{in1} increases above V_{Th} : switch for inverter 1 moves to "D" position from previous "U" position

2. v_{in1} decreases below V_{Tl} : switch for inverter 1 moves to "U" position from previous "D" position