Problem 10. The circuit is not "complementary," PMOS transistors in series need to be in parallel in the NMOS bottom half. The $B$-input and $C$-input transistors do not satisfy this.

If $A = 0$, $B = V_{DD}$, and $C = V_{DD}$, using the switch model, we find $O = V_{DD}$.

F is connected to $V_{DD}$ + ground at the same time. Impossible, so circuit is not a logic circuit.
Problem 20

\[ V_{PD} + V_{THP} - \varepsilon \]

\[ \text{PMOS}_1 \]

\[ V_{PD} + V_{THP} - \varepsilon \]

\[ \text{PMOS}_2 \]

\[ V_{PD} + V_{THP} - \varepsilon \]

\[ \text{NMOS}_1 \]

\[ V_{PD} + V_{THP} - \varepsilon \]

\[ \text{NMOS}_2 \]

\[ V_{out} \]

\[ \varepsilon \]

**NMOS_1** **cutoff.**

For **PMOS_1**, \( V_{GSP_1} = V_{DD} + V_{THP} - \varepsilon - V_{PD} \)

\[ = V_{THP} - \varepsilon \]

So **PMOS_1** is barely turned on, \( I_{D_1} \) is small.

**PMOS_2** and **NMOS_2** have this same current.

**NMOS_2** has \( V_{GS N_2} = V_{PD} + V_{THP} - \varepsilon \)

Since \( V_{PD} \) much larger in magnitude than \( V_{THP} - \varepsilon \)
NMOS2 fully turned on. This combined with small $I_D$ means \textbf{NMOS2 triode} and $V_{DS_{N2}}$ small. This means $V_{OUT}$ is close to 0V.

This means the drain of PMOS2 is close to 0V. The gate of PMOS2 is at 0V. This means $V_{DSP2} \approx V_{GSP2}$.

This means $V_{DSP2} < V_{GSP2} - V_{THP}$ since subtracting $V_{THP}$ amounts to adding a positive number.

\textbf{PMOS2 saturation}. $V_{DSP2}$ must be small, because if it were large, then $V_{GSP2}$ would also be large and a large $I_{DP2}$ would result. $I_{DP2}$ must be small since PMOS1 was barely turned on.

This means $V_{DSP1}$ must be large in magnitude ($-V_{DSP1} - V_{DSP2} + V_{DS_{N2}}$ sum to $V_{DD}$) so \textbf{PMOS1 saturation}.
Problem 38: Since $V_{in}$ close to $V_m$, assume both transistors in saturation.

2 nonlinear transistor equations:

\[ I_{DN} = V_2 \left( \text{mA} / V^2 \right) (0.495 V - 1 V)^2 \left( 1 + 0.01 V^1 V_{DSN} \right) \]
\[ = 1.1175 \left( 1 + 0.01 V_{DSN} \right) \]
\[ I_{DP} = -V_2 \left( \text{mA} / V^2 \right) (-2.565 V - 1 V)^2 \left( 1 - 0.01 V^1 V_{DSP} \right) \]
\[ = -1.1325 \left( 1 - 0.01 V_{DSP} \right) \]

By KCL,

\[ I_{DN} + I_{DP} = 0 \Rightarrow I_{DN} = -I_{DP} \]

By KVL,

\[ -V_{PSN} + V_{DSP} + V_{DD} = 0 \Rightarrow V_{DSP} = V_{DSN} - V_{DD} = V_{PSN} - 5 V \]

Substitute into $I_{DN}$

\[ 1.1325 \left( 1 - 0.01 (V_{DSN} - 5 V) \right) = 1.175 \left( 1 + 0.01 V_{DSN} \right) \]

Solution: $V_{DSN} = 3.18 V$ ok for saturation

$V_{DSP} = -1.82 V$ also ok for saturation.

$V_{out} = 3.18 V$
Problem 4°: Let's find the $R$ that results in exactly 50 mA through the diode under "maximum current" conditions. $V_{IN} = 0$ results in the largest $V_{OUT}$, which results in the largest current through $R$. Look at

\[ V_{DD} = 5V \]

NMOS transistor cut off: ignore it from now on.

If $I_D = -50 \text{ mA}$, PMOS is in triode. Why? To be in saturation, PMOS $I_{DS}$ must be $I_{DSAT} = \sqrt{2} \cdot 100 \text{ mA}/\sqrt{2} (-5V - (-1V))^2 = -900 \text{ mA}$. So $I_{DS} = -50 \text{ mA} = 100 \text{ mA}/\sqrt{2}(-5V - (-1V - \frac{V_{DS}}{2})V_{DS}^2$

Solve: solutions $V_{DS} = \frac{3}{2} - 0.1277, -7.873$ \(\text{ incorrect} \)

So $V_{DSN} = 4.873 \text{ V}$

2 V goes over LED, so 2.873 V over resistor. $R = \frac{2.873 \text{ V}}{50 \text{ mA}} = 57.5 \Omega$ and any larger value works too.
Problem 5°

(a) Shortest pull-down when all NMOS transistors active; when \( A = B = C = D = V_{DD} \).

\[ R_{eq} = 2R_N \parallel 2R_N \]

all NMOS cutoff

\[ R_N = \frac{3}{4} \frac{V_{DD}}{I_{DSAT_N}} \]

\[ I_{DSAT_N} = \frac{1}{2} \frac{1 \text{um}}{0.5 \text{um}} \frac{50000 \text{ mm}^2}{V_S \mu \text{m}^2} \left( 5 \text{V} - -1 \text{V} \right)^2 = 4 \text{mA} \]

\[ R_N = \frac{3}{4} \cdot \frac{5 \text{V}}{4 \text{mA}} = 9.375 \Omega \]

\[ R_{eq} = 2R_N \parallel 2R_N = R_N = 937.5 \Omega \]

Inverter at output contributes 2 transistors, so

\[ C_{out} = 2 \times C_G + C_I \]

\[ C_G = (1 \text{um} \times 0.5 \text{um}) \frac{5 \text{fF}}{\mu \text{m}^2} = 2.5 \text{fF} \]

\[ C_I = (1 \text{um} \times 10 \text{um}) \frac{0.1 \text{fF}}{\mu \text{m}^2} = 1 \text{fF} \]

\[ C_{out} = 6 \text{fF} \]

\[ t_p = 0.69 \times R_{eq} \times C_{out} = 3.88 \text{ps} \]
b) Longest pull-down when 2 series NMOS are active (e.g., \( A = C = V_{DD}, B = D = 0 \)),

\[ R_{eq} = 2R_N = 1.875 \text{ k\Omega} \]

\[ C_{out} = 6 \text{ fF} \]

0.69 \times R_{eq} \times C_{out} = 7.76 \text{ ps} 

\[ R_p = -\frac{3}{4} \frac{V_{DD}}{I_{DSATp}} \]

\[ I_{DSATp} = -\frac{1}{2} \frac{1 \mu m}{0.5 \mu m} \frac{25000 \text{mm}^2}{Vs} \frac{5fF}{\mu m^2} \times (-5 \text{ V} - 1 \text{ V})^2 \]

\[ R_p = -\frac{3}{4} \frac{5V}{-2mA} = 1.875 \text{ k\Omega} \]

c) Shortest pull-up when all PMOS active (\( A = B = C = D = 0 \))

\[ R_p = -\frac{3}{4} \frac{V_{DD}}{I_{DSATp}} \]
\[ R_{eq} = 2R_p \parallel 2R_p = R_p = 1.875\, k\Omega \]

\[ t_p = 0.69\, \text{Cout} \quad R_{eq} = 7.76\, \text{ps} \]

\[ \text{still 6}\, \text{ftF} \]

d) Longest pull-up when 2 series PMOS active, e.g., \( A = B = 0, C = D = V_{DD} \)

\[ R_{eq} = 2R_p = 3.75\, k\Omega \]

\[ 0.69\, \text{Cout} \quad R_{eq} = 15.5\, \text{ps} \]

**Problem 6.** For one inverter:

Pull-down \( t_p = R_N \, \text{Cout} \cdot 0.69 \)

Pull-up \( t_p = R_p \, \text{Cout} \cdot 0.69 \)

We found \( R_N, R_p, \) and \( \text{Cout} \) contributed by inverter in Problem 5.
Pull-down $t_p = 0.69 \times 937.5 \times 6 \text{fF} = 3.88 \text{ps}$
Pull-up $t_p = 0.69 \times 1.875 \times 6 \text{fF} = 7.76 \text{ps}$

Worst-case $t_p$ is $7.76 \text{ps}$.

So the "dumb" way to find total propagation delay through 4 inverters is to take

$$t_p \text{ total} = 4 \times t_p \text{ worst-case individual} = 31 \text{ ps}$$

But since these are inverters, every pull-down is followed by a pull-up (if stage 1 output goes down, stage 2 goes up, stage 3 goes down, etc.)

so a better estimate would be

$$t_p \text{ total} = 2 \times t_p \text{ pull-up} + 2 \times t_p \text{ pull-down} = 23.3 \text{ ps}$$