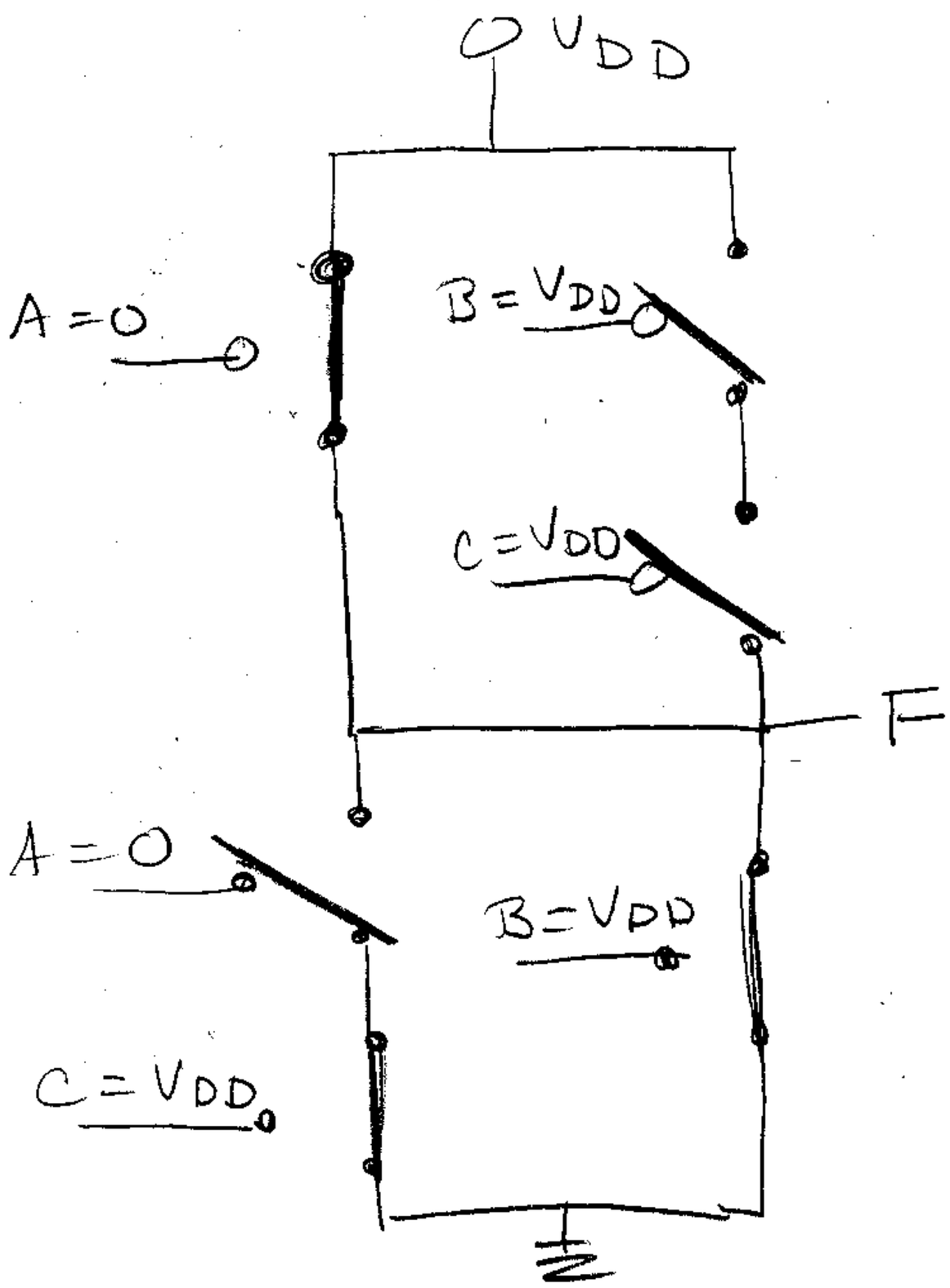
EE 40
Solutions
Midterm 3 Review

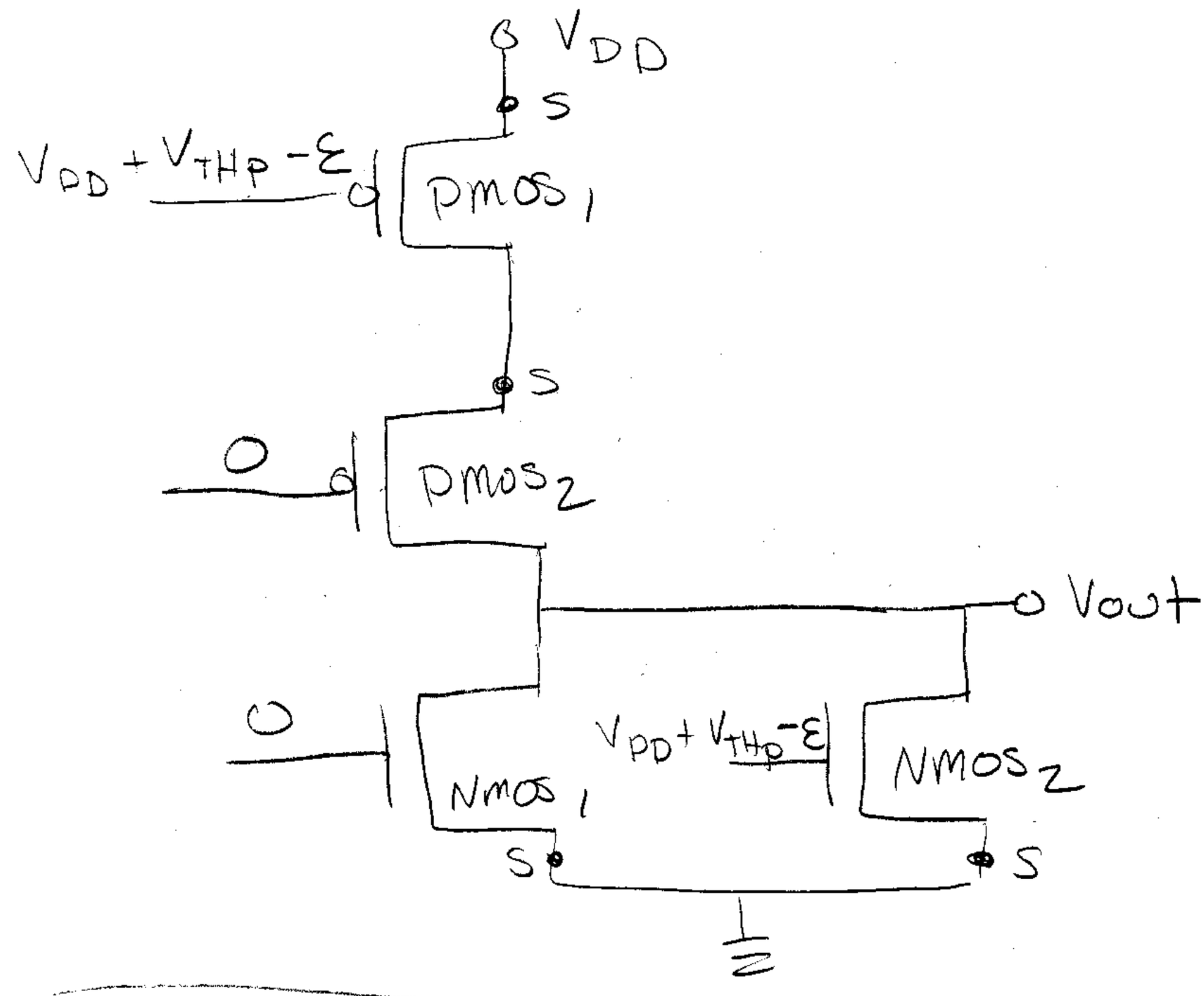
<u>Problem 1</u>: The circuit is not "complementary"; PMOS transistors in series need to be in parallel in the NMOS bottom half. The B-input + C-input transistors do not satisfy this.

If $A = 0$, $B = V_{DD}$ and $C = V_{DD}$, using the switch model, we find



F is connected to V_{DD} + ground at the same time, Impossible so circuit is <u>not</u> a logic circuit,

Problem 2:



NMOS1 cutoff.

For $PMOS_1$, $V_{GSP_1} = V_{DD} + V_{THp} - \varepsilon - V_{DD}$

$= V_{THp} - \varepsilon$

So $PMOS_1$ is barely turned on,

I_{DP_1} is small,

$PMOS_2$ and $NMOS_2$ have this same current.

$NMOS_2$ has $V_{GSN_2} = V_{DD} + V_{THp} - \varepsilon$

Since V_{DD} much larger in magnitude than $V_{THp} - \varepsilon$,

$NMOS_2$ fully turned on. This combined with small I_D means $NMOS_2$ triode and $V_{DS_{N_2}}$ small. This means V_{OUT} is close to 0 V.

This means the drain of $PMOS_2$ is close to 0 V. The gate of $PMOS_2$ is at 0 V. This means $V_{DSP_2} \approx V_{GSP_2}$.

This meass $V_{DSP_2} < V_{GSP_2} - V_{THP}$ since subtracting V_{THP} amounts to adding a positive number.

$PMOS_2$ saturation. V_{DSP_2} must be small, because if it were large, then V_{GSP_2} would also be large and a large I_{DP_2} would result – I_{DP_2} must be small since $PMOS_1$ was barely turned on.

This means V_{DSP_1} must be large in magnitude ($-V_{DSP_1} - V_{DSP_2} + V_{DSN_2}$ sum to V_{DD}) so $PMOS_1$ saturation.

Problem 3: Since V_{IN} close to V_M, assume both transistors in saturation.

2 nonlinear transistor equations:

$$I_{DN} = \tfrac{1}{2}(1\,mA/V^2)(2.495V - 1V)^2(1 + 0.01V^{-1}V_{DSN})$$
$$= 1.1175(1 + 0.01V_{DSN})$$

$$I_{DP} = -\tfrac{1}{2}(1mA/V^2)(-2.505V - 1V)^2(1 - 0.01V^{-1}V_{DSP})$$
$$= -1.1325(1 - 0.01V_{DSP})$$

By KCL,

$$I_{DN} + I_{DP} = 0 \Rightarrow I_{DN} = -I_{DP}$$

By KVL,

$$-V_{DSN} + V_{DSP} + V_{DD} = 0 \Rightarrow V_{DSP} = V_{DSN} - V_{DD}$$
$$= V_{DSN} - 5V$$

Substitute into I_{DN}

$$1.1325(1 - 0.01(V_{DSN} - 5V)) = 1.175(1 + 0.01V_{DSN})$$

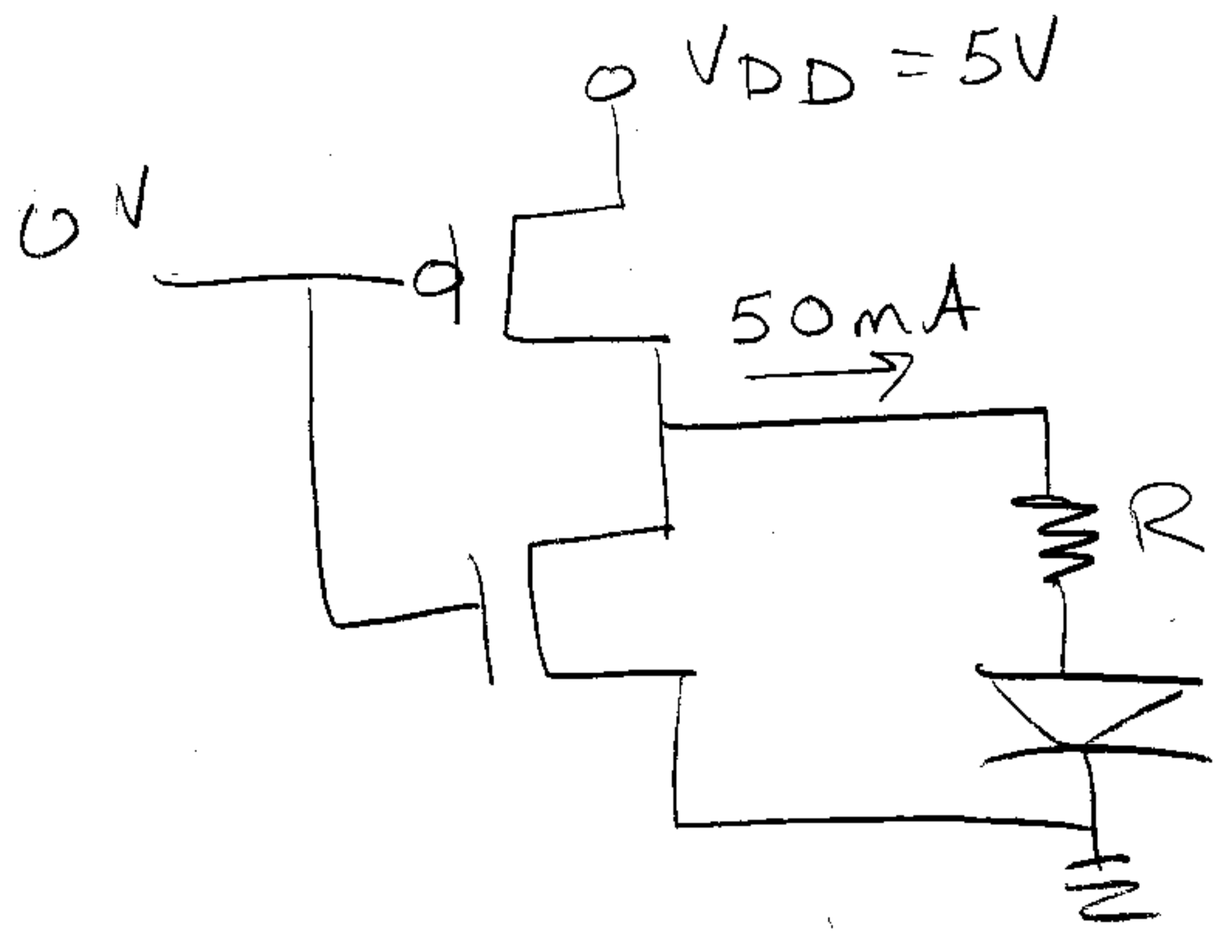
Solution: $V_{DSN} = 3.18V$ ok for saturation

$V_{DSP} = -1.82V$ also ok for saturation.

$V_{out} = 3.18V$

Problem 4: Let's find the R that results in exactly 50 mA through the diode under "maximum current" conditions. $V_{IN} = 0$ results in the largest V_{OUT}, which results in the largest current through R.

Look at



NMOS transistor cutoff: ignore it from now on.

If $I_D = -50$ mA, PMOS is in triode.

Why? To be in saturation, PMOS I_{Dp} must be $I_{DSATP} = -\frac{1}{2} \cdot 100\,mA/V^2 (-5V - -1V)^2 = -800$ mA.

So $I_{Dp} = -50\,mA = -100\,mA/V^2 \left(-5V - -1V - \frac{V_{DSP}}{2}\right) V_{DSP}$

Solve: solutions $V_{DSP} = \{-0.127, -7.873\}$

correct impossible

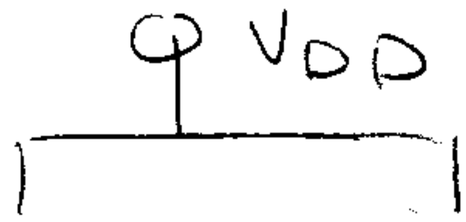
So $V_{DSN} = 4.873$ V

2 V goes over LED, so 2.873 V over resistor.

$R = \frac{2.873\,V}{50\,mA} = 57.5\,\Omega$ and any larger value works too.

Problem 5:

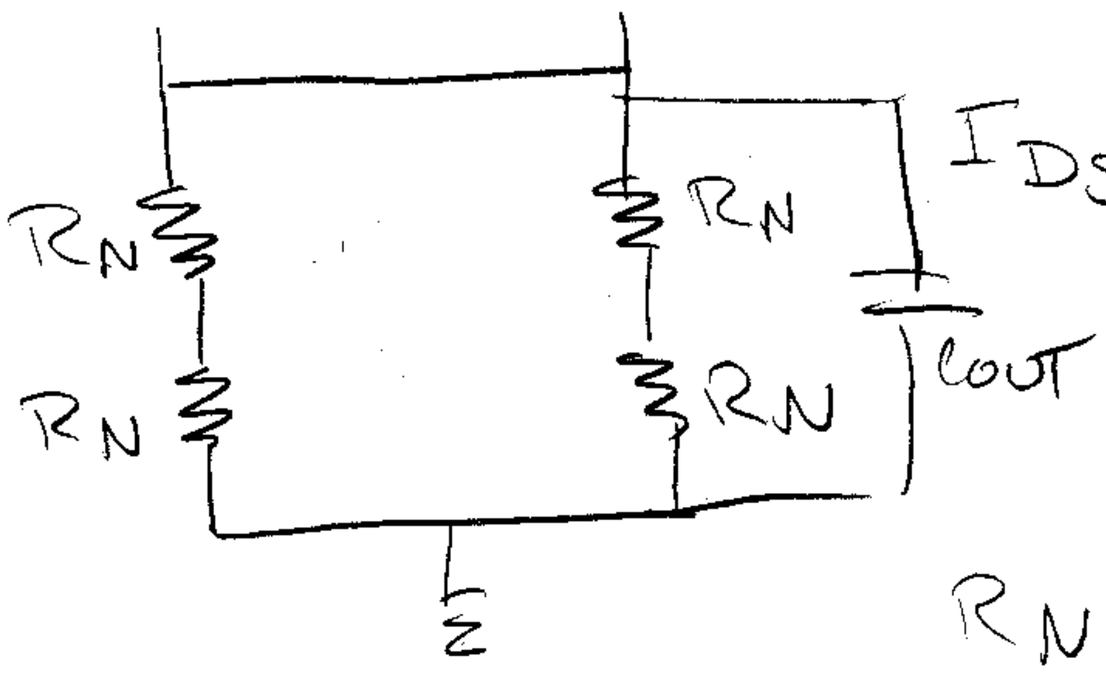
a) Shortest poll-down when all NMOS transistors active; when $A = B = C = D = V_{DD}$.



$$R_{eq} = 2R_N \parallel 2R_N$$

all PMOS cutoff

$$R_N = 3/4 \, \frac{V_{DD}}{I_{DSAT\,N}}$$



$$I_{DSAT_N} = \frac{1}{2} \frac{1\mu m}{0.5\mu m} \, 50000 \frac{mA^2}{V^2} \, 5 \frac{fF}{\mu m^2} \cdot (5V - 1V)^2$$

$$= 4mA$$

$$R_N = 3/4 \cdot \frac{5V}{4mA} = 937.5\,\Omega$$

$$R_{eq} = 2R_N \parallel 2R_N = R_N = 937.5\,\Omega$$

Inverter at output contributes 2 transistor gates

$$C_{OUT} = 2C_G + C_I$$

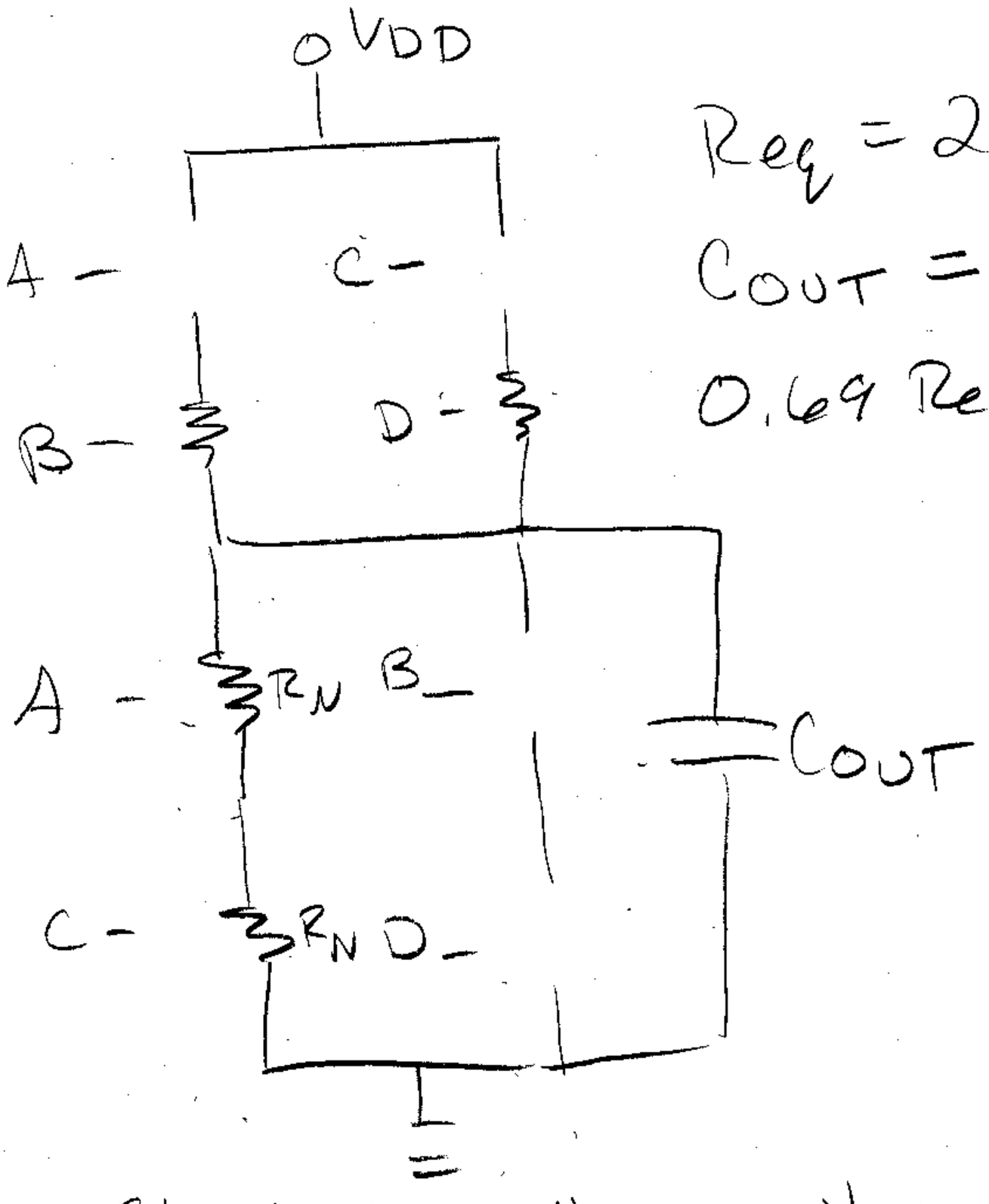
$$C_G = (1\mu m \cdot 0.5\mu m) \frac{5fF}{\mu m^2} = 2.5\,fF$$

$$C_I = (1\mu m \cdot 10\mu m) \frac{0.1\,fF}{\mu m^2} = 1\,fF$$

$$C_{out} = 6\,fF$$

$$t_p = 0.69\, R_{eq}\, C_{OUT} = 3.88\,ps$$

b) Longest pull-down when 2 series NMOS are active (e.g., $A = C = V_{DD}$, $B = D = 0$).

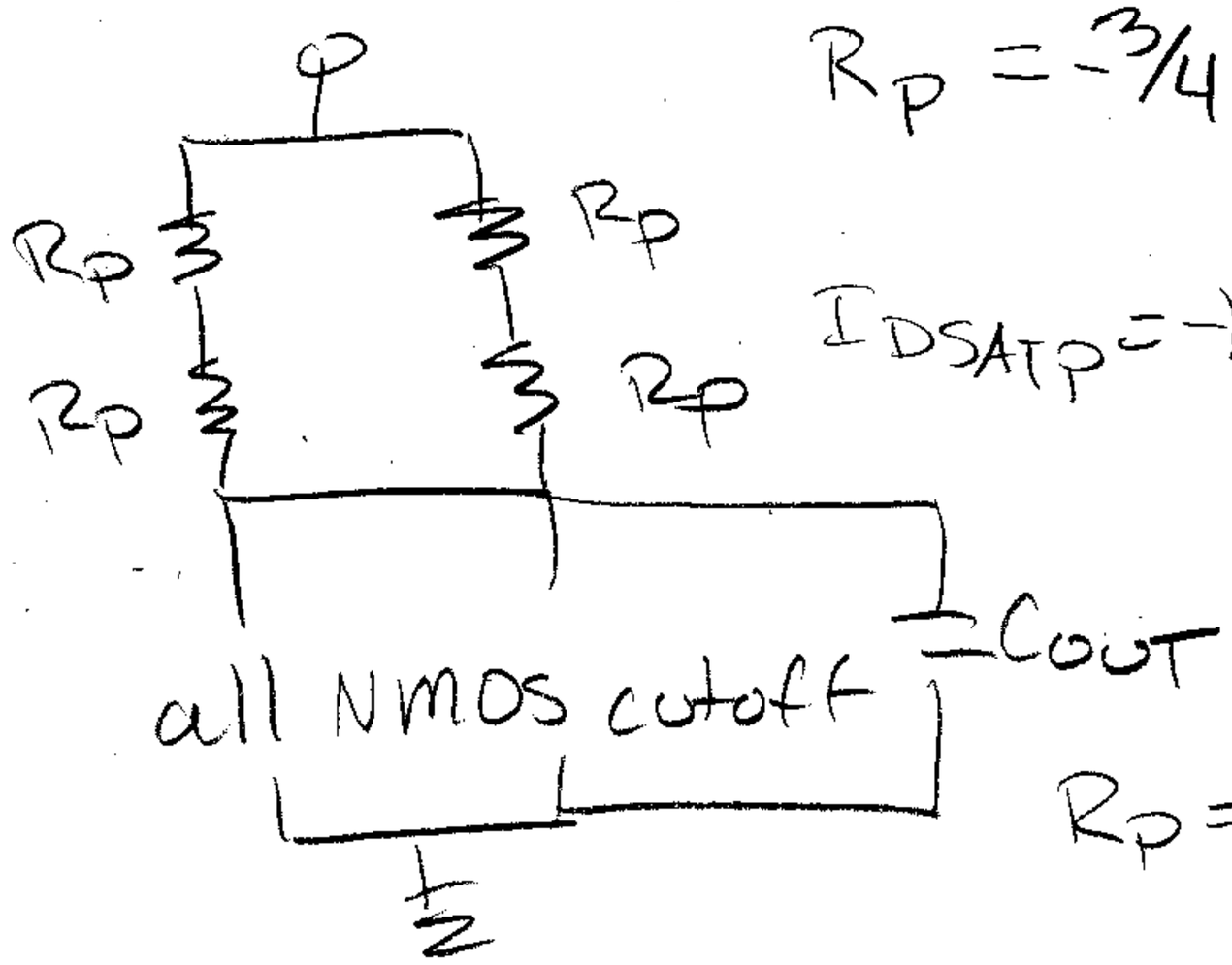


$R_{eq} = 2R_N = 1.875\ k\Omega$

$C_{OUT} = 6\ fF$

$0.69\ R_{eq} C_{OUT} = 7.76\ ps$

c) Shortest pull-up when all PMOS active ($A = B = C = D = 0$)



$$R_p = -\frac{3}{4}\frac{V_{DD}}{I_{DSAT_p}}$$

$$I_{DSAT_p} = -\frac{1}{2}\frac{1\mu m}{0.5\mu m}\ 25000\frac{mm^2}{Vs}\ \frac{5fF}{\mu m^2}\ (-5V - -1V)^2$$

$$= -2mA$$

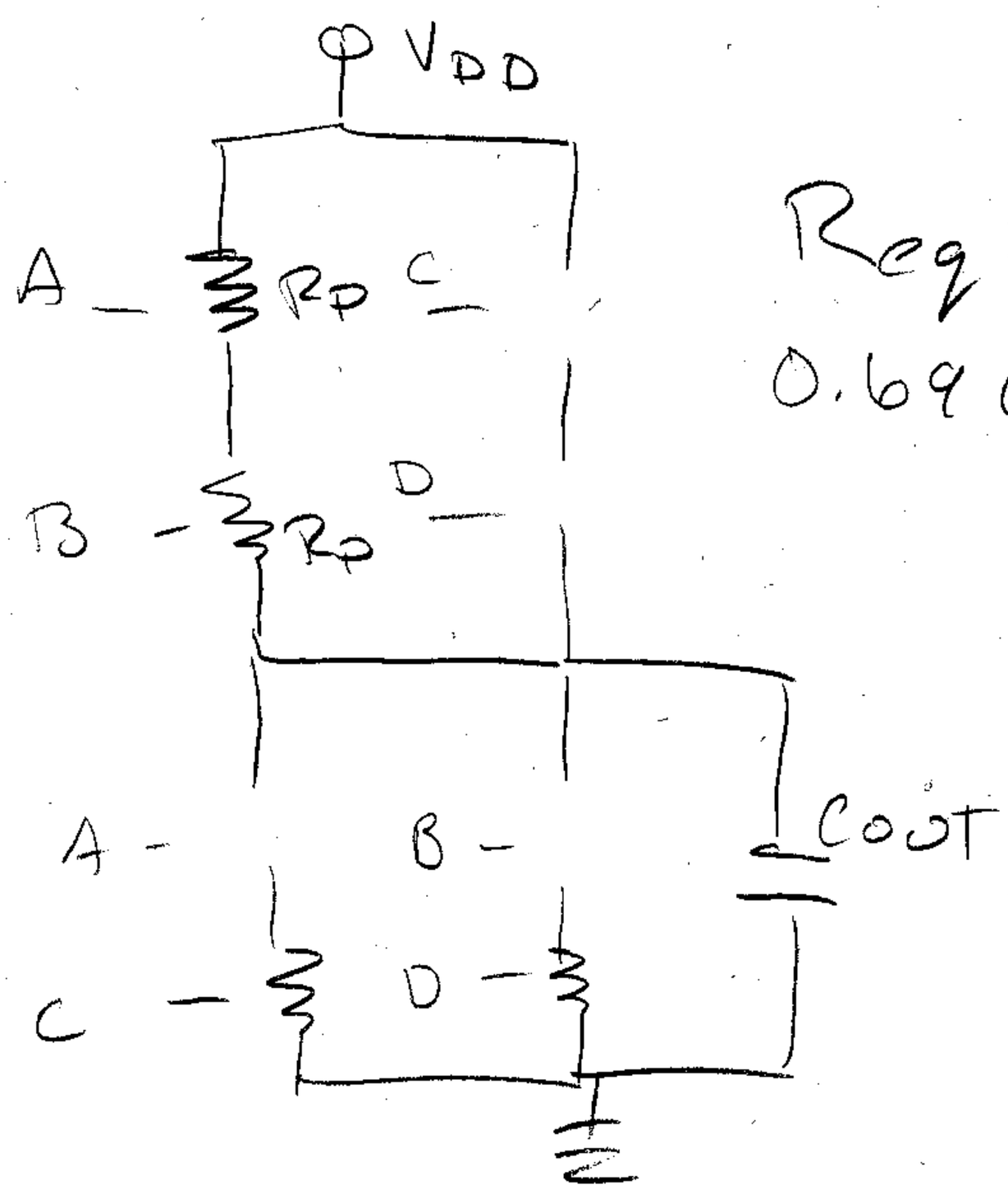
$$R_p = -\frac{3}{4}\frac{5V}{-2mA} = 1.875\ k\Omega$$

$R_{eq} = 2R_p \parallel 2R_p = R_p = 1.875\,k\Omega$

$t_p = 0.69\, C_{OUT} R_{eq} = 7.76\,ps$

still 6 fF

d) Longest pull-up when 2 series PMOS active, e.g. $A = B = 0$, $C = D = V_{DD}$



$R_{eq} = 2R_p = 3.75\,k\Omega$

$0.69\, C_{out} R_{eq} = 15.5\,ps$

<u>Problem 6</u>: For one inverter,

pull-down $t_p = R_N C_{OUT} \cdot 0.69$

pull-up $t_p = R_p C_{out} \cdot 0.69$

We found R_N, R_p, and C_{out} contributed by inverter in Problem 5.

pull-down $t_p = 0.69 \cdot 937.5 \cdot 6fF = 3.88\,ps$

pull-up $t_p = 0.69 \cdot 1.875K \cdot 6fF = 7.76\,ps$

Worst-case t_p is 7.76 ps.

So the "dumb" way to find total propagation delay through 4 inverters is to take

$$t_{p_{total}} = 4\, t_{p_{\substack{\text{worst-case}\\ \text{individual}}}} = 31\,ps$$

But since these are inverters, every pull-down is followed by a pull-up (if stage 1 output goes down, stage 2 goes up, stage 3 goes down, etc)

so a better estimate would be

$$t_{p_{total}} = 2\, t_{p_{pull\text{-}up}} + 2\, t_{p_{pull\text{-}down}}$$

$$= 23.3\,ps$$