UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Spring 2004**

Homework Assignment #10
Due 2pm in 240 Cory on Friday, April 9.
Be sure to put your **Discussion Section** on your paper.

Problem 1: Inverter Circuits and Noise Margins

a) Describe qualitatively how an NMOS inverter circuit works. Explain how relatively large noise margins $\boldsymbol{NM_H}$ and $\boldsymbol{NM_L}$ can be achieved. (Refer to Slides 2 and 6 of Lecture 18 for the definitions of $\boldsymbol{NM_H}$ and $\boldsymbol{NM_L}$).

b) Describe qualitatively how a CMOS inverter works. What are its advantages with respect to noise margins, power consumption, and size, as compared with the NMOS inverter?

Problem 2: CMOS Logic Gates

(Read: pp. 237-241 of Section 6.2.1, Rabaey *et al.*)

A static CMOS logic gate is a combination of two networks: a *pull-up network* of PMOS transistors, and a *pull-down network* of NMOS transistors. The pull-up network provides a connection between the output and the power-supply V_{DD} anytime the output of the logic gate is meant to be **1** (based on the inputs). The pull-down network provides a connection between the output and *GND* anytime the output of the logic gate is meant to be **0** (based on the inputs). Remember that NMOS devices are turned on with a high (logic **1**) input voltage, whereas PMOS devices are turned on with a low (logic **0**) input voltage, and that transistors connected in series correspond to an AND function, whereas transistors connected in parallel correspond to an OR function. (Refer to Slides 5 & 6 of Lecture 19.)

Design a complex CMOS logic gate to implement the function $\mathbf{F} = \overline{(\mathbf{A} + \mathbf{B} \cdot \mathbf{C})}$.

Problem 3: Combinatorial Logic Circuits. Hambley problem 7.19 (a and c only). In each case, draw a logic circuit implementing the given Boolean expression using AND, OR, and NOT gates.

Problem 4: Combinatorial Logic Circuits. Hambley problem 7.20 (a and b only)

Problem 5: Logic Circuit Synthesis. Hambley problem 7.34. Write the expression only using the sum-of-products method. Simplify this expression if possible using a Karnaugh map. Draw a logic circuit using only NAND gates.