UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Spring 2004**

Homework Assignment #11
Due 2pm in 240 Cory on Friday, 4/23/04
Be sure to put your **Discussion Section** on your paper.

Problem 1: Sequential Logic Circuits: a) Hambley 7.56; b) Hambley 7.57.

Problem 2: Propagation Delay and Timing Diagram

a) How would you size the NMOS and PMOS transistors in a 3-input NAND gate to achieve comparable worst-case pull-up and pull-down delays? (In other words, indicate the $(W/L)_{PMOS}$ to $(W/L)_{NMOS}$ ratio so that t_{pLH} and t_{pHL} are equal.) Assume that the W/L ratio for a PMOS transistor must be 3× larger than for an NMOS transistor, in order to achieve comparable equivalent resistance in the on state.) Note that the worst-case pull-up delay occurs when only one PMOS transistor is switched on.

b) Consider the fanout = 1 inverter of Example 5.4 (and Example 5.5) from Rabaey *et al.*, discussed in Lecture 22. Estimate the propagation delays t_{pLH} and t_{pHL} if the driving inverter is instead connected to 4 inverters (*i.e.* fanout = 4). You can assume that each of the extrinsic capacitance components of the driving inverter output capacitance increases by a factor of 4, while the intrinsic capacitance components are unchanged, for this case. The values of R_n and R_p for W/L = 1 are 13 kΩ and 31 kΩ, respectively. As noted in class, the W/L ratios for the NMOS and PMOS transistors in the inverters are not equal to 1. Thus, you'll need to calculate the actual equivalent resistance values in order to determine the propagation delays.

c) Assume each NAND gate in the logic circuit below has propagation delay t_p = 50 ps. Note that the logic input signals **A**, **B**, and **C** each change from **0** to **1** at time t = 50 ps. Draw the timing diagrams for the logic signals **D**, **E**, **F**, and **G**, for times in the range t = 0 to t = 250 ps.