UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 Spring 2004

Homework Assignment #12
Due 2pm in 240 Cory on Wed, 5/5/04.
Be sure to put your Discussion Section on your paper.

Problem 1: MOS Capacitor Fabrication Process (using SIMPLer)
(SIMPLer is accessed online at http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.html . See the help file for useful information on how to use it. Note that the smallest square that you can draw is 0.5 μm on a side.)

Create a fabrication process and mask set using SIMPLer for a simple metal-oxide-semiconductor (MOS) capacitor structure which uses metal (aluminum) for the upper electrode and doped Si as the lower electrode:

1. Start with an n-type wafer.
2. Grow 500 nm of silicon dioxide (SiO_2).
3. Pattern the oxide:
    a. Deposit photoresist
    b. Pattern the photoresist so that it covers the wafer **except** in a square region 10 μm × 10 μm.
    c. Etch away the oxide in the 10 μm × 10 μm square region, using an etchant that does not attack either the photoresist or silicon. (In SIMPLer, use a "pattern oxide" step.)
    d. Strip the photoresist
4. Implant phosphorus donor atoms (dose = 10^{14} cm^{-2}); anneal to a depth of 250 nm.
5. Grow 50 nm silicon dioxide.
6. Deposit a 1 μm thick aluminum layer.
7. Pattern the metal:
    a. Deposit photoresist
    b. Pattern the photoresist so that only a region 12 μm × 12 μm square remains, centered over the region of thin oxide.
    c. Etch away the metal outside the 12 μm × 12 μm region, using an etchant that does not attack either the photoresist or oxide.
    d. Strip the photoresist.

Turn in a printout of the capacitor layout and cross section after each step (1 through 7) of the fabrication process. Alternatively (*e.g.* if you cannot figure out how to print out the figures with a white background), you can simply provide accurate (to scale) hand-drawn sketches.

Problem 2: CMOS Inverter Layout
Consider the CMOS inverter example in SIMPLer:
Note that the substrate is lightly doped p-type, and that an n-well region is used for the PMOSFET (the upper transistor in the layout). There are 2 problems with this example:

1. It neglects to provide body contacts for the NMOSFET and PMOSFET.
2. The relative sizes of the transistors are not realistic. ($(W/L)_{PMOS}$ / $(W/L)_{NMOS}$ should be >1)

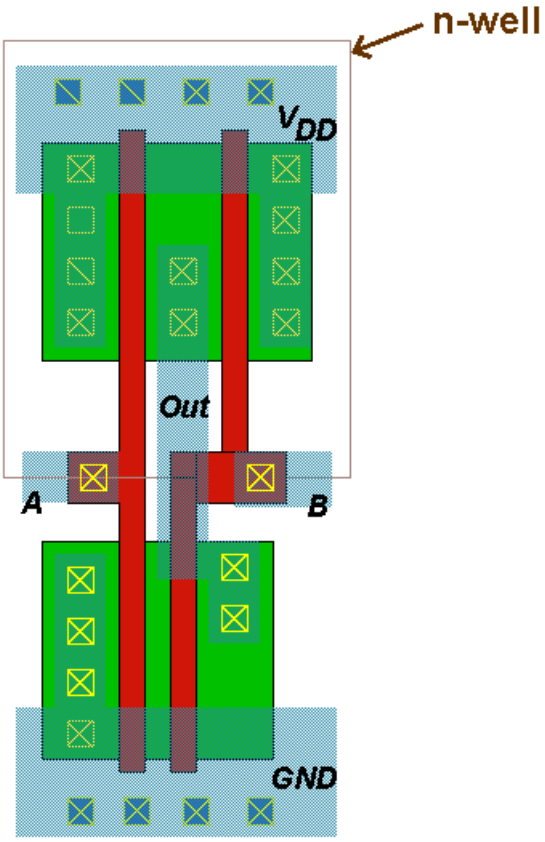
Modify the mask set in order to correct these problems:

- Enlarge the size of the n-well (oxide mask in Step 2) in order to make room for an n-well contact.
- Modify the "active area" mask in Step 6 so that openings are provided for body contacts, and also so that the MOSFET channel widths are sized appropriately to achieve $t_{pHL} \cong t_{pLH}$. (Assume that the minimum feature size is 1 μm (2 grid spacings), so that you cannot reduce the MOSFET channel length.)
- Modify the "select mask" used in Steps 11 & 14 to allow for the body contact regions to be doped.
- Modify the contact and metal masks in Steps 17 & 19 to make sure that the n-well and p-type substrate are properly biased (to V_{DD} or GND). Note also that you will need to make modifications to these masks because the "active area" mask was modified.

Turn in a printout or hand-drawn sketches of the modified CMOS inverter layout and cross section (showing a cut through the body, source and drain contacts for the PMOSFET and NMOSFET, as in the original example) of the final structure. On the layout, label the transistors ("PMOS" and "NMOS") and metal lines (Input, Output, V_{DD}, and GND). On the cross-section, label the various layers (n-type Si, p-type Si, oxide, poly-Si, metal).

Problem 3: Circuit Extraction from Layout

Draw the circuit diagram corresponding to the layout below. The substrate is p-type. (Brown = n-well mask; Green = active mask; Red = gate mask; Blue = metal mask)



Problem 4: IC Fabrication Technology Advancement

The number of square dice ("chips") per wafer can be estimated to be $N = \pi (R - S)^2 / S^2$, where R is the radius of the wafer and S is the length of one side of the dice. Suppose that the cost of processing a single 200mm-diameter wafer in a particular process (0.18 μm minimum feature size) is $2000, and that 90% of the dice fabricated are good (*i.e.* "yield" is 90%).

- **a)** Determine the processing cost per good die, for a die size of 0.5 cm.
- **b)** By scaling the technology from 0.18 μm minimum feature size to 0.13 μm minimum feature size, the chip size can be proportionately reduced. However, the yield goes down to 70%. Determine the cost per good die for the scaled technology.
- **c)** Suppose the cost of processing a 300mm-diameter wafer in the 0.13 μm process is $3,000. What is the minimum yield required in order to make it worthwhile to run 300mm-diameter wafers instead of 200mm-diameter wafers?