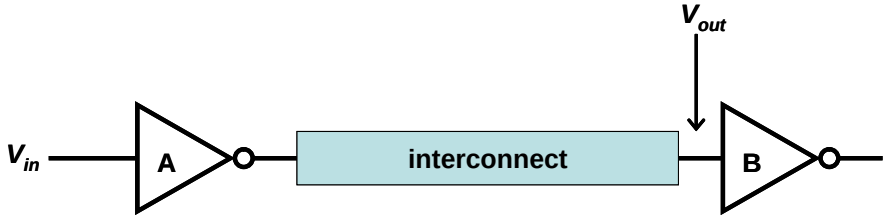
UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 Spring 2004

Homework Assignment #13
Not to be handed in. Be sure to complete to prepare for the final.
Solutions will be posted week of May 10.

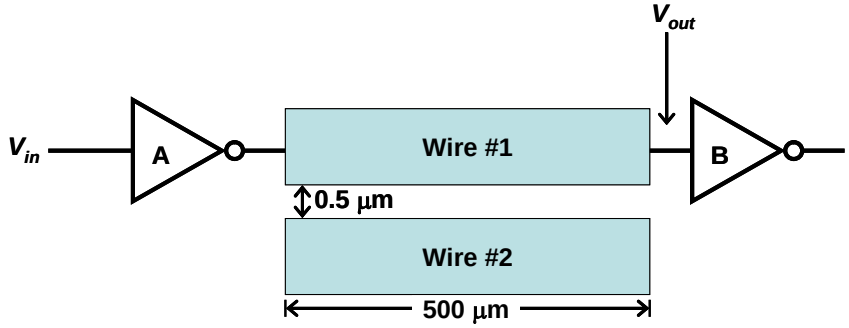
Problem 1: Interconnect Delay
Consider the cascaded CMOS inverters below:



We are interested in the propagation delay of Inverter A (between V_{in} and V_{out}). The equivalent on-resistance R_{dr} of the NMOSFET or PMOSFET in Inverter A is 10 kΩ. The intrinsic capacitance $C_{intrinsic}$ (due to the drain pn-junction capacitances and gate-overlap capacitances for Inverter A) is 3 fF; the fanout capacitance C_{fanout} (input capacitance of Inverter B, *i.e.* the MOSFET gate capacitances for Inverter B) is 3 fF.

Suppose the oxide (SiO_2, with dielectric permittivity $\varepsilon_{SiO2} = 3.45\times10^{-13}$ F/cm) between the aluminum (resistivity = 2.7 μΩ-cm) metal layer and the silicon substrate is 1 μm thick (*i.e.* t_{di} = 1 μm). If the aluminum interconnect thickness H is 0.5 μm and its width W is 1 μm, how long must it be in order for the interconnect delay ($(0.69R_{dr} + 0.38R_{wire})C_{wire}$) to account for half of the propagation delay for Inverter A? (Use the equation on Slide 8 of Lecture 26 for the interconnect capacitance, and the last equation on Slide 13 of Lecture 26 for the propagation delay.)

Problem 2: Coupling Capacitance



The figure above shows Inverter A driving Inverter B. Wire #1, connecting the output of Inverter A to the input of Inverter B, is close to Wire #2. Let's examine how the capacitive coupling between Wire #1 and Wire #2 can affect the propagation delay for Inverter A. Assume that the CMOS technology and inverter design are the same as in Problem 1. Each of the aluminum wires is 0.5 μm thick and 2 μm wide, and they are spaced 0.5 μm apart. **For this problem, you can assume the fringing-field capacitance of the wires is negligible.**

a) Calculate the resistance of Wire# 1 and verify that it is small compared to R_{dr} of Inverter A.
b) A Stanford engineering student treats Wire# 2 as a floating line. What RC time constant does s/he get? (Use the equation in Slide 20 of Lecture 26.)
c) You decide to make a more conservative estimate of the delay by treating Wire #2 as a grounded line. What RC time constant do you get? (Use the equation in Slide 19 of Lecture 26.)

Problem 3: Ring Oscillator Analysis

a) You have an 11 stage ring oscillator. Each inverter in the ring has the following parameters: R_n = 4 k ohm, R_p = 5 k ohm, C_n = 6 fF, C_p= 12 fF, V_{DD} = 2.5 V, V_{iL} = 0.9 V, V_{iH} = 1.6 V. Determine the frequency and period of this ring oscillator. Only consider the gate capacitances listed here, neglect other capacitances.

b) One of the inverters in the ring oscillator of part (a) is replaced with an inverter that is 10 times larger, i.e. it has 10 times the gate capacitance and 1/10 driving resistance. Find the frequency and period of this modified ring oscillator.