UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Spring 2004**

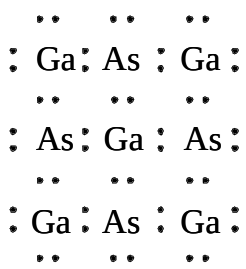
Homework Assignment #7
Issued: Mar. 4, 2004, Due: 2pm in 240 Cory on Friday, Mar. 12, 2004.
Be sure to put your **Discussion Section number** on your paper.

Problem 1: Semiconductor Fundamentals

a) How do mobile electrons and holes come into existence in a pure (undoped) semiconductor? Explain qualitatively how the resistivity of an intrinsic (undoped) semiconductor should change as a function of temperature. (Assume that the electron and hole mobilities are not a strong function of temperature.)

b) Explain how a Column-III atom (with three outer-shell valence electrons) residing at a substitutional lattice site contributes a hole to the silicon lattice. Explain how a Column-V atom (with five outer-shell valence electrons) residing at a substitutional lattice site contributes an electron to the silicon lattice.

c) The following is a two-dimensional representation of the semiconductor GaAs:



Consider your answer in part **(b)**. If Si atoms are inserted as dopants in GaAs and exclusively replace Ga atoms in the lattice, will the Si-doped GaAs material be n-type or p-type? What if the Si atoms exclusively replace As atoms?

Problem 2: Carrier Concentrations and Doping

Consider a Si sample maintained at T = 300K, doped with arsenic to a concentration 10^{15} cm^{-3}.

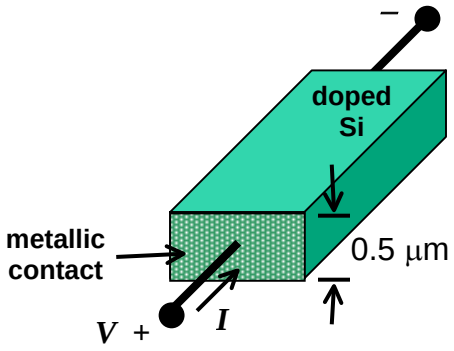
a) Is this material n-type or p-type? What are the majority and minority carrier concentrations?

b) Suppose the sample type is converted to the opposite type by counter-doping it with boron to a concentration 10^{17} cm^{-3}. What are the majority and minority carrier concentrations now?

c) As the temperature of this sample is increased, n_i will eventually increase to be higher than the dopant concentration, and the sample will become intrinsic ($n \cong p \cong n_i$). Estimate the temperature at which this occurs, by finding the temperature at which n_i be much greater (*i.e.* 10× higher) than $|N_A - N_D|$. You can use the formula for n_i given in Lecture 13, Slide 14, or simply use the plot of n_i *vs. T*.

Problem 3: Integrated-Circuit Resistor

Consider a resistor fabricated using a 0.5 μm-thick film of Si doped with phosphorus to a concentration 10^{18} cm^{-3}. The layout dimensions of this resistor are: length L = 5 μm; width W = 1.0 μm:



a) What is the sheet resistance of the Si film?

b) What is the resistance value for this resistor?

c) The saturation drift velocity for electrons in Si is ~10^7 cm/s. That is, this is the maximum drift velocity for electrons in Si. Sketch the current *vs.* voltage (*I-V*) characteristic of this resistor, for the range of voltages from –20V to 20V.

Problem 4: pn-Junction Electrostatics

As discussed in Lecture 14, a "depletion region" exists at the junction between p-type material and n-type material. This region is depleted of mobile carriers, so that there is significant net charge density (due to the immobile ionized dopants). The width W_j of the depletion region varies with the applied voltage V_D. Therefore, the amount of charge stored in the depletion region also varies with bias. This behavior is modeled as a capacitance. The junction capacitance $C_j = \varepsilon_{Si} A_D / W_j$ where A_D is the junction area and ε_{Si} = 10^{-12} F/cm is the dielectric permittivity of silicon.

a) If the width of the depletion region is 1 μm, and the area of the junction is 2 μm x 5 μm, what is the capacitance (in units of femto-farads, fF)?

b) Is the junction capacitance greater when $V_D < 0$ than when $V_D = 0$? Why or why not? (Explain qualitatively – no equations needed -- in one or two sentences.)