UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Spring 2004**

Homework Assignment #8
Issued: 3/11/04
Due: 2pm in 240 Cory on Friday, 3/19/04
Be sure to put your name and **Discussion Section** on your paper.

Problem 1: Hambley 10.12

Problem 2: Hambley 10.28

Problem 3: MOSFET Fundamentals

a) Explain qualitatively (without using any equations) how a conductive path is formed between the n-type source and drain regions of an n-channel enhancement-mode MOSFET (with a p-type body), by applying a suitable voltage on the gate electrode. How does the resistance between the source and drain change with increasing gate voltage?
b) How does the resistance between the source and drain change with drain voltage increasing from 0 V up to the gate voltage, for a long n-channel MOSFET? (Again, explain qualitatively without resorting to any equations.) Assume that the source and the body are each biased at 0 Volts.
c) How does your answer to part (b) change if the channel length is very short (so that velocity saturation effects are evident)?

Problem 4: MOSFET *I-V* characteristics

A long-channel n-channel enhancement-mode MOSFET has threshold voltage $V_T = 0.5$ V, process transconductance parameter $k_n' = 0.2$ mA/V^2, channel length $L = 1$ μm and channel width $W = 10$ μm.

a) Sketch the drain current *vs.* gate voltage (I_{DS} *vs.* V_{GS}) characteristic for $0 \le V_{GS} \le 5$ V, $V_{DS} = 0.5$ V.
b) Sketch the drain current *vs.* drain voltage (I_{DS} *vs.* V_{DS}) characteristics for $0 \le V_{DS} \le 5$ V, for $V_{GS} = 0$ V, 1 V, 2, V, 3 V, 4 V, and 5 V.
c) For each set of voltages below, state the region of operation and compute the drain current:
   i) $V_{GS} = 1$ V and $V_{DS} = 5$ V
   ii) $V_{GS} = 1$ V and $V_{DS} = 0.5$ V
   iii) $V_{GS} = 0$ V and $V_{DS} = 5$ V