Lecture #15

OUTLINE

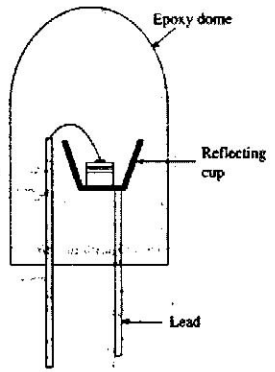
- Diode analysis and applications continued
- The MOSFET
  - The MOSFET as a controlled resistor
  - Pinch-off and current saturation
  - Channel-length modulation
  - Velocity saturation in a short-channel MOSFET

Reading

- **Rabaey *et al.***
  - **Chapter 3.3.1-3.3.2**
- **Hambley**
  - **Chapter 12.1**

Light Emitting Diode (LED)

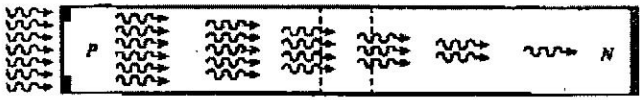
- LEDs are made of compound semiconductor materials
  - Carriers diffuse across a forward-biased junction and recombine in the quasi-neutral regions
    → optical emission



Semiconductor	*Color*	*Peak λ(μm)*
$GaAs_{0.6}P_{0.4}$	Red	0.650
$GaAs_{0.35}P_{0.65}$:N	Orange-Red	0.630
$GaAs_{0.14}P_{0.86}$:N	Yellow	0.585
GaP:N	Green	0.565
GaP:Zn-O	Red	0.700
AlGaAs	Red	0.650
AlInGaP	Orange	0.620
AlInGaP	Yellow	0.585
AlInGaP	Green	0.570
SiC	Blue	0.470
GaN	Blue	0.450

Optoelectronic Diodes (cont'd)

- Light incident on a pn junction generates electron-hole pairs
- The minority carriers which are generated in the depletion region, and the minority carriers which are generated in the quasi-neutral regions and then diffuse into the depletion region, are swept across the junction by the electric field



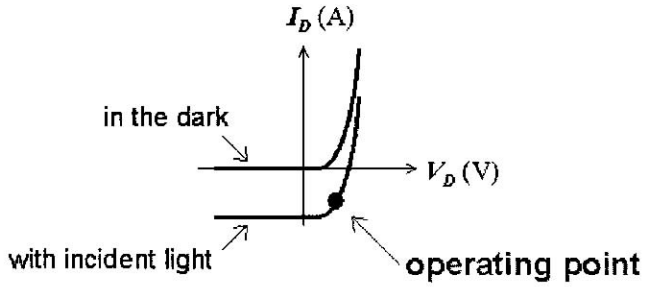
- This results in an additional component of current flowing in the diode:

$$I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$$

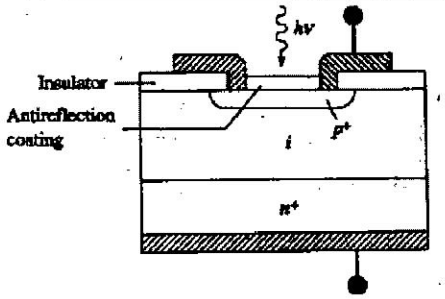
where $I_{optical}$ is proportional to the intensity of the light

Photovoltaic (Solar) Cell

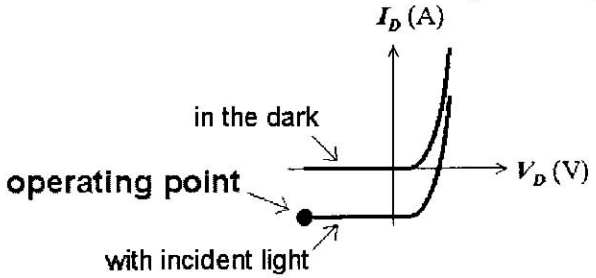
$$I_D = I_S(e^{qV_D/kT} - 1) - I_{optical}$$



Photodiode



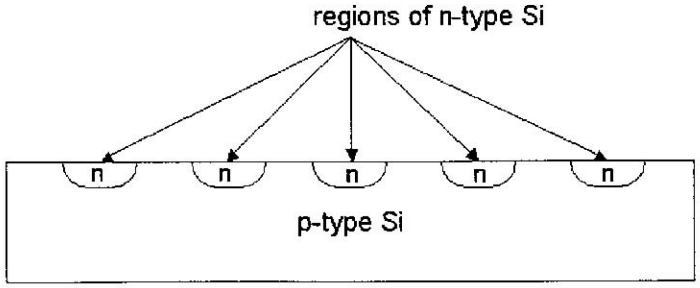
- An intrinsic region is placed between the p-type and n-type regions
  - $W_j \cong W_{i\text{-region}}$, so that most of the electron-hole pairs are generated in the depletion region
  - → faster response time (~10 GHz operation)



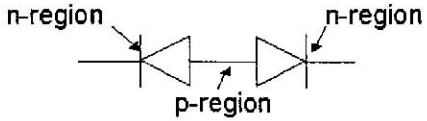
Why are pn Junctions Important for ICs?

- The basic building block in digital ICs is the MOS transistor, whose structure contains reverse-biased diodes.
  - pn junctions are important for electrical isolation of transistors located next to each other at the surface of a Si wafer.
  - The junction capacitance of these diodes can limit the performance (operating speed) of digital circuits

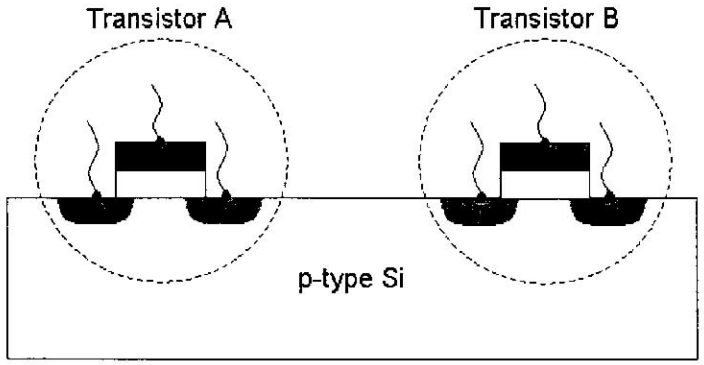
Device Isolation using pn Junctions



No current flows if voltages are applied between n-type regions, because two pn junctions are "back-to-back"



=> n-type regions **isolated** in p-type substrate and vice versa



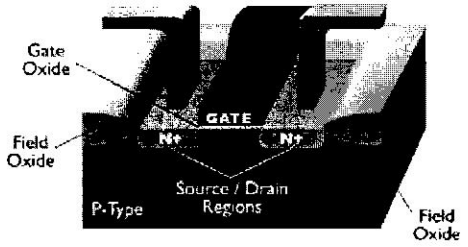
We can build large circuits consisting of many transistors without worrying about current flow between devices. The p-n junctions **isolate** the transistors because there is always at least one **reverse-biased** p-n junction in every potential current path.

Modern Field Effect Transistor (FET)

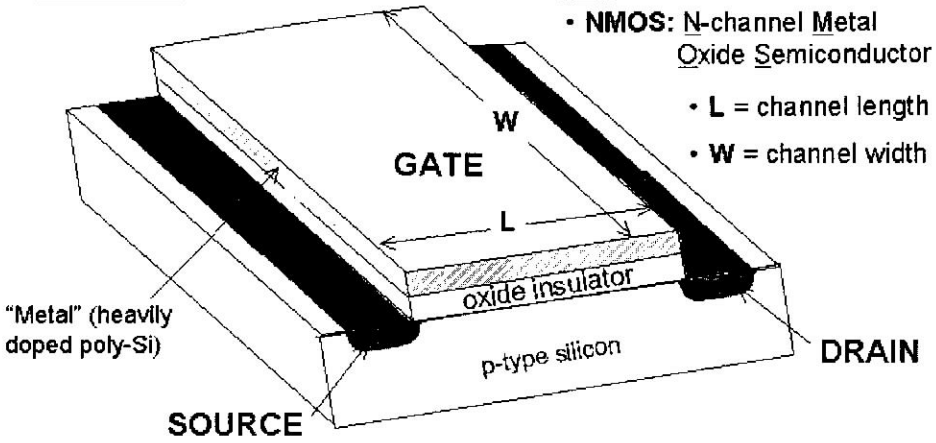
- An electric field is applied normal to the surface of the semiconductor (by applying a voltage to an overlying electrode), to modulate the conductance of the semiconductor

→ Modulate drift current flowing between 2 contacts ("source" and "drain") by varying the voltage on the "gate" electrode

Metal-oxide-semiconductor (MOS) FET:



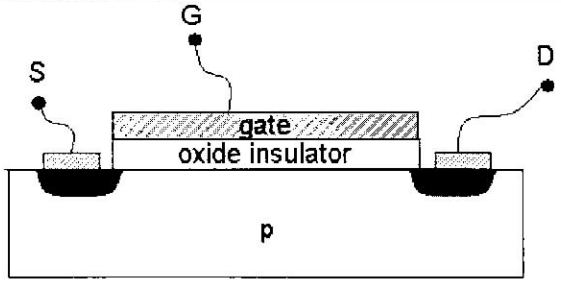
MOSFET



- **NMOS:** N-channel Metal Oxide Semiconductor
- **L** = channel length
- **W** = channel width

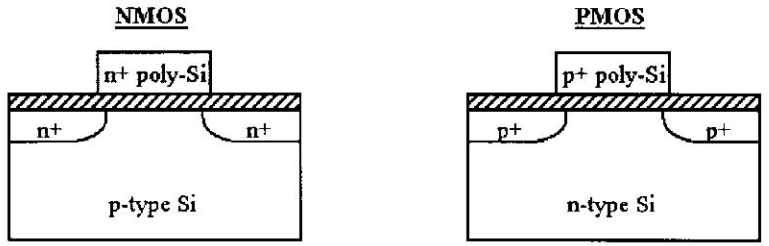
- A GATE electrode is placed above (electrically insulated from) the silicon surface, and is used to control the resistance between the SOURCE and DRAIN regions

N-channel MOSFET



- Without a gate voltage applied, no current can flow between the source and drain regions.
- Above a certain gate-to-source voltage (***threshold voltage*** V_T), a conducting layer of mobile electrons is formed at the Si surface beneath the oxide. These electrons can carry current between the source and drain.

N-channel *vs.* P-channel MOSFETs

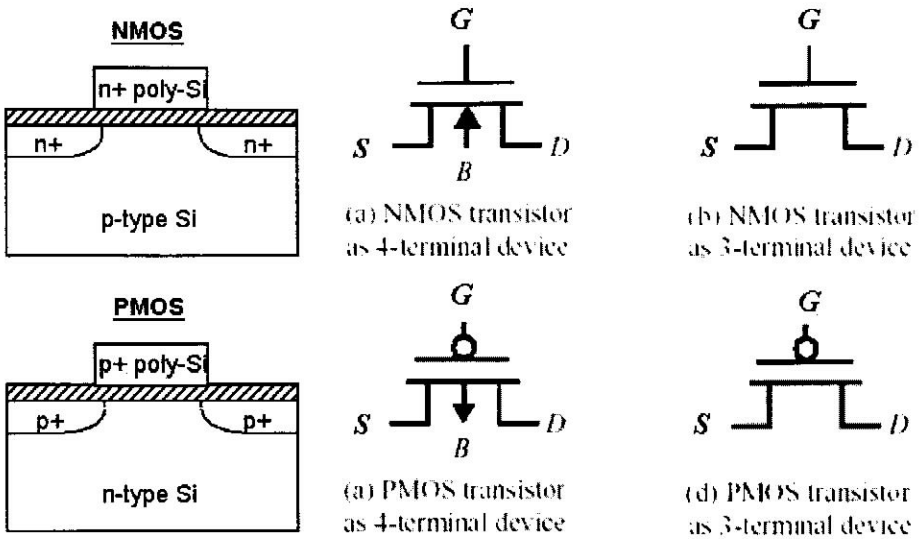


- For current to flow, $V_{GS} > V_T$
- Enhancement mode: $V_T > 0$
- Depletion mode: $V_T < 0$
  - Transistor is ON when V_G=0V

- For current to flow, $V_{GS} < V_T$
- Enhancement mode: $V_T < 0$
- Depletion mode: $V_T > 0$
  - Transistor is ON when V_G=0V

("n+" denotes very heavily doped n-type material; "p+" denotes very heavily doped n-type material)

MOSFET Circuit Symbols

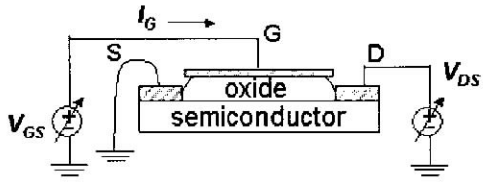


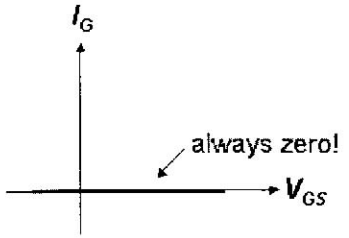
MOSFET Terminals

- The voltage applied to the GATE terminal determines whether current can flow between the SOURCE & DRAIN terminals.
  - For an n-channel MOSFET, the SOURCE is biased at a *lower* potential (often 0 V) than the DRAIN
    (Electrons flow from SOURCE to DRAIN when $V_G > V_T$)
  - For a p-channel MOSFET, the SOURCE is biased at a *higher* potential (often the supply voltage V_{DD}) than the DRAIN
    (Holes flow from SOURCE to DRAIN when $V_G < V_T$)
- The BODY terminal is usually connected to a fixed potential.
  - For an n-channel MOSFET, the BODY is connected to 0 V
  - For a p-channel MOSFET, the BODY is connected to V_{DD}

NMOSFET I_G vs. V_{GS} Characteristic

Consider the current I_G (flowing into **G**) versus V_{GS}:



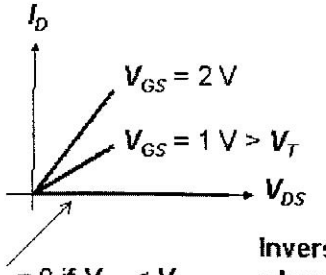


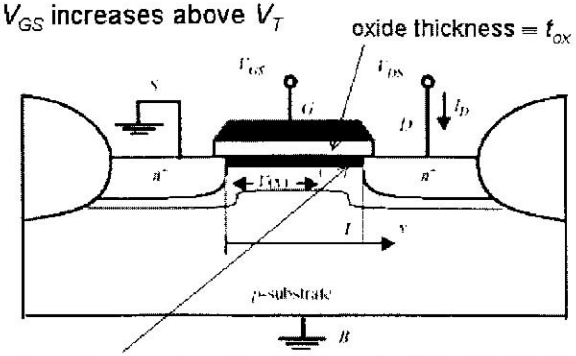
The gate is insulated from the semiconductor, so there is no significant gate current.

The MOSFET as a Controlled Resistor

- The MOSFET behaves as a resistor when V_{DS} is low:
  - Drain current I_D increases linearly with V_{DS}
  - Resistance R_{DS} between SOURCE & DRAIN depends on V_{GS}
    - R_{DS} is lowered as V_{GS} increases above V_T

NMOSFET Example:

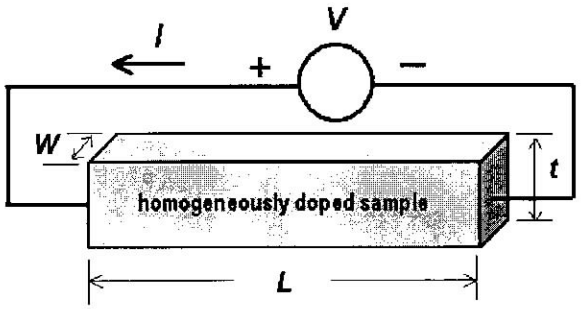




Inversion charge density $Q_i(x) = -C_{ox}[V_{GS}-V_T-V(x)]$
where $C_{ox} \equiv \varepsilon_{ox} / t_{ox}$

Sheet Resistance Revisited

Consider a sample of n-type semiconductor:

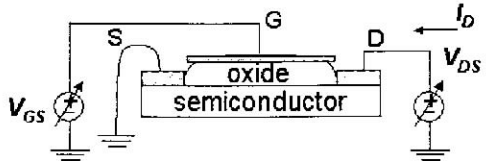


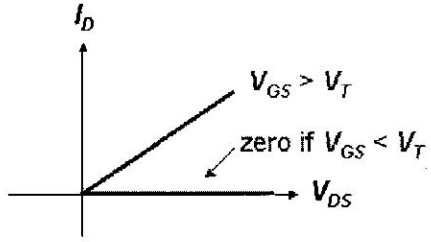
$$R_s = \frac{\rho}{t} = \frac{1}{\sigma t} = \frac{1}{q\mu_n n t} = \frac{1}{\mu_n Q_n}$$

where Q_n is the charge per unit area

NMOSFET I_D vs. V_{DS} Characteristics

Next consider I_D (flowing into **D**) versus V_{DS}, as V_{GS} is varied:





Above threshold ($V_{GS} > V_T$): "inversion layer" of electrons appears, so conduction between **S** and **D** is possible

Below "threshold" ($V_{GS} < V_T$): no charge → no conduction

MOSFET as a Controlled Resistor (cont'd)

$$I_D = \frac{V_{DS}}{R_{DS}}$$

$$R_{DS} = R_s(L/W) = \frac{L/W}{\mu_n Q_i} = \frac{L/W}{\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})}$$

average value of $V(x)$

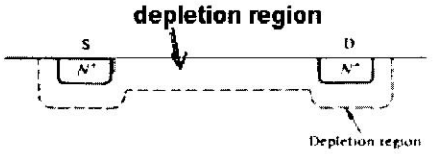
$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}}$$

We can make R_{DS} low by

- applying a large "gate drive" ($V_{GS} - V_T$)
- making W large and/or L small

Charge in an N-Channel MOSFET

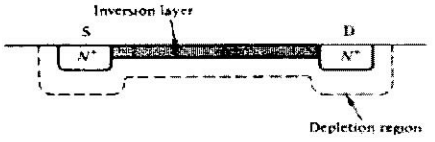
$V_{GS} < V_T$:



(no inversion layer at surface)

$V_{GS} > V_T$:

$V_{DS} \approx 0$



$$I_D = WQ_{inv}v$$
$$= WQ_{inv}\mu_n E$$

$V_{DS} > 0$ (small)

$$= WQ_{inv}\mu_n\left(\frac{V_{DS}}{L}\right)$$

Average electron velocity **v** is proportional to lateral electric field **E**

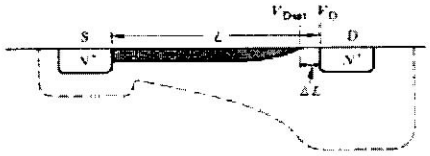
What Happens at Larger V_{DS}?

$V_{GS} > V_T$:

$V_{DS} = V_{GS} - V_T$

Inversion-layer is "pinched-off" at the drain end

$V_{DS} > V_{GS} - V_T$



As V_{DS} increases above $V_{GS} - V_T \equiv V_{DSAT}$, the length of the "pinch-off" region ΔL increases:

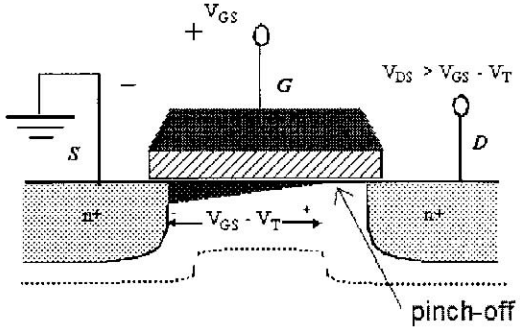
- **"extra" voltage ($V_{DS} - V_{Dsat}$) is dropped across the distance ΔL**
- **the voltage dropped across the inversion-layer "resistor" remains V_{Dsat}**

  $\Rightarrow$ the drain current I_D saturates

Note: Electrons are swept into the drain by the *E*-field when they enter the pinch-off region.

Summary of I_D vs. V_{DS}

- As V_{DS} increases, the inversion-layer charge density at the drain end of the channel is reduced; therefore, I_D does not increase linearly with V_{DS}.
- When V_{DS} reaches $V_{GS} - V_T$, the channel is "pinched off" at the drain end, and I_D saturates (*i.e.* it does not increase with further increases in V_{DS}).



$$I_{DSAT} = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2$$

I_D vs. V_{DS} Characteristics

The MOSFET I_D-V_{DS} curve consists of two regions:

1) Resistive or "Triode" Region: $0 < V_{DS} < V_{GS} - V_T$

$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where $k_n' = \mu_n C_{ox}$

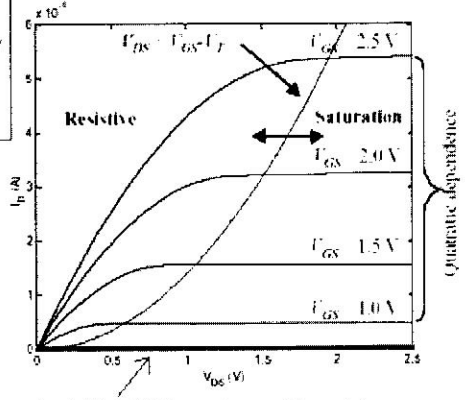
process transconductance parameter

2) Saturation Region:

$V_{DS} > V_{GS} - V_T$

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

where $k_n' = \mu_n C_{ox}$

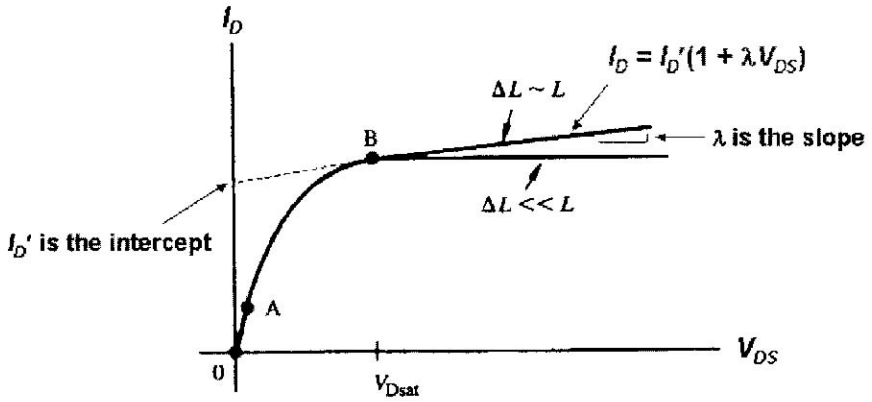


"CUTOFF" region: $V_G < V_T$

Channel-Length Modulation

If L is small, the effect of ΔL to reduce the inversion-layer "resistor" length is significant

$\rightarrow I_D$ increases noticeably with ΔL (*i.e.* with V_{DS})

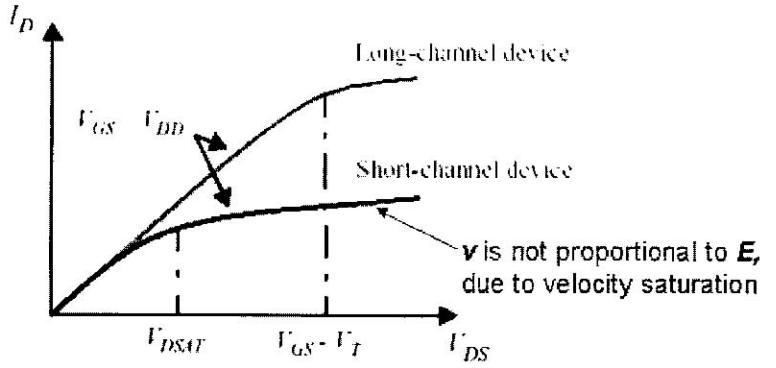


Velocity Saturation

At *high electric fields*, the average velocity of carriers is NOT proportional to the field; it saturates at ~10^7 cm/sec for both electrons and holes:

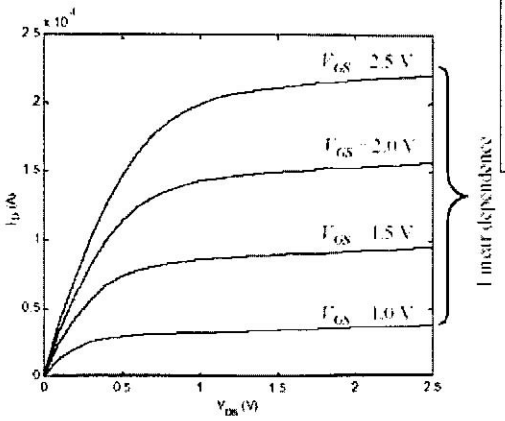
Current Saturation in Modern MOSFETs

- In digital ICs, we typically use transistors with the shortest possible gate-length for high-speed operation.
- In a very short-channel MOSFET, I_D saturates because the carrier velocity is limited to ~10^7 cm/sec



Consequences of Velocity Saturation

1. I_D is lower than that predicted by the mobility model
2. I_D increases **linearly** with $V_{GS} - V_T$ rather than quadratically in the saturation region



$$I_{DSAT} = WC_{ox}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]v_{sat}$$

where $V_{DSAT} = \frac{L}{\mu_n} v_{sat}$

P-Channel MOSFET I_D vs. V_{DS}

- As compared to an n-channel MOSFET, the signs of all the voltages and the currents are reversed:

Note that the effects of velocity saturation are less pronounced than for an NMOSFET. ***Why is this the case?***