Lecture #18

**OUTLINE**
- Continue small signal analysis
- Logic functions
- NMOS logic gates
- The CMOS inverter

**Reading**
- Rabaey *et al.*: Chapter 5.2
- Hambley: Chapter 7.1-7.2

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**Digital Signals**
- For a digital signal, the voltage must be within one of two ranges in order to be defined:
  - "1": \[ V_{OH} \text{ to } V_{DD} \]
  - "0": \[ V_{IL} \text{ to } V_{OL} \]
- Positive Logic:
  - "low" voltage = logic state 0
  - "high" voltage = logic state 1

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**Logic Functions, Symbols, & Notation**

<table>
<thead>
<tr>
<th>NAME</th>
<th>SYMBOL</th>
<th>NOTATION</th>
<th>TRUTH TABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;NOT&quot;</td>
<td>![Not Symbol]</td>
<td>[ F = \overline{A} ]</td>
<td>[ \begin{array}{c</td>
</tr>
<tr>
<td>&quot;OR&quot;</td>
<td>![Or Symbol]</td>
<td>[ F = A + B ]</td>
<td>[ \begin{array}{c</td>
</tr>
<tr>
<td>&quot;AND&quot;</td>
<td>![And Symbol]</td>
<td>[ F = A \cdot B ]</td>
<td>[ \begin{array}{c</td>
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<tr>
<td>&quot;XOR&quot;</td>
<td>![Xor Symbol]</td>
<td>(exclusive OR) [ F = A \oplus B ]</td>
<td>[ \begin{array}{c</td>
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NMOS Inverter ("NOT" Gate)

Circuit:
\[ V_{DD} \]
\[ I_D \]
\[ V_{IN} = V_{DD} \]
\[ V_{DD}/R_D \]
\[ V_{GS} = V_{IN} \leq V_T \]
\[ V_{DS} = V_{OUT} \]

Voltage-Transfer Characteristic:
Increasing
\[ V_{DS} = V_{IN} \]
\[ V_{DD} \]
\[ V_{DS} \]

Noise Margins

Definition of Input Levels

Definition of Noise Margins

Noise margin high
\[ NM_H = V_{OH} - V_{IH} \]

Noise margin low
\[ NM_L = V_{IL} - V_{OL} \]

NMOS NAND Gate

- Output is low only if both inputs are high

Truth Table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
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NMOS NOR Gate

- Output is low if either input is high

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Disadvantages of NMOS Logic Gates

- Large values of $R_D$ are required in order to
  - achieve a low value of $V_{OL}$
  - keep power consumption low

→ Large resistors are needed, but these take up a lot of space.

- One solution is to replace the resistor with an NMOSFET that is always on.

The CMOS Inverter: Intuitive Perspective

CIRCUIT

SWITCH MODELS

Low static power consumption, since one MOSFET is always off in steady state

CMOS Inverter Voltage Transfer Characteristic

CMOS Inverter Load-Line Analysis

$V_{IN} = V_{DD}$

$V_{OUT} = V_{DD} + V_{DS}$

$V_{IN} = 0$ V

$V_{OUT} = V_{DD} + V_{DS}$

Increasing

Increasing $V_{IN}$