

Lecture #21

ANNOUNCEMENT

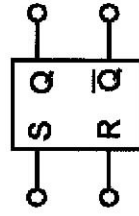
- Midterm 2 thurs. april 15, 9:40-11am.
- A-M initials in 10 Evans
- N-Z initials in Sibley auditorium
- Closed book, except for two 8.5 x 11 inch cheat sheets
- Comprehensive, but focuses on HW's 5-9; L's, C's, 1st-order ckts, semiconductor devices, diode ckts, mosfet model, common source amplifier
- extra office hour with Mervin in 297 Cory next Monday 6-7pm

OUTLINE

- Sequential logic circuits
- Fan-out
- Propagation delay
- CMOS power consumption

Reading: Hambley Ch. 7; Rabaey et al. Secs. 5.2, 5.5, 6.2.1

The S-R ("Set" - "Reset") Flip-Flop

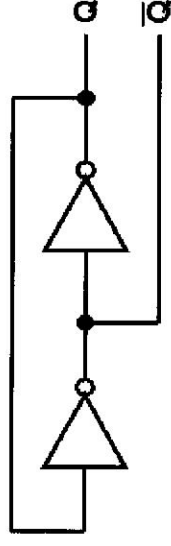


S-R Flip-Flop Symbol:

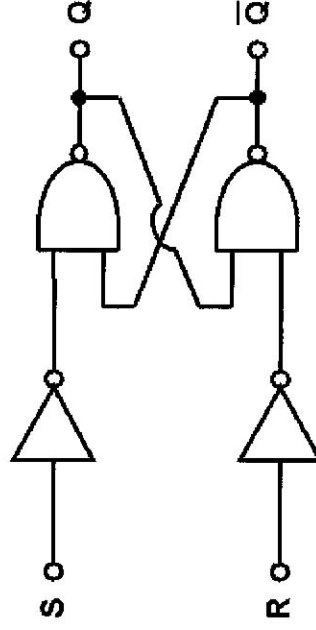
- Rule 1:
 - If $S = 0$ and $R = 0$, Q does not change.
- Rule 2:
 - If $S = 0$ and $R = 1$, then $Q = 0$
- Rule 3:
 - If $S = 1$ and $R = 0$, then $Q = 1$
- Rule 4:
 - $S = 1$ and $R = 1$ should never occur.

Flip-Flops

- One of the basic building blocks for sequential circuits is the **flip-flop**:
 - 2 stable operating states \rightarrow stores 1 bit of info.
 - A simple flip-flop can be constructed using two inverters:

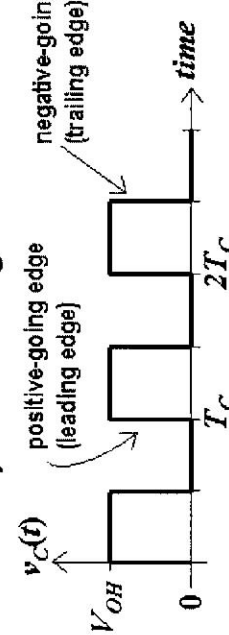


Realization of the S-R Flip-Flop



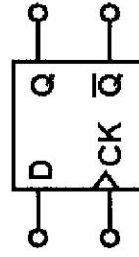
R	S	Q_n	Q_{n+1}
0	0	0	1
0	1	1	0
1	0	0	0
1	1	1	1 (not allowed)

Clock Signals

- Often, the operation of a sequential circuit is synchronized by a **clock signal** :
- 
- The clock signal regulates when the circuits respond to new inputs, so that operations occur in proper sequence.
 - Sequential circuits that are regulated by a clock signal are said to be **synchronous**.

The D ("Delay") Flip-Flop

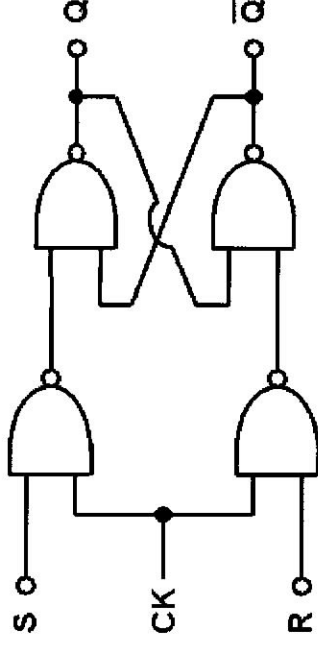
D Flip-Flop Symbol:



- The output terminals **Q** and **Q** behave just as in the S-R flip-flop.
- Q** changes only when the clock signal **CK** makes a positive transition.

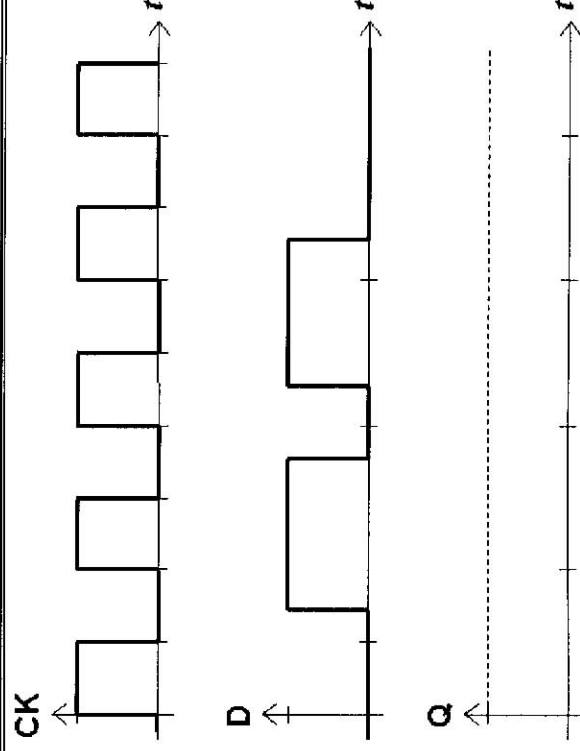
CK	D	Q _n
0	x	Q _{n-1}
1	x	Q _{n-1}
↑	0	0
↑	1	1

Clocked S-R Flip-Flop



- When **CK = 0**, the value of **Q** does not change
- When **CK = 1**, the circuit acts like an ordinary S-R flip-flop

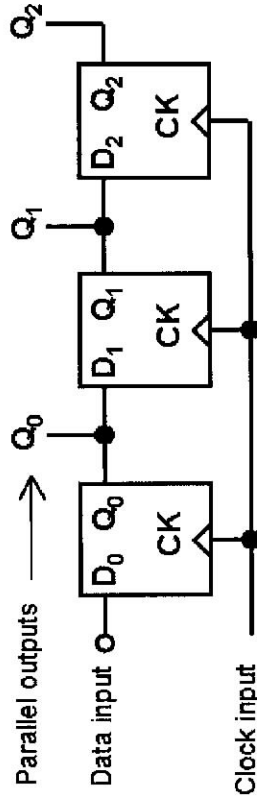
D Flip-Flop Example (Timing Diagram)



Registers

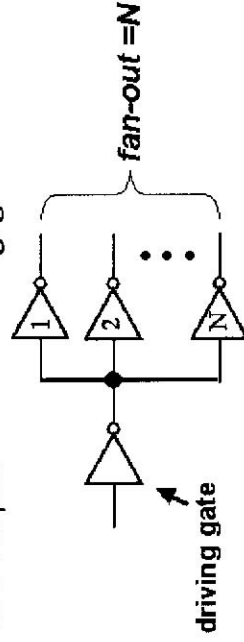
- A **register** is an array of flip-flops that is used to store or manipulate the bits of a digital word.

Example: Serial-In, Parallel-Out Shift Register



Fan-Out

- Typically, the output of a logic gate is connected to the input(s) of one or more logic gates
- The **fan-out** is the number of gates that are connected to the output of the driving gate:



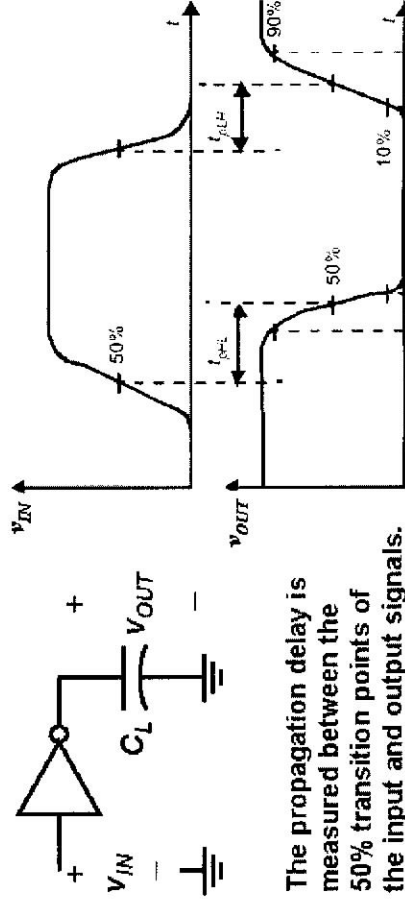
- Fanout leads to increased capacitive load on the driving gate, and therefore longer propagation delay
 - The input capacitances of the driven gates sum, and must be charged through the equivalent resistance of the driver

Conclusion (Logic Circuits)

- Complex combinational logic functions can be achieved simply by interconnecting NAND gates (or NOR gates).
- Logic gates can be interconnected to form flip-flops.
- Interconnections of flip-flops form registers.
- A complex digital system such as a computer consists of many gates, flip-flops, and registers. Thus, logic gates are the basic building blocks for complex digital systems.

Effect of Capacitive Loading

- When an input signal of a logic gate is changed, there is a **propagation delay** before the output of the logic gate changes. This is due to capacitive loading at the output.



The propagation delay is measured between the 50% transition points of the input and output signals.

Calculating the Propagation Delay

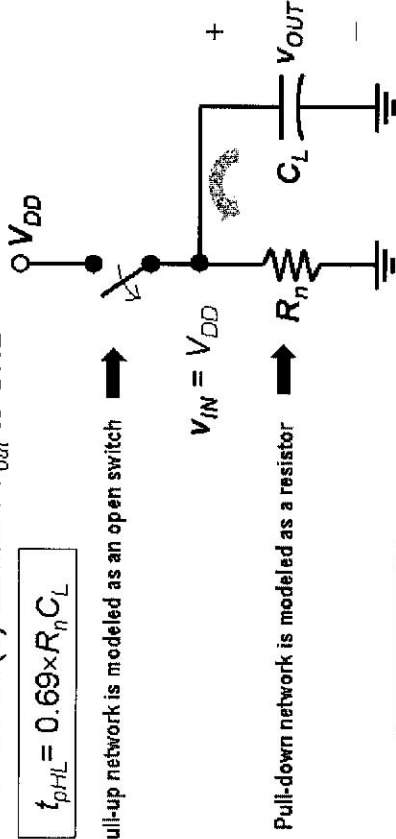
Model the MOSFET in the ON state as a resistive switch:

Case 1: V_{out} changing from High to Low
(input signal changed from Low to High)

- PMOSFET(s) connect V_{out} to GND

$$t_{pHL} = 0.69 \times R_n \times C_L$$

Pull-up network is modeled as an open switch



Pull-down network is modeled as a resistor

Output Capacitance of a Logic Gate

- The output capacitance of a logic gate is comprised of several components:

- "intrinsic capacitance" → pn-junction and gate-drain capacitance
- both NMOS and PMOS transistors
- "extrinsic capacitance" → capacitance of connecting wires
- input capacitances of the fan-out gates

Impact of gate-drain capacitance

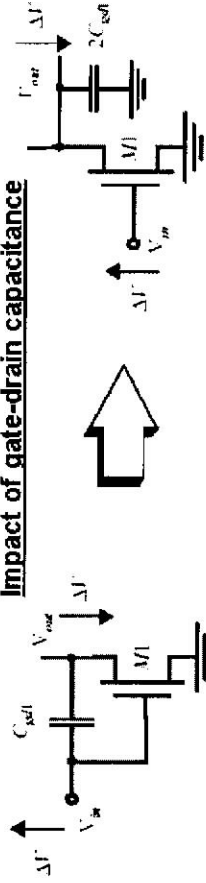


Figure 5.14 The Miller effect → A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value.

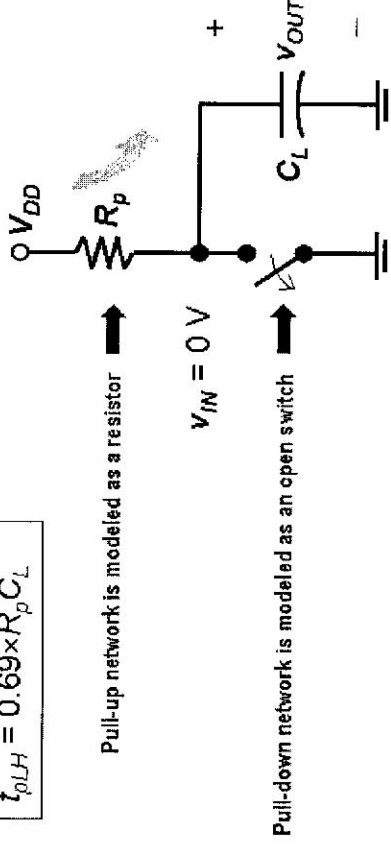
Calculating the Propagation Delay (cont'd)

Case 2: V_{out} changing from Low to High
(input signal changed from High to Low)

- PMOSFET(s) connect V_{out} to V_{DD}

$$t_{pLH} = 0.69 \times R_p \times C_L$$

Pull-up network is modeled as a resistor



Pull-down network is modeled as an open switch

Minimizing Propagation Delay

- A fast gate is built by

1. Keeping the output capacitance C_L small

- Minimize the area of drain pn junctions.
- Lay out devices to minimize interconnect capacitance.
- Avoid large fan-out.

2. Decreasing the equivalent resistance of the transistors

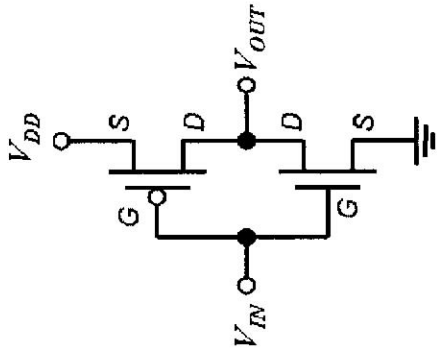
- Decrease L
- Increase W
- ... but this increases pn junction area and hence C_L

3. Increasing V_{DD}

- trade-off with power consumption & reliability

Transistor Sizing for Performance

- Widening the transistors reduces resistance, but increases capacitance
- In order to have the on-state resistance of the PMOS transistor match that of the NMOS transistor (e.g. to achieve a symmetric voltage transfer curve), its W/L ratio must be larger by a factor of ~ 3 . To achieve minimum propagation delay, however, the optimum factor is ~ 2 .



EECS40, Spring 2004

Lecture 21, Slide 17

Prof. Sanders

CMOS Power Consumption

- The total power consumed by a CMOS circuit is comprised of several components:

- Dynamic power consumption due to charging and discharging capacitances*:

$$P_{dyn} = C_L V_{DD}^2 f_{0 \rightarrow 1} = C_{EFF} V_{DD}^2 f$$

$f_{0 \rightarrow 1}$ = frequency of 0 \rightarrow 1 transitions ("switching activity")

f = clock rate (maximum possible event rate)

Effective capacitance C_{EFF} = average capacitance charged every clock cycle

* This is typically by far the dominant component!

EECS40, Spring 2004

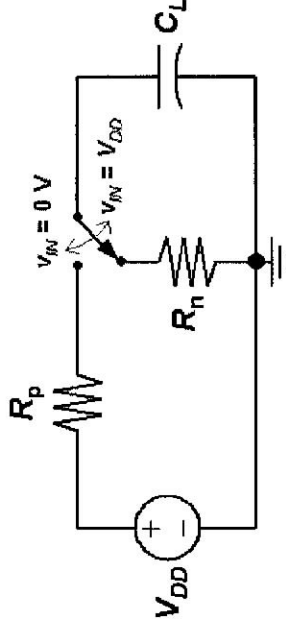
Lecture 21, Slide 19

Prof. Sanders

CMOS Energy Consumption (Review)

- The energy delivered by the voltage source in charging the load capacitance is $C_L V_{DD}^2$
 - Half of this is stored in C_L ; the other half is absorbed by the resistance through which C_L is charged.

\rightarrow In one complete cycle (charging and discharging), the total energy delivered by the voltage source is $C_L V_{DD}^2$



EECS40, Spring 2004

Lecture 21, Slide 18

Prof. Sanders

CMOS Power Consumption (cont'd)

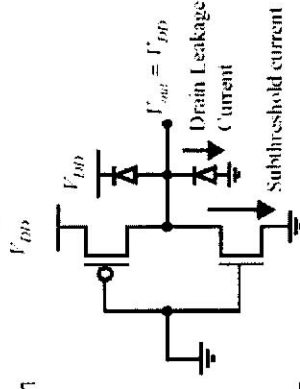
- Dynamic power consumption due to direct-path currents during switching

$$P_{dp} = C_{sc} V_{DD}^2 f$$

$C_{sc} = t_{sc, peak} / V_{DD}$ is the equivalent capacitance charged every clock cycle due to "short-circuits" between V_{DD} & GND (typically <10% of total power consumed)

- Static power consumption due to transistor leakage and pn-junction leakage

$$P_{stat} = I_{stat} V_{DD}$$



EECS40, Spring 2004

Lecture 21, Slide 20

Prof. Sanders

Low-Power Design Techniques

1. Reduce V_{DD}

- quadratic effect on P_{dyn}
Example: Reducing V_{DD} from 2.5 V to 1.25 V reduces power dissipation by factor of 4
- Lower bound is set by V_T : V_{DD} should be $>2V_T$

2. Reduce load capacitance

- Use minimum-sized transistors whenever possible

3. Reduce the switching activity

- involves design considerations at the architecture level (beyond the scope of this class!)

NAND Gates vs. NOR Gates

- In order for a 2-input NAND gate to have the same pull-down delay (t_{pHL}) as an inverter, the NMOS devices in the NAND gate must be made twice as wide.
 - This first-order analysis neglects the increase in capacitance which results from widening the transistors.
 - Note: The delay depends on the input signal pattern.
 - In order for a 2-input NOR gate to have the same pull-up delay (t_{pLH}) as an inverter, the PMOS devices in the NOR gate must be made twice as wide.
 - Since hole mobility is lower than electron mobility (so that larger W/L ratios are needed for PMOS devices as compared with NMOS devices), stacking PMOS devices in series (as is done in a NOR gate) should be avoided as much as possible.
- **NAND gates are preferred for implementing logic!**