Lecture #26

ANNOUNCEMENTS

- Basic Tutebot demonstration due by Fri. May 7 in lab section
- Tutebot demonstration contest on Tues., May 11, 9:30-11am, 10 Evans – possible extra credit for strong efforts. Class staff will judge.

OUTLINE

- Interconnect modeling
- Propagation delay with interconnect
- Inter-wire capacitance
- Pi model for capacitive coupling
- Coupling capacitance effects
  - loading
  - crosstalk

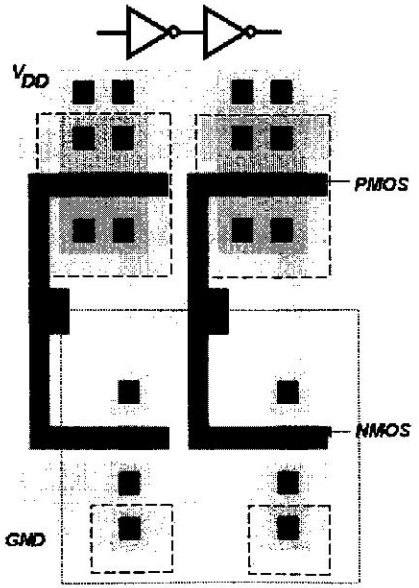
Reading (Rabaey *et al.*)
Chapter 4: Secs. 4.1-4.4.4 ; Chapter 5: pp. 212-213

Interconnects

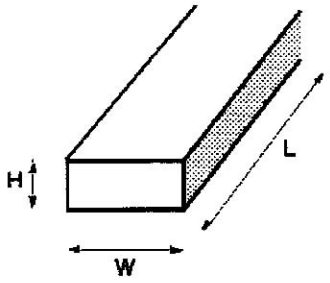
- An ***interconnect*** is a thin-film wire that electrically connects 2 or more components in an integrated circuit.
- Interconnects can introduce parasitic (unwanted) components of capacitance, resistance, and inductance. These ***"parasitics"*** detrimentally affect
  - performance (*e.g.* propagation delay)
  - power consumption
  - reliability
- As transistors are scaled down in size and the number of metal wiring layers increases, the impact of interconnect parasitics increases.
  → Need to model interconnects, to evaluate their impact

Interconnect Resistance & Capacitance

Metal lines run over thick oxide covering the substrate
→ **contribute RESISTANCE & CAPACITANCE to the output node of the driving logic gate**



Wire Resistance



$$R_{wire} = \frac{\rho L}{H W} = R_s \frac{L}{W}$$

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Material	Sheet Res. (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

Interconnect Resistance Example

Typical values of R_n and R_p are **~10 kΩ**, for W/L = 1

... but R_n, R_p are much lower for large transistors (used to drive long interconnects with reasonable t_p)

Compare with the resistance of a 0.5μm-thick Al wire:

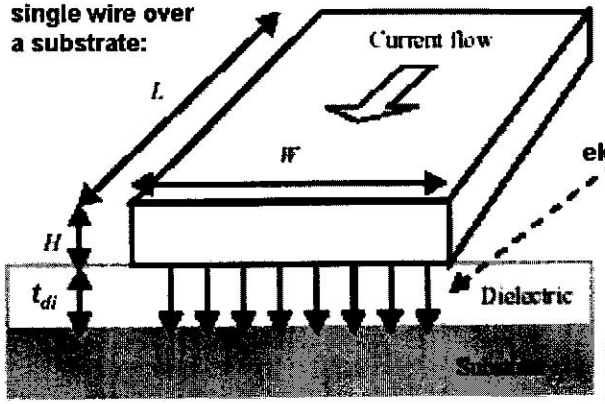
$R_\square = \rho / H = (2.7\ \mu\Omega\text{-cm}) / (0.5\ \mu\text{m}) = 5.4 \times 10^{-2}\ \Omega /$

Example: $L = 1000\ \mu$m, $W = 1\ \mu$m

$\rightarrow R_{wire} = R\ (L / W)$

$= (5.4 \times 10^{-2}\ \Omega /\ \ )(1000/1) = \mathbf{54\ \Omega}$

Wire Capacitance: The Parallel Plate Model



$$C_{pp} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Relative Permittivities

Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Parallel-Plate Capacitance Example

- Oxide layer is typically ~500 nm thick
- Interconnect wire width is typically ~0.5 μm wide (1st level)

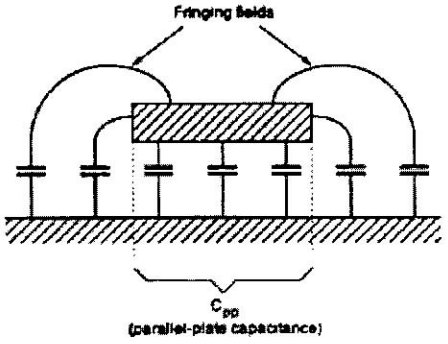
$\Rightarrow$ capacitance per unit length = 345 fF/cm = 34.5 aF/μm

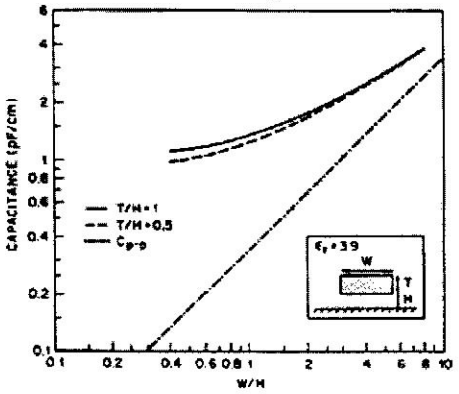
Example: $L = 30\ \mu$m

$\rightarrow C_{pp} \cong 1$ fF (compare with C_n~ 2 fF)

Fringing-Field Capacitance

For $W / t_{di} < 1.5$, C_{fringe} is dominant





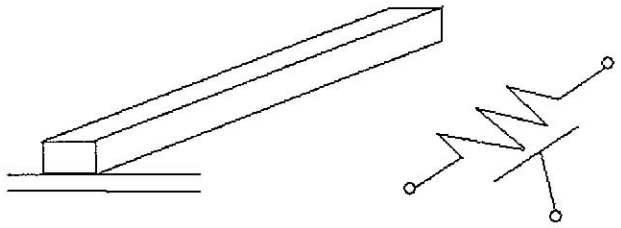
Wire capacitance per unit length:

$$c_{wire} \cong c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di} / H)} \qquad w = W - \frac{H}{2}$$

Modeling an Interconnect

Problem: Wire resistance and capacitance to underlying substrate is spread along the length of the wire

"Distributed RC line"

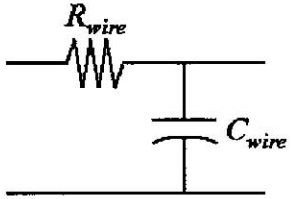


We will start with a simple model...

Lumped RC Model

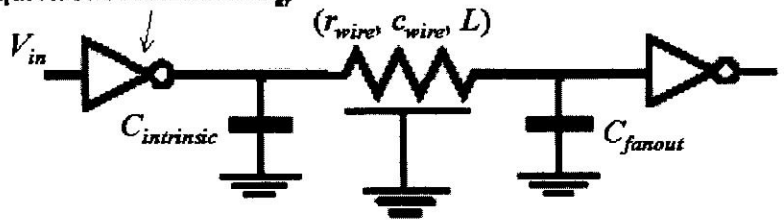
Model the wire as single capacitor and single resistor:

- C_{wire} is placed at the end of the interconnect
  → adds to the gate capacitance of the load
- R_{wire} is placed at the logic-gate output node
  → adds to the MOSFET equivalent resistance

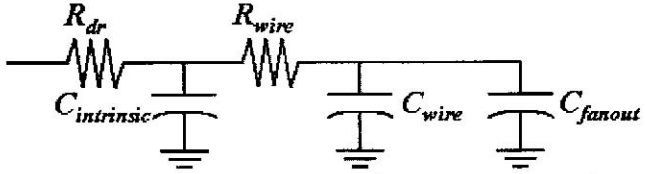


Cascaded CMOS Inverters w/ Interconnect

Equivalent resistance R_{dr}



Using "lumped RC" model for interconnect:



$$\tau_D = R_{dr}C_{intrinsic} + (R_{dr} + R_{wire})(C_{wire} + C_{fanout})$$
$$= R_{dr}C_{intrinsic} + (R_{dr} + R_{wire})C_{fanout} + (R_{dr} + R_{wire})C_{wire}$$

Effect of Interconnect Scaling

$$R_{wire}C_{wire} = \left[\rho\frac{L}{WH}\right]\left[\frac{\varepsilon_{di}}{t_{di}}(WL) + \frac{2\pi\varepsilon_{di}L}{\log(t_{di}/H)}\right] \propto \rho\varepsilon_{di}L^2$$

- Interconnect delay scales as square of L
  ⇒ minimize interconnect length!
- If W is large, then it does not appear in $R_{wire}C_{wire}$
  - Capacitance due to fringing fields becomes more significant as W is reduced; C_{wire} doesn't actually scale with W for small W

Propagation Delay with Interconnect

Using the lumped-RC interconnect model:

$$t_p = 0.69\tau_D$$
$$= 0.69\,R_{dr}C_{intrinsic} + 0.69(R_{dr} + R_{wire})C_{fanout}$$
$$+ 0.69(R_{dr} + R_{wire})C_{wire}$$

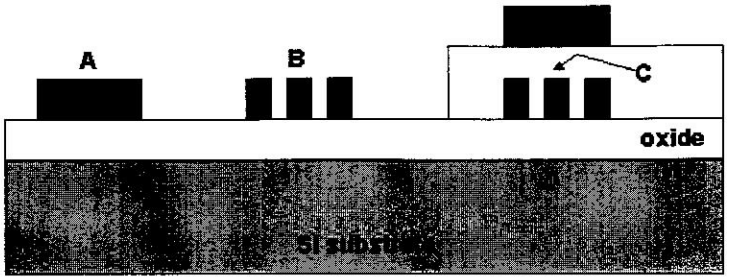
In reality, the interconnect resistance & capacitance are distributed along the length of the interconnect.

→ The interconnect delay is actually less than $R_{wire}C_{wire}$:

$$t_p = 0.69R_{dr}C_{intrinsic} + 0.69(R_{dr} + R_{wire})C_{fanout}$$
$$+ (0.69R_{dr} + 0.38R_{wire})C_{wire}$$

The 0.38 factor accounts for the fact that the wire resistance and capacitance are distributed.

Interconnect Wire-to-Wire Capacitance



Wire A simply has capacitance (C_{pp} + C_{fringe}) to substrate

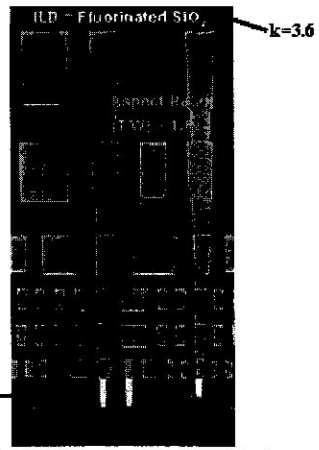
Wire B has additional sidewall capacitance to neighboring wires

Wire C has additional capacitance to the wire above it

Wiring Examples - Intel Processes

Advanced processes: narrow linewidths, taller wires, close spacing → relatively large inter-wire capacitances

Intel 0.25µm Process (Al)
5 Layers - Tungsten Vias
Source: *Intel Technical Journal* 3Q98



Intel 0.13µm Process (Cu)
Source: *Intel Technical Journal* 2Q02

Effects of Inter-Wire Capacitance

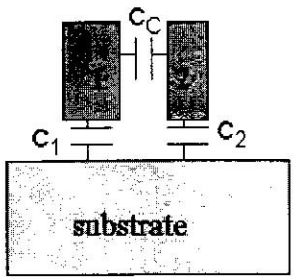
- Capacitance between closely spaced lines leads to two major effects:
  1. **Increased capacitive loading on driven nodes (speed loss)**
  2. **Unwanted transfer of signals from one place to another through capacitive coupling *"crosstalk"***
- We will use a very simple model to estimate the magnitude of these effects. In real circuit designs, very careful analysis is necessary.

Pi Model for Capacitive Coupling

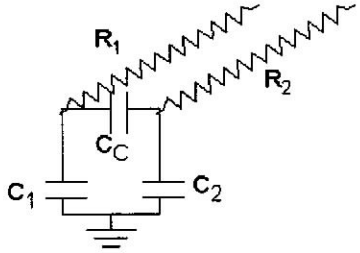
There are three capacitances as illustrated

Wire 1 has resistance R_1

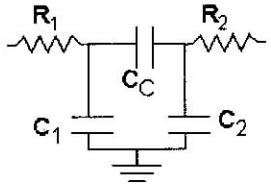
Wire 2 has resistance R_2



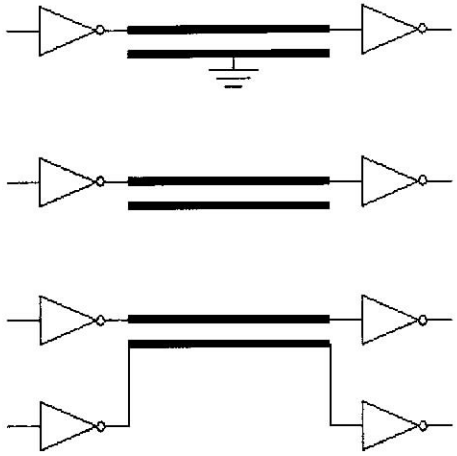
Using a simple lumped model for each wire we have three capacitances and two resistances



Which, when redrawn in a plane, has a "π" shape



Coupling Capacitance: Loading Effect



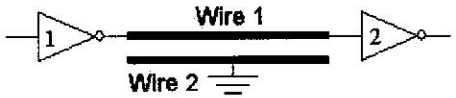
A) Coupling to grounded adjacent line

B) Coupling to floating adjacent line

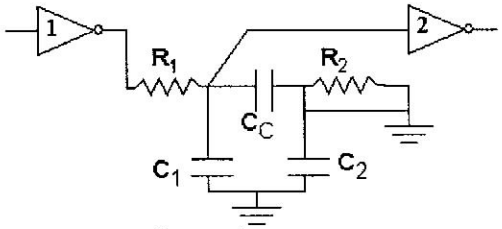
C) Coupling to driven adjacent line

Case C is well-approximated to be the same as case A

Case A: Coupling to Grounded Line



Insert the Pi model:



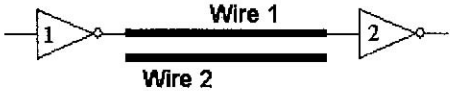
C_1 and C_C are in parallel with the input capacitance of inverter 2, C_{in2}.

This combined C is driven by the output resistance of inverter 1 in series with the line resistance R_1

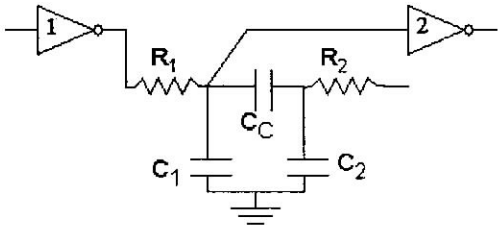
intrinsic capacitance of inverter 1

$$\tau_D = R_{dr1}C_{out1} + (R_1 + R_{dr1})(C_1 + C_C + C_{in2})$$

Case B: Coupling to Floating Line



Insert the Pi model:

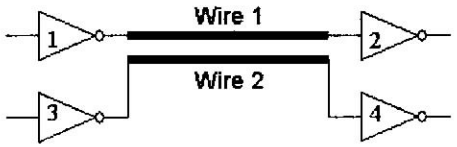


C_1 is in parallel with the series combination of C_C and C_2.

This combined C is driven by the output resistance of inverter 1 in series with the line resistance R_1

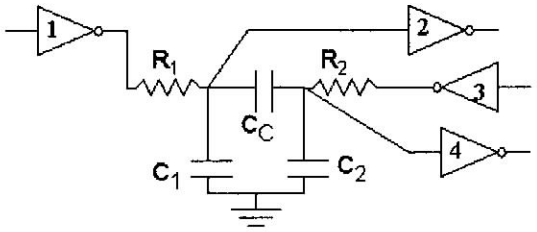
$$\tau_D = R_{dr1}C_{out1} + (R_1 + R_{dr1})\left(C_1 + \frac{C_2 C_C}{C_2 + C_C} + C_{in2}\right)$$

Coupling Capacitance: Crosstalk



Signal from (1) couples to adjacent line

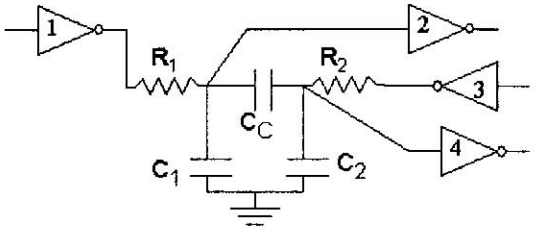
Insert Pi model:



Note that (4) receives both from (3) and from (1). The latter is undesired crosstalk.

Similarly, (2) receives signal both from (1) and from (3).

Let's assume (3) is quiet, and (1) is broadcasting…



We want to estimate the magnitude of the crosstalk signal at the input to (4).

We cannot easily treat this problem exactly (yet), but we can see that:

1. The crosstalk signal is attenuated by the capacitive voltage divider C_C in series with (C_2 || C_{in4}).
2. If C_C is very large, about half the signal from (1) is coupled into (4) because of the voltage divider R_1+R_{dr1} in series with R_2+R_{dr3} where V_{in4} is tapped off at the center.

Approaches to Reducing Crosstalk

1. Increase inter-wire spacing (decrease C_C)
2. Decrease field-oxide thickness (decrease C_C/C_2)

   …but this loads the driven nodes and thus decreases circuit speed.
3. Place ground lines (or V_{DD} lines) between signal lines