Lecture #17 (cont'd from #16)

OUTLINE

- MOSFET I_D *vs.* V_{GS} characteristic
- Circuit models for the MOSFET
  - resistive switch model
  - small-signal model

Reading

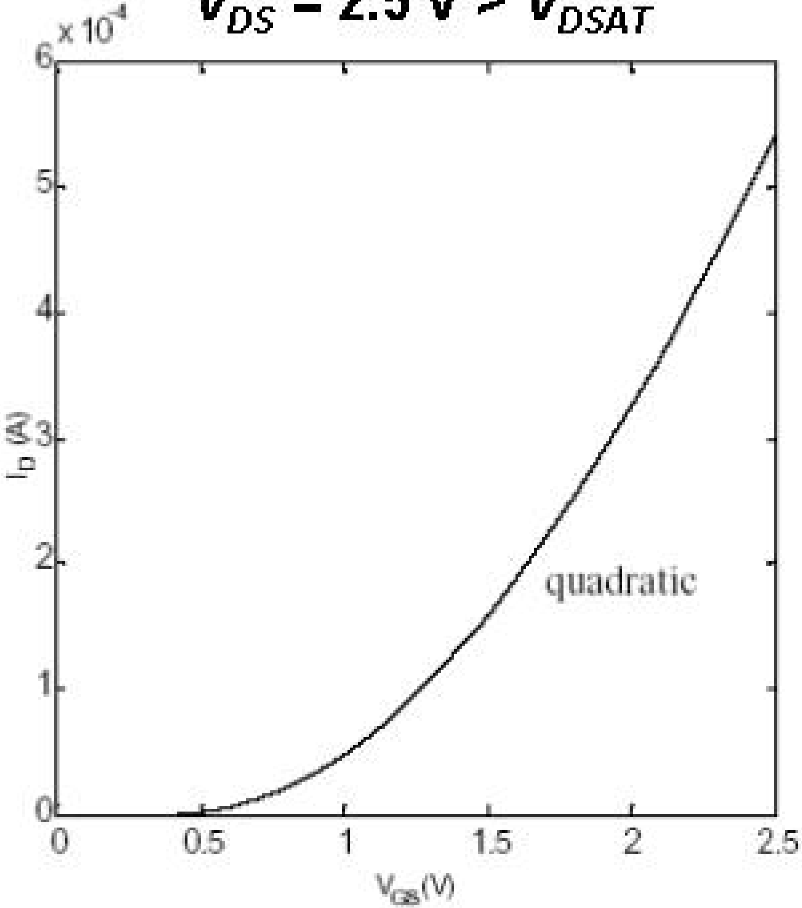
- **Rabaey *et al.*:** Chapter 3.3.2
- ***Hambley*:** Chapter 12 (through 12.5)

MOSFET I_D vs. V_{GS} Characteristic

- Typically, V_{DS} is fixed when I_D is plotted as a function of V_{GS}

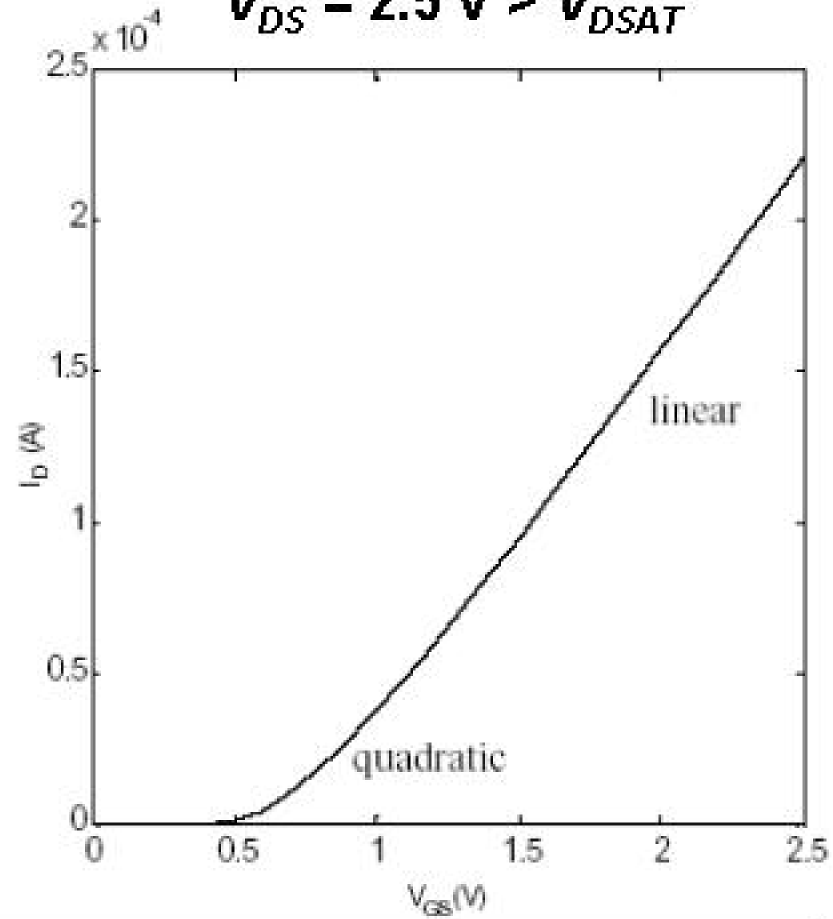
Long-channel MOSFET

$V_{DS} = 2.5\ V > V_{DSAT}$



Short-channel MOSFET

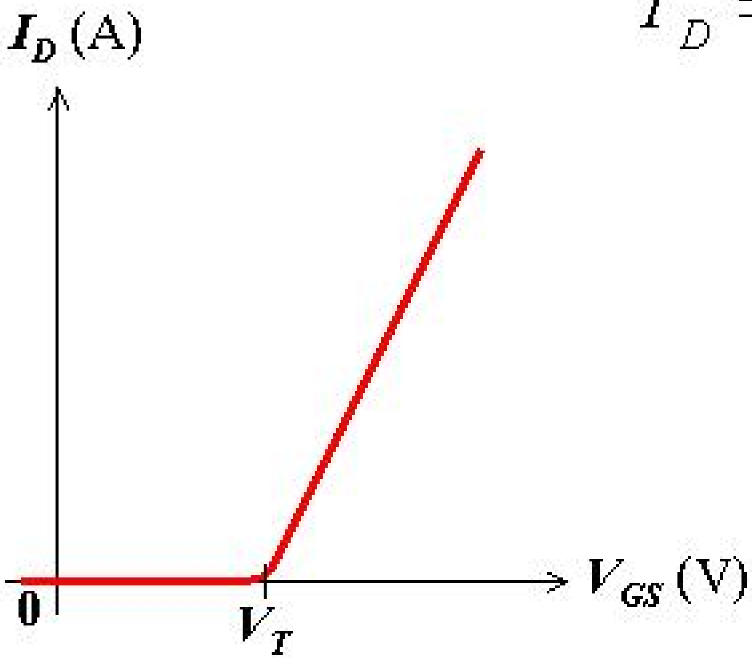
$V_{DS} = 2.5\ V > V_{DSAT}$



MOSFET V_T Measurement

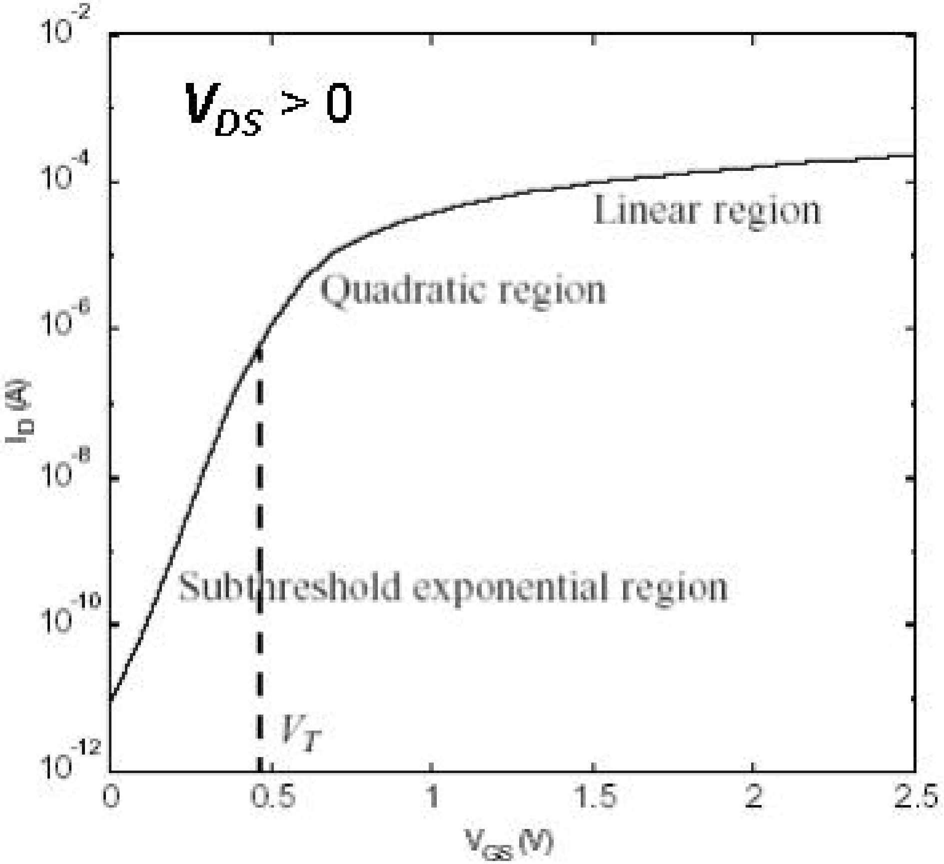
- V_T can be determined by plotting I_D vs. V_{GS}, using a low value of V_{DS} :

$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$



Subthreshold Conduction (Leakage Current)

- The transition from the ON state to the OFF state is gradual. This can be seen more clearly when I_D is plotted on a logarithmic scale:



- In the subthreshold ($V_{GS} < V_T$) region,

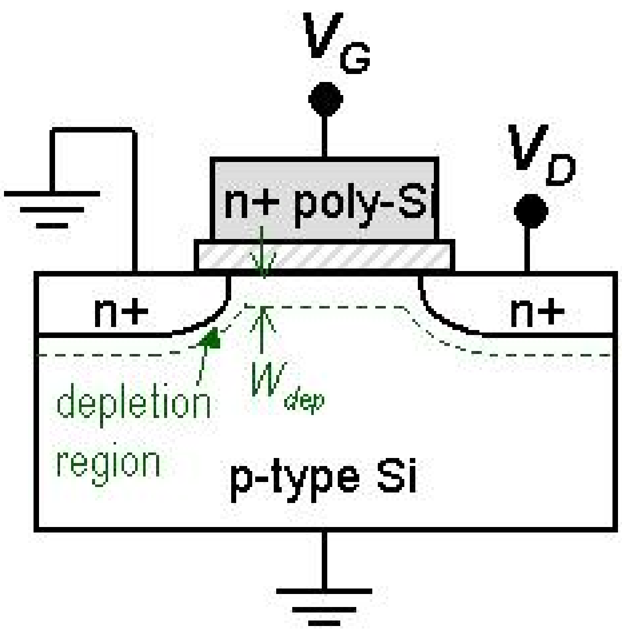
$$I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$$

This is essentially the channel-source pn junction current.
(Some electrons diffuse from the source into the channel, if this pn junction is forward biased.)

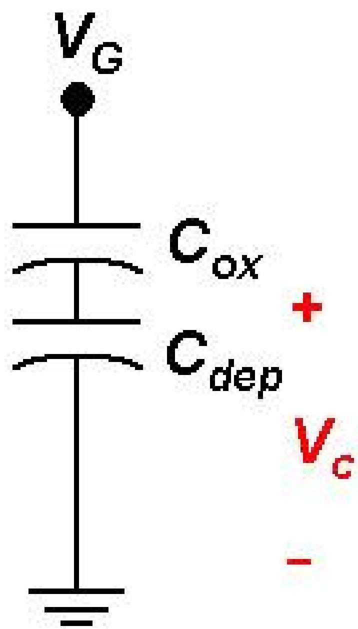
Qualitative Explanation for Subthreshold Leakage

- The channel V_c (at the Si surface) is capacitively coupled to the gate voltage V_G:

DEVICE



CIRCUIT MODEL



$$C_{dep} = \frac{\varepsilon_{Si}}{W_{dep}} \propto \sqrt{\frac{1}{N_A}}$$

Using the capacitive voltage divider formula:

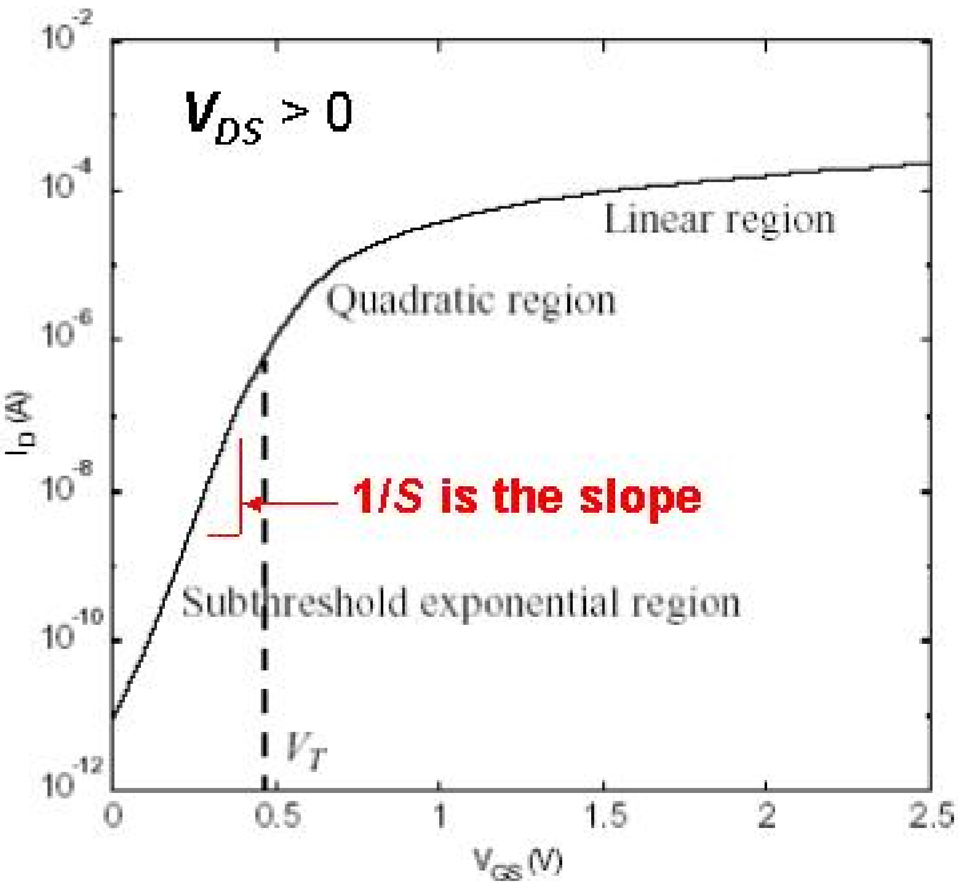
$$\Delta V_c = \frac{C_{ox}}{C_{ox} + C_{dep}} \Delta V_G$$

The forward bias on the channel-source pn junction increases with V_G scaled by the factor $C_{ox} / (C_{ox}+C_{dep})$

$$\Rightarrow n = \frac{C_{ox} + C_{dep}}{C_{ox}} = 1 + \frac{C_{dep}}{C_{ox}}$$

Slope Factor (or Subthreshold Swing) *S*

- ***S*** is defined to be the inverse slope of the log (I_D) *vs.* V_{GS} characteristic in the subthreshold region:



$$S \equiv n\left(\frac{kT}{q}\right)\ln(10)$$

Units: Volts per decade

Note that ***S*** ≥ 60 mV/dec at room temperature:

$$\left(\frac{kT}{q}\right)\ln(10) = 60\,\text{mV}$$

V_T Design Trade-Off

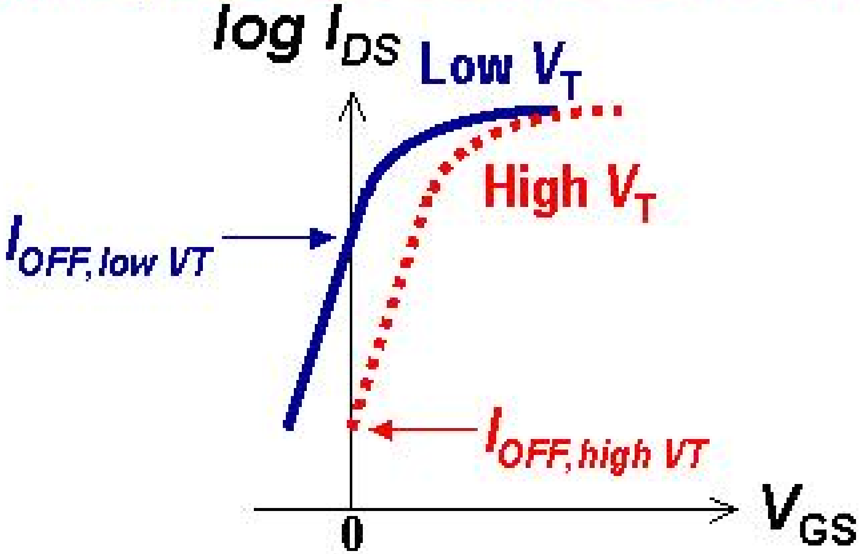
(Important consideration for digital-circuit applications)

- Low V_T is desirable for high ON current

$$I_{DSAT} \propto (V_{DD} - V_T)^{\eta} \qquad 1 < \eta < 2$$

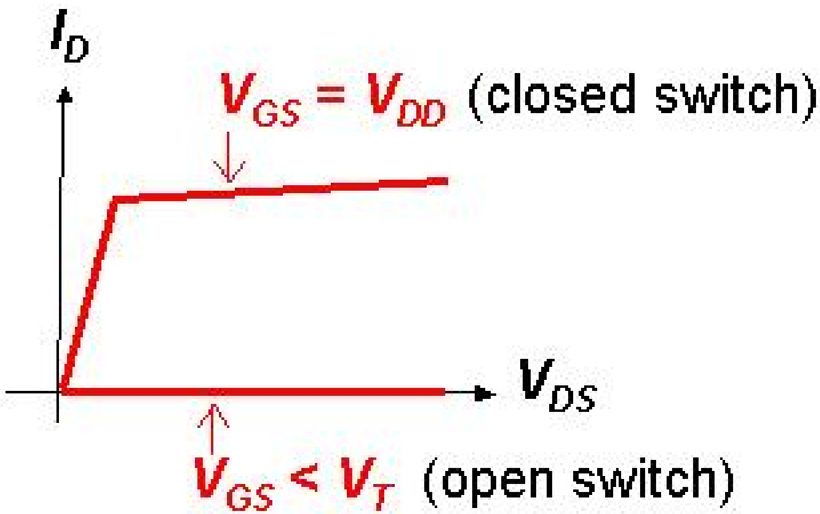
where V_{DD} is the power-supply voltage

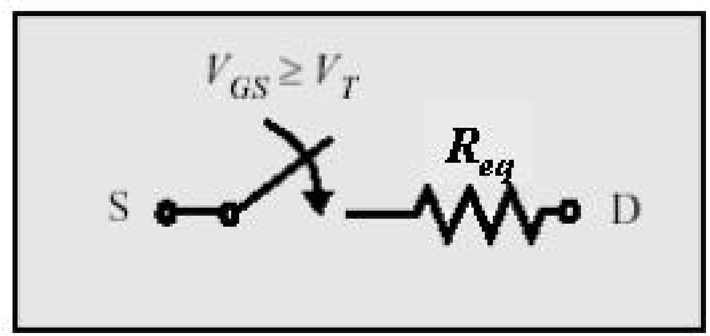
...but high V_T is needed for low OFF current



The MOSFET as a Resistive Switch

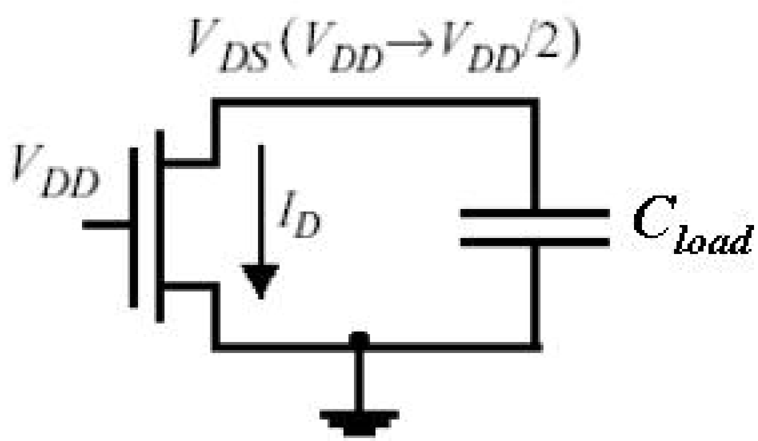
- For digital circuit applications, the MOSFET is either OFF ($V_{GS} < V_T$) or ON ($V_{GS} = V_{DD}$). Thus, we only need to consider two I_D vs. V_{DS} curves:
  1. the curve for $V_{GS} < V_T$
  2. the curve for $V_{GS} = V_{DD}$





Equivalent Resistance R_{eq}

- In a digital circuit, an n-channel MOSFET in the ON state is typically used to discharge a capacitor connected to its drain terminal:
  - gate voltage $V_G = V_{DD}$
  - source voltage V_S = 0 V
  - drain voltage V_D initially at V_{DD}, discharging toward 0 V



The value of R_{eq} should be set to the value which gives the correct propagation delay (time required for output to fall to ½V_{DD}):

$$I_{DSATn} = \frac{k'_n}{2}\frac{W}{L}\left(V_{DD} - V_{Tn}\right)^2 \longrightarrow$$

$$R_{eq} \cong \frac{3}{4}\frac{V_{DD}}{I_{DSATn}}\left(1 - \frac{5}{6}\lambda_n V_{DD}\right)$$

Typical MOSFET Parameter Values

- For a given MOSFET fabrication process technology, the following parameters are known:
  - V_T (~0.5 V)
  - C_{ox} and k' (<0.001 A/V^2)
  - V_{DSAT} ($\leq$ 1 V)
  - λ ($\leq$ 0.1 V^{-1})

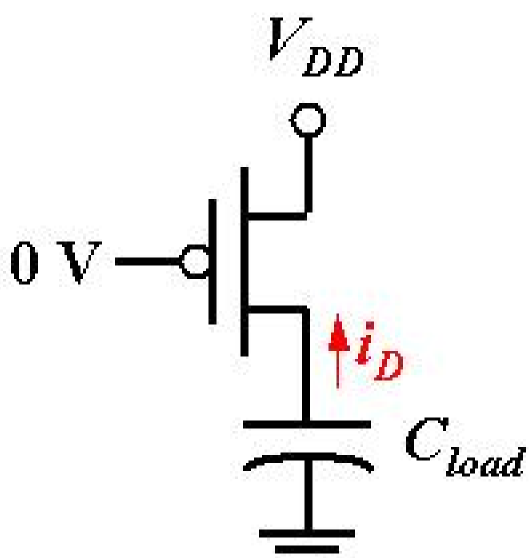
Example R_{eq} values for 0.25 μm technology (***W*** = ***L***):

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

How can R_{eq} be decreased?

P-Channel MOSFET Example

- In a digital circuit, a p-channel MOSFET in the ON state is typically used to charge a capacitor connected to its drain terminal:
  - gate voltage V_G = **0 V**
  - source voltage V_S = V_{DD} (power-supply voltage)
  - drain voltage V_D initially at **0 V**, charging toward V_{DD}



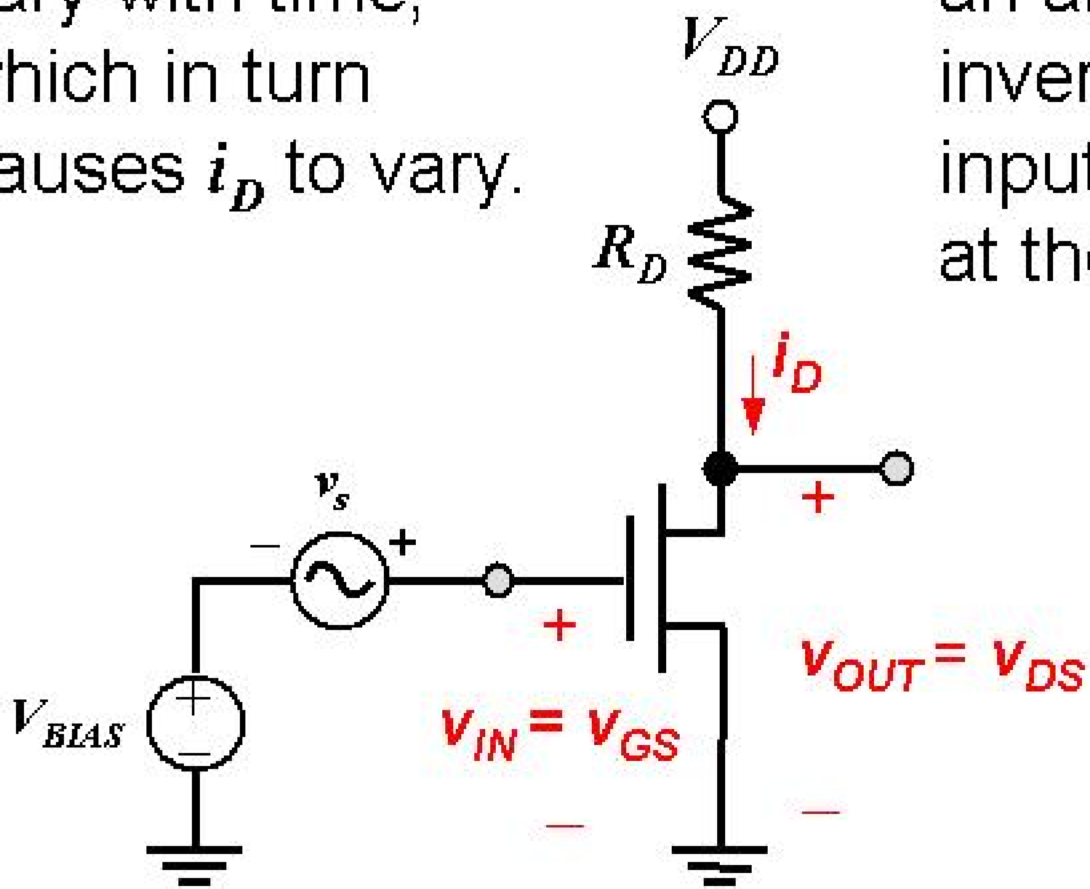
$$R_{eq} \cong \frac{3}{4} \frac{V_{DD}}{\left|I_{DSATp}\right|}\left(1-\frac{5}{6}\lambda_p V_{DD}\right)$$

$$I_{DSAT} = -\frac{k_p'}{2}\frac{W}{L}\left(V_{DD}-\left|V_{Tp}\right|\right)^2$$

Common-Source (CS) Amplifier

- The input voltage v_s causes v_{GS} to vary with time, which in turn causes i_D to vary.

- The changing voltage drop across R_D causes an amplified (and inverted) version of the input signal to appear at the drain terminal.



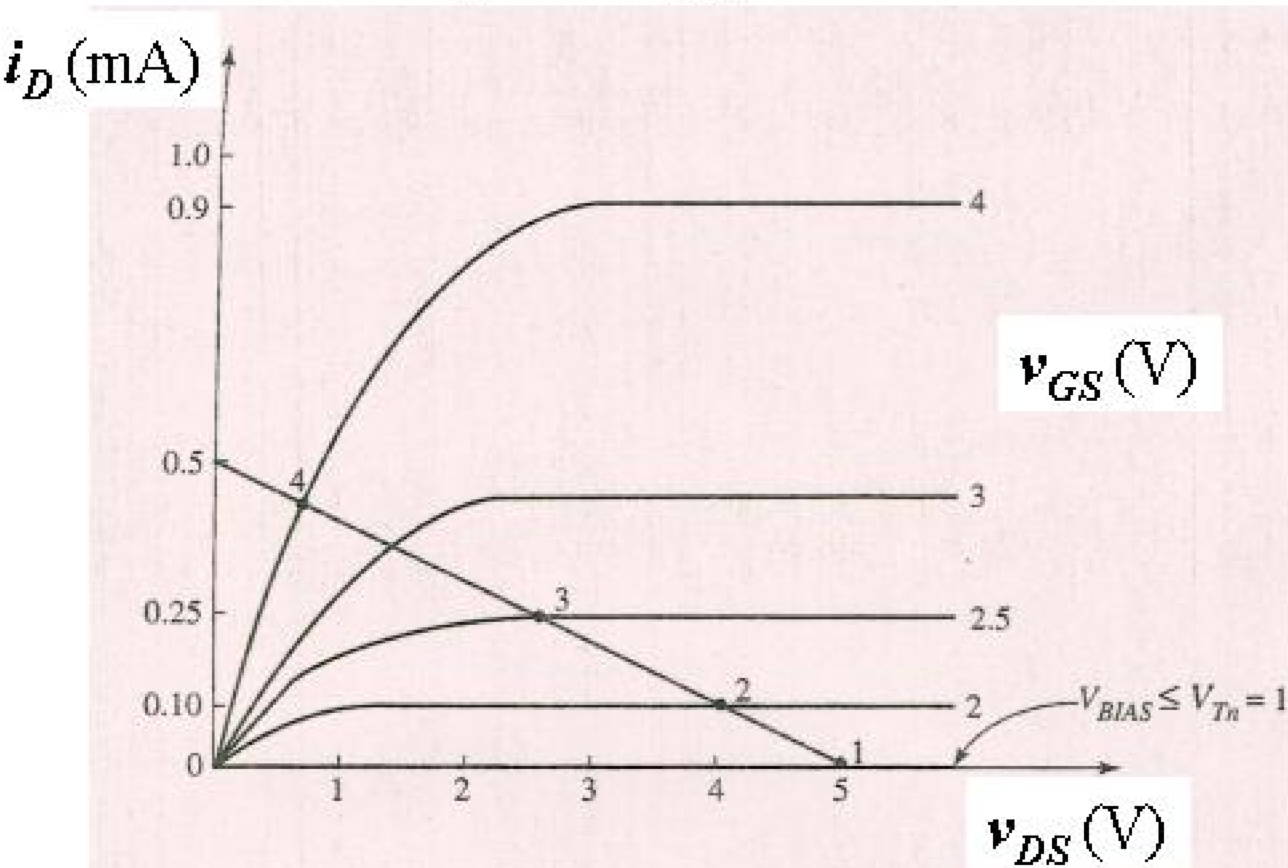
Notation

- Subscript convention:
  - $V_{DS} \equiv V_D - V_S$, $V_{GS} \equiv V_G - V_S$, *etc.*
- Double-subscripts denote DC sources:
  - V_{DD} , V_{CC} , I_{SS} , *etc.*
- To distinguish between DC and incremental components of an electrical quantity, the following convention is used:
  - DC quantity: upper-case letter with upper-case subscript
    - I_D , V_{DS} , *etc.*
  - Incremental quantity: lower-case letter with lower-case subscript
    - i_d , v_{ds} , *etc.*
  - Total (DC + incremental) quantity:

    lower-case letter with upper-case subscript
    - i_D , v_{DS} , *etc.*

Load-Line Analysis of CS Amplifier

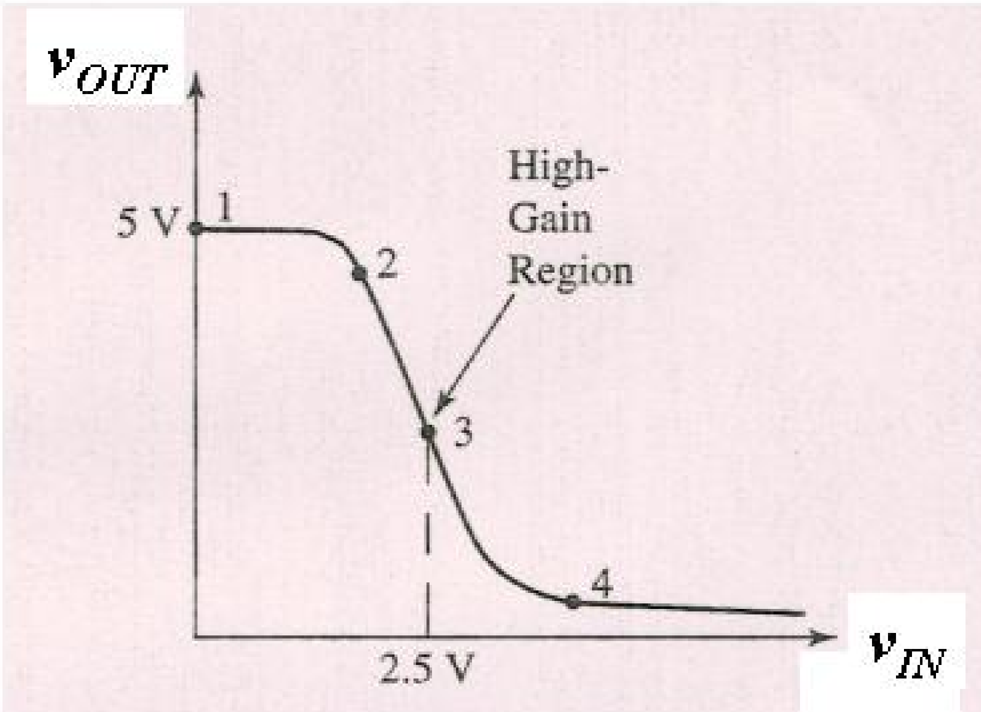
- The operating point of the circuit can be determined by finding the intersection of the appropriate MOSFET i_D vs. v_{DS} characteristic and the load line:



load-line equation:

$$V_{DD} = R_D i_D + v_{DS}$$

Voltage Transfer Function



<u>Goal</u>:
Operate the amplifier in the high-gain region, so that small changes in $\boldsymbol{v_{IN}}$ result in large changes in $\boldsymbol{v_{OUT}}$

(1): transistor biased in cutoff region

(2): $v_{IN} > V_T$; transistor biased in saturation region

(3): transistor biased in saturation region

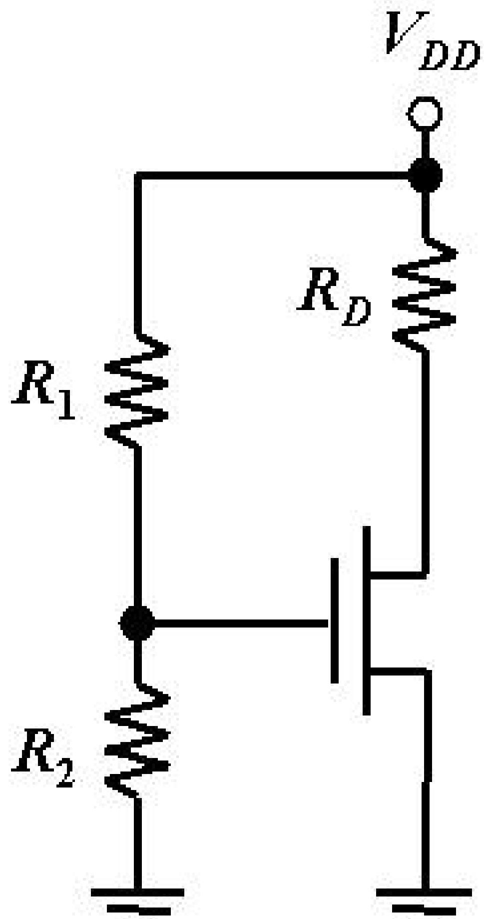
(4): transistor biased in "resistive" or "triode" region

Quiescent Operating Point

- The operating point of the amplifier for zero input signal (v_s = 0) is often referred to as the ***quiescent operating point.*** (Another word: ***bias***.)
  - The bias point should be chosen so that the output voltage is approximately centered between V_{DD} and 0 V.
  - v_s varies the input voltage around the input bias point.

Note: The relationship between v_{OUT} and v_{IN} is not linear; this can result in a distorted output voltage signal. If the input signal amplitude is very small, however, we can have amplification with negligible distortion.

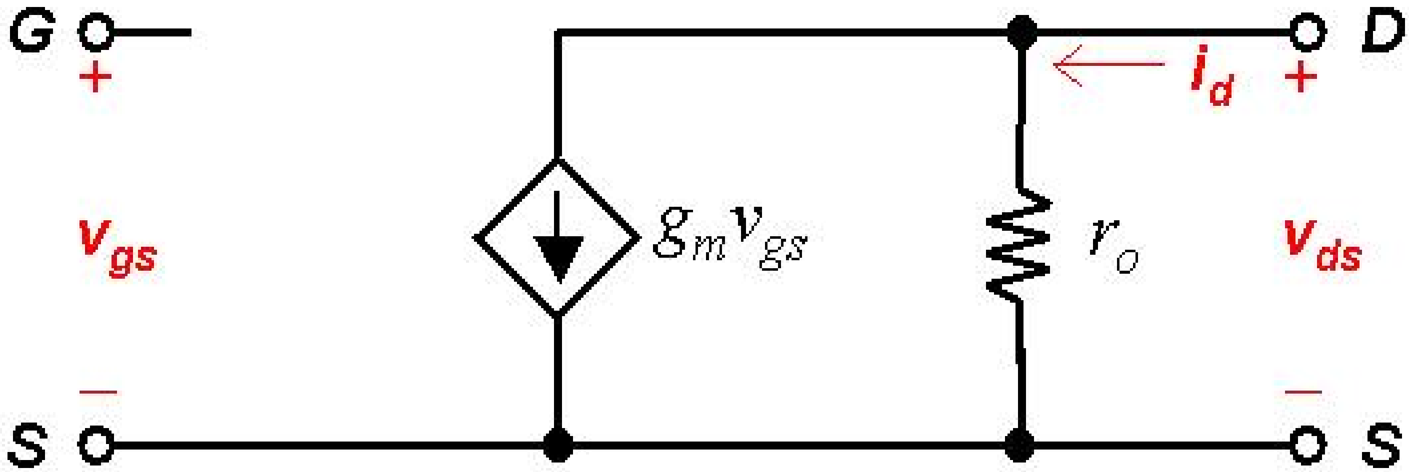
Bias Circuit Example



Rules for Small-Signal Analysis

- A DC supply voltage source acts as a short circuit
  - Even if AC current flows through the DC voltage source, the AC voltage across it is zero.
- A DC supply current source acts as an open circuit
  - Even if AC voltage is applied across the current source, the AC current through it is zero.

NMOSFET Small-Signal Model

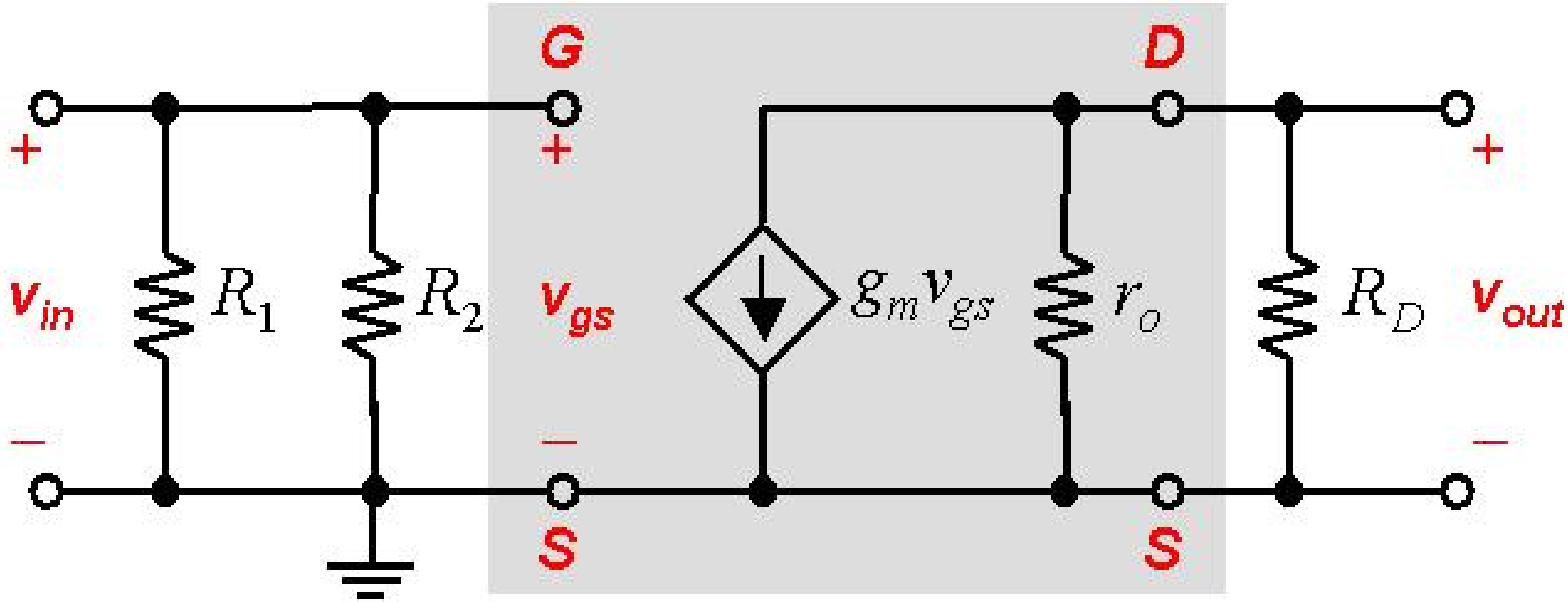


$$i_d = \frac{\partial i_D}{\partial v_{GS}} v_{gs} + \frac{\partial i_D}{\partial v_{DS}} v_{ds} = g_m v_{gs} + g_o v_{ds}$$

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \cong \frac{W}{L} k' \left(V_{GS} - V_T\right)$$ ***transconductance***

$$g_o \equiv \frac{\partial i_D}{\partial v_{DS}} \cong \lambda I_D$$ ***output conductance***

Small-Signal Equivalent Circuit



$$v_{out} = -g_m v_{gs} \left(r_o \parallel R_D \right)$$

voltage gain $$A_v = \frac{v_{out}}{v_{in}} = -g_m \left(r_o \parallel R_D \right)$$