Lecture #18

OUTLINE

• Continue small signal analysis
• Logic functions
• NMOS logic gates
• The CMOS inverter

Reading

• Rabaey et al.: Chapter 5.2
• Hambleley: Chapter 7.1-7.2
Digital Signals

- For a digital signal, the voltage must be within one of two ranges in order to be defined:

- Positive Logic:
  - “low” voltage ≡ logic state 0
  - “high” voltage ≡ logic state 1
### Logic Functions, Symbols, & Notation

<table>
<thead>
<tr>
<th>NAME</th>
<th>SYMBOL</th>
<th>NOTATION</th>
<th>TRUTH TABLE</th>
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</thead>
<tbody>
<tr>
<td>“NOT”</td>
<td><img src="image" alt="Not Symbol" /></td>
<td>$F = \overline{A}$</td>
<td><img src="image" alt="Truth Table" /></td>
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<tr>
<td>“OR”</td>
<td><img src="image" alt="Or Symbol" /></td>
<td>$F = A + B$</td>
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<td>“AND”</td>
<td><img src="image" alt="And Symbol" /></td>
<td>$F = A \cdot B$</td>
<td><img src="image" alt="Truth Table" /></td>
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**NOR**

\[ F = \overline{A + B} \]

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<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
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<tr>
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**NAND**

\[ F = \overline{A \cdot B} \]

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**XOR** (exclusive OR)

\[ F = A \oplus B \]

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NMOS Inverter ("NOT" Gate)

Circuit:

\[ V_{DD} \]
\[ R_D \]
\[ i_D \]
\[ V_{IN} \]
\[ V_{DS} = V_{OUT} \]
\[ V_{DD} \]
\[ V_{DS} \]

Voltage-Transfer Characteristic

\[ V_{IN} = V_{DD} \]

Increasing
\[ V_{GS} = V_{IN} > V_T \]

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Noise Margins

Definition of Input Levels

- Logic swing $V_{\text{sw}}$
- $V_{\text{OL}}$ to $V_{\text{OH}}$
- $V_{\text{IL}}$ to $V_{\text{IH}}$
- Slope $= -1$

Definition of Noise Margins

- Noise margin high $NM_H = V_{\text{OH}} - V_{\text{IH}}$
- Noise margin low $NM_L = V_{\text{IL}} - V_{\text{OL}}$

Gate output

Gate input

Undefined region

$V_{\text{OL}}$

$V_{\text{IL}}$

$V_{\text{IH}}$

$V_{\text{OH}}$
NMOS NAND Gate

- Output is low only if both inputs are high

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NMOS NOR Gate

- Output is low if either input is high

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Disadvantages of NMOS Logic Gates

• Large values of $R_D$ are required in order to
  - achieve a low value of $V_{OL}$
  - keep power consumption low

→ Large resistors are needed, but these take up a lot of space.

• One solution is to replace the resistor with an NMOSFET that is always on.
The CMOS Inverter: Intuitive Perspective

**CIRCUIT**

- $V_{IN}$
- $V_{OUT}$
- $V_{DD}$
- $G$
- $S$
- $D$

**SWITCH MODELS**

- $V_{DD}$
- $V_{OUT}$
- $V_{OL} = 0 \text{ V}$
- $V_{OH} = V_{DD}$
- $R_p$
- $R_n$

Low static power consumption, since one MOSFET is always off in steady state

$V_{IN} = V_{DD}$

$V_{IN} = 0 \text{ V}$
CMOS Inverter Voltage Transfer Characteristic

Diagram showing the voltage transfer characteristic of a CMOS inverter. The graph plots $V_{OUT}$ against $V_{IN}$ with $V_{DD}$ as the upper limit. The characteristic is divided into regions labeled A, B, C, D, and E, each with a different state (N: off, P: lin, N: sat, P: sat, N: lin, P: off) for the NMOS and PMOS transistors.

The diagram also includes a circuit representation of a CMOS inverter with terminals labeled $V_{IN}$ and $V_{OUT}$.
CMOS Inverter Load-Line Analysis

\[ V_{IN} = V_{DD} + V_{GSp} \]

\[ V_{OUT} = V_{DD} + V_{DSP} \]

Increasing \( V_{IN} \):
- \( V_{IN} = 0 \text{ V} \)
- \( V_{IN} = V_{DD} \)

Increasing \( V_{OUT} \):
- \( V_{DSP} = -V_{DD} \)
- \( V_{DSP} = 0 \)

\( I_{Dn} = -I_{DP} \)
CMOS Inverter Load-Line Analysis: Region A

\[ V_{IN} \leq V_{Tn} \]

\[ I_{Dn} = -I_{Dp} \]

\[ V_{OUT} = V_{DSn} \]

\[ V_{GSn} = V_{IN} - V_{DD} \]

\[ V_{DSn} = V_{OUT} - V_{DD} \]
CMOS Inverter Load-Line Analysis: Region B

\[ \frac{V_{DD}}{2} > V_{IN} > V_{Tn} \]

\[ I_{Dn} = -I_{Dp} \]

\[ V_{DSn} = V_{IN} - V_{DD} \]

\[ V_{DSn} = V_{OUT} - V_{DD} \]

\[ V_{OUT} = V_{DSn} \]
CMOS Inverter Load-Line Analysis: Region D

\[ V_{DD} - |V_{Tp}| > V_{IN} > V_{DD}/2 \]

\[ I_{Dn} = -I_{Dp} \]

\[ V_{DSn} = V_{DD} - V_{OUT} \]

\[ V_{GSp} = V_{IN} - V_{DD} \]
CMOS Inverter Load-Line Analysis: Region E

\[ V_{IN} > V_{DD} - |V_{Tp}| \]

\[ I_{Dn} = -I_{Dp} \]

\[ V_{DSn} = V_{OUT} - V_{DD} \]

\[ V_{OUT} = V_{DSn} \]