Lecture #18

OUTLINE

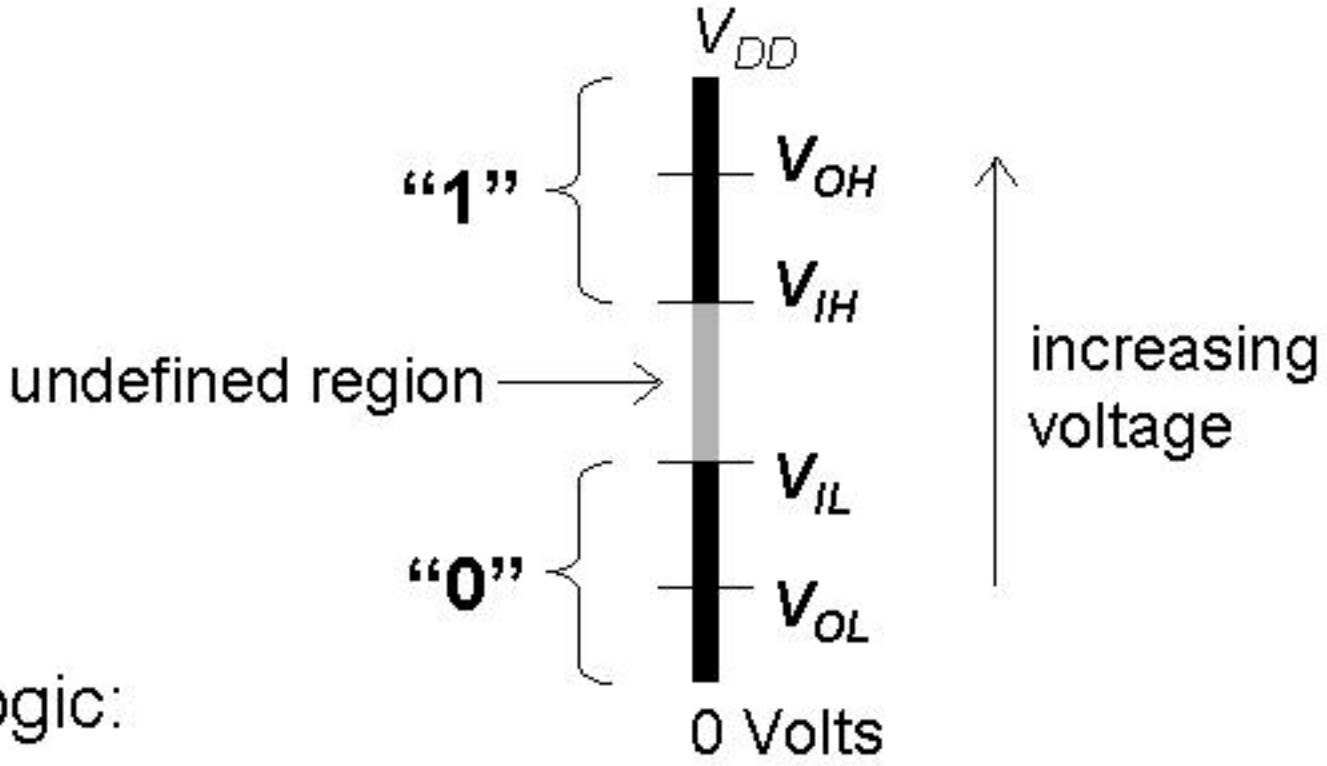
- Continue small signal analysis
- Logic functions
- NMOS logic gates
- The CMOS inverter

Reading

- Rabaey *et al.*: Chapter 5.2
- Hambley: Chapter 7.1-7.2

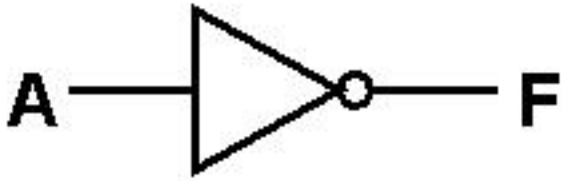
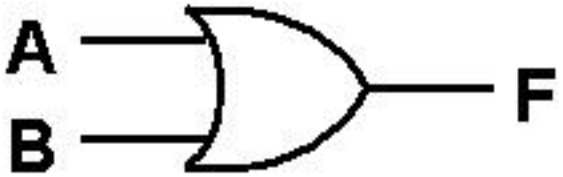
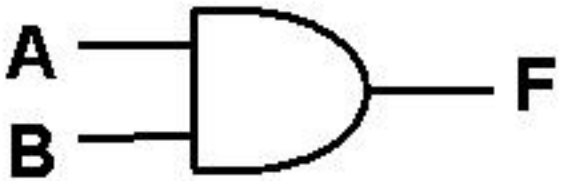
Digital Signals

- For a digital signal, the voltage must be within one of two ranges in order to be defined:



- Positive Logic:
  - "low" voltage ≡ logic state **0**
  - "high" voltage ≡ logic state **1**

Logic Functions, Symbols, & Notation

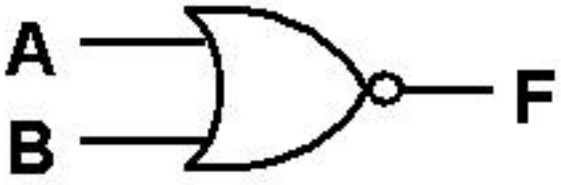
NAME	SYMBOL	NOTATION	TRUTH TABLE
"NOT"		$F = \overline{A}$	
"OR"		F = A+B	
"AND"		F = A•B	

A	F
0	1
1	0

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

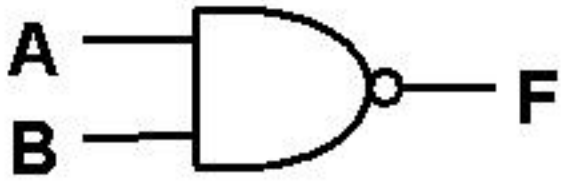
"NOR"



$F = \overline{A+B}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

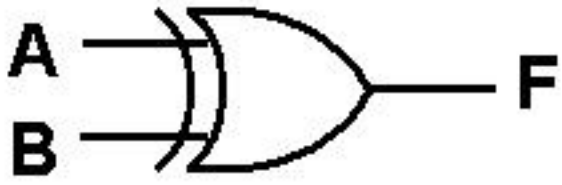
"NAND"



$F = \overline{A \cdot B}$

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

"XOR"
(exclusive OR)

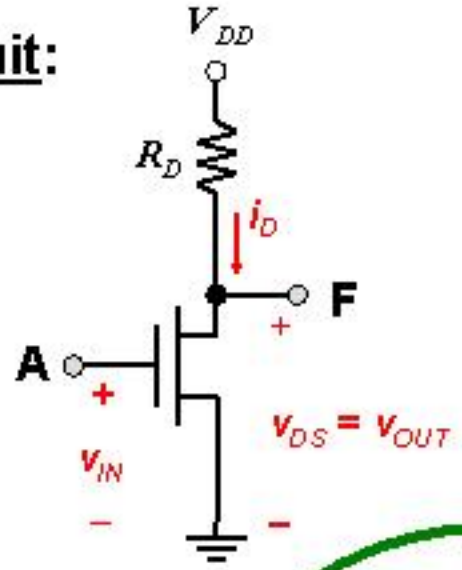


$F = A \oplus B$

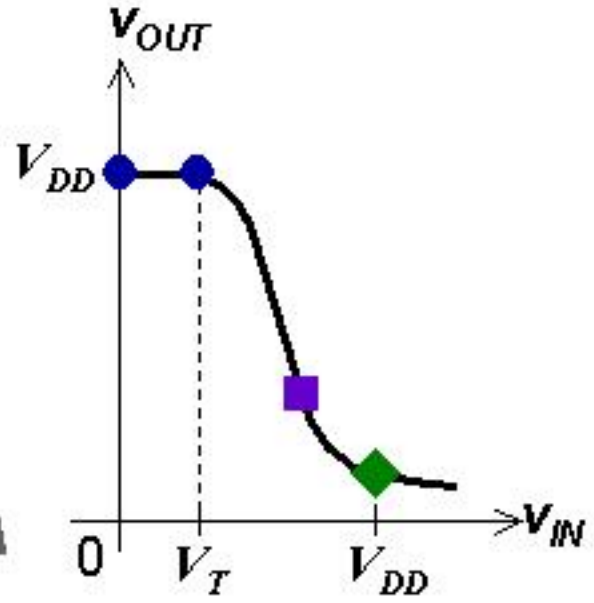
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

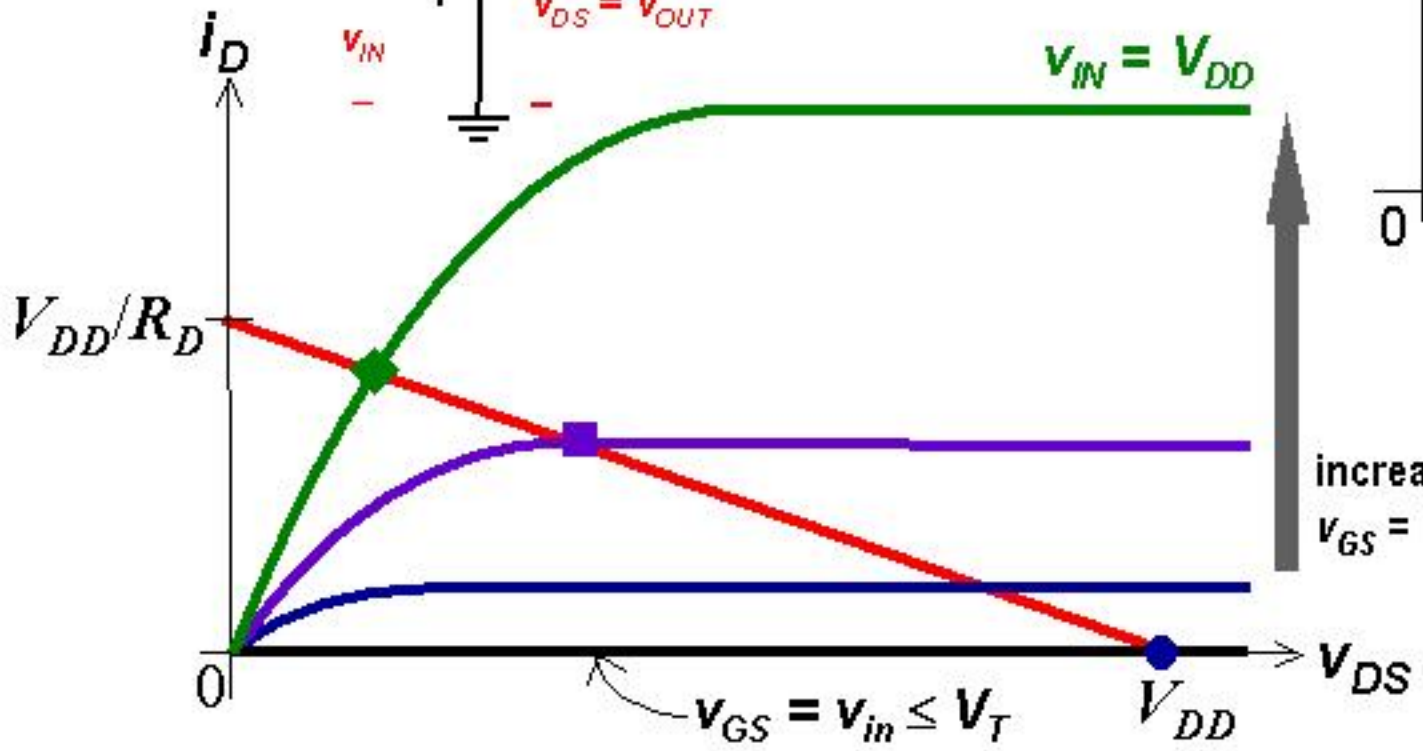
NMOS Inverter ("NOT" Gate)

Circuit:



Voltage-Transfer Characteristic

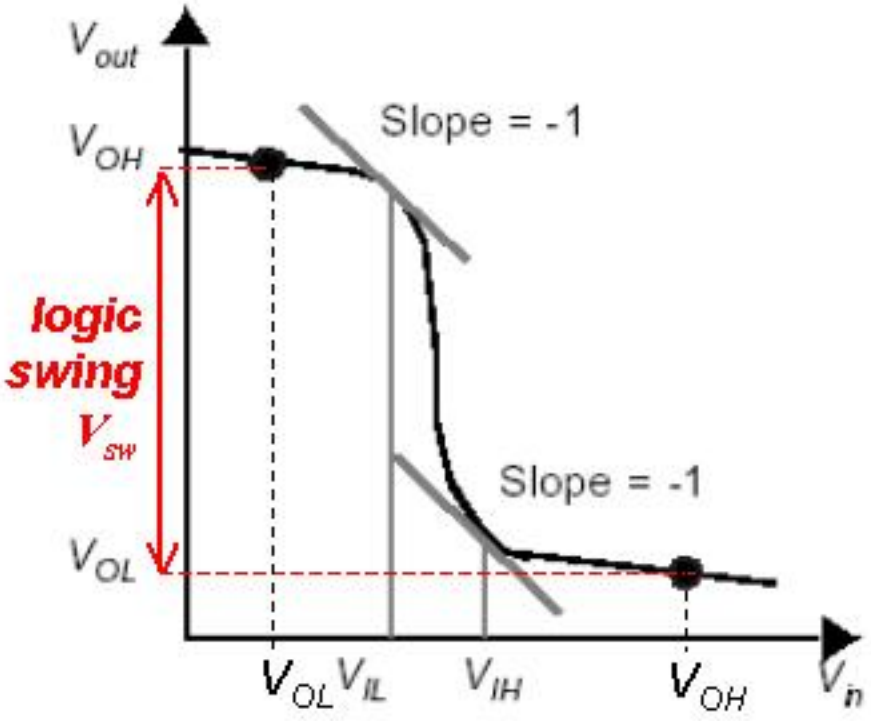




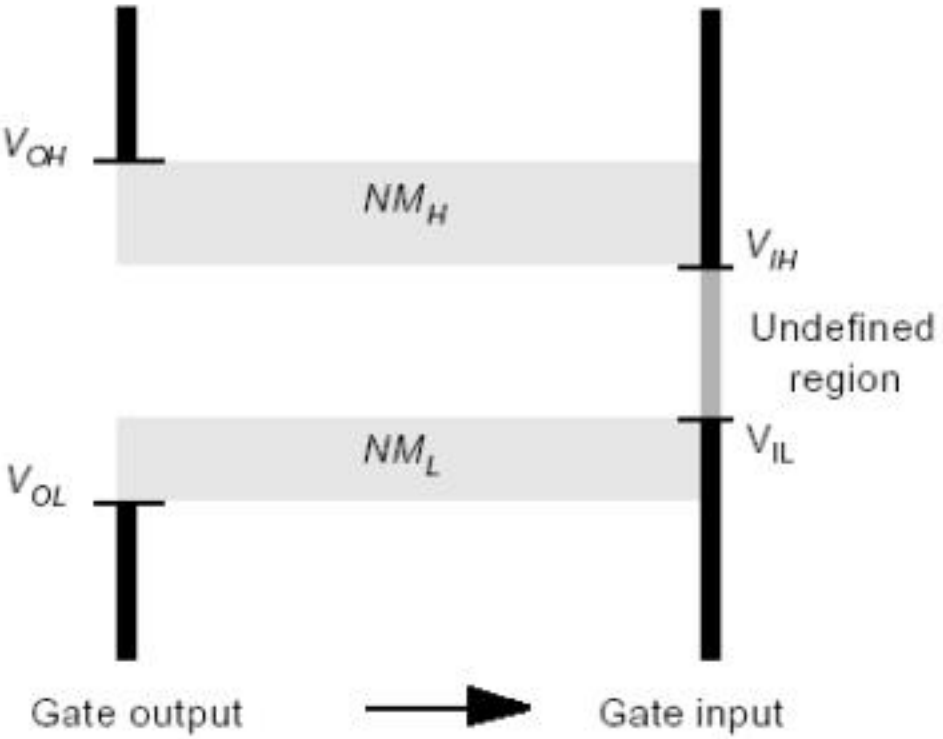
A	F
0	1
1	0

Noise Margins

Definition of Input Levels



Definition of Noise Margins

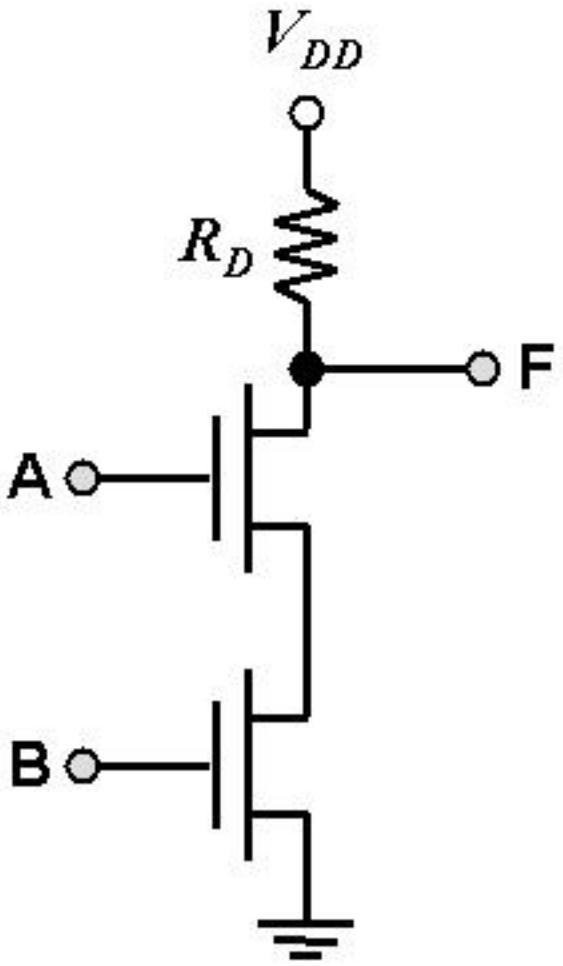


Noise margin high $NM_H = V_{OH} - V_{IH}$

Noise margin low $NM_L = V_{IL} - V_{OL}$

NMOS NAND Gate

- Output is low only if both inputs are high

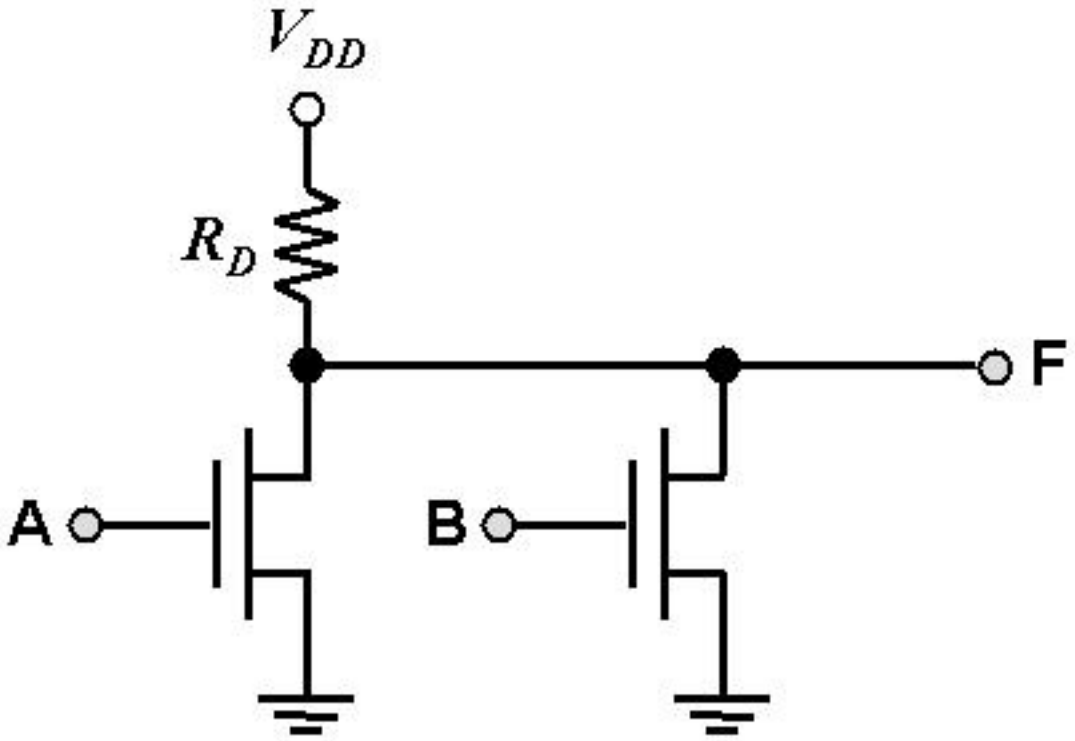


Truth Table

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

NMOS NOR Gate

- Output is low if either input is high



Truth Table

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Disadvantages of NMOS Logic Gates

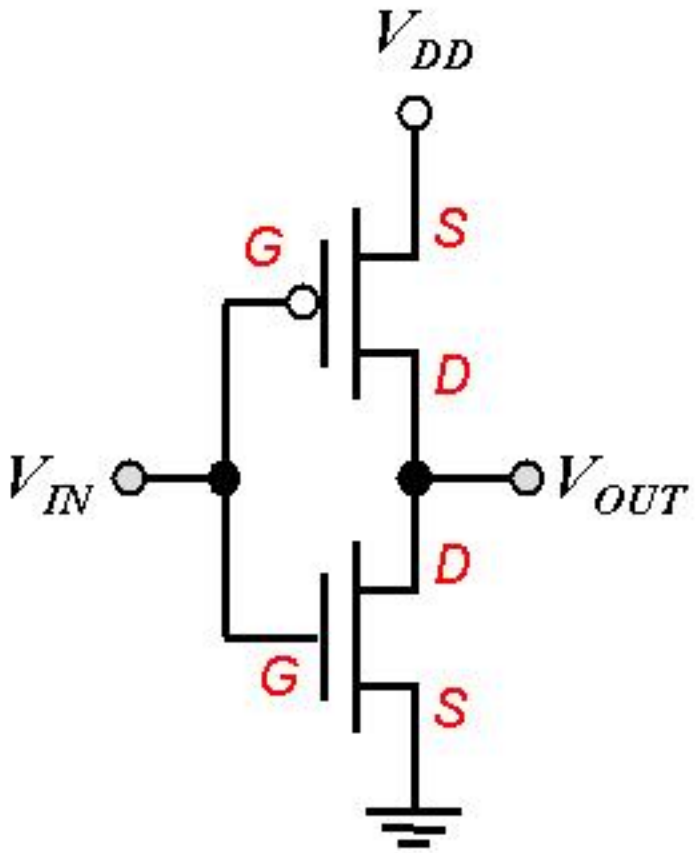
- Large values of R_D are required in order to
  - achieve a low value of V_{OL}
  - keep power consumption low

  → Large resistors are needed, but these take up a lot of space.

    - One solution is to replace the resistor with an NMOSFET that is always on.

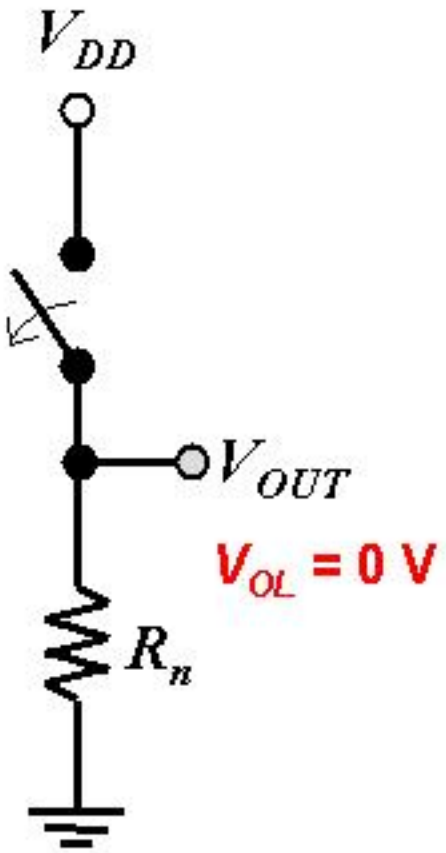
The CMOS Inverter: Intuitive Perspective

CIRCUIT

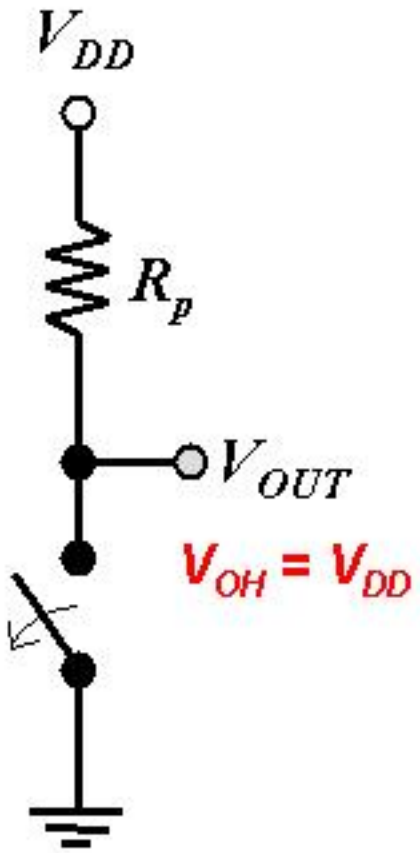


Low static power consumption, since one MOSFET is always off in steady state

SWITCH MODELS

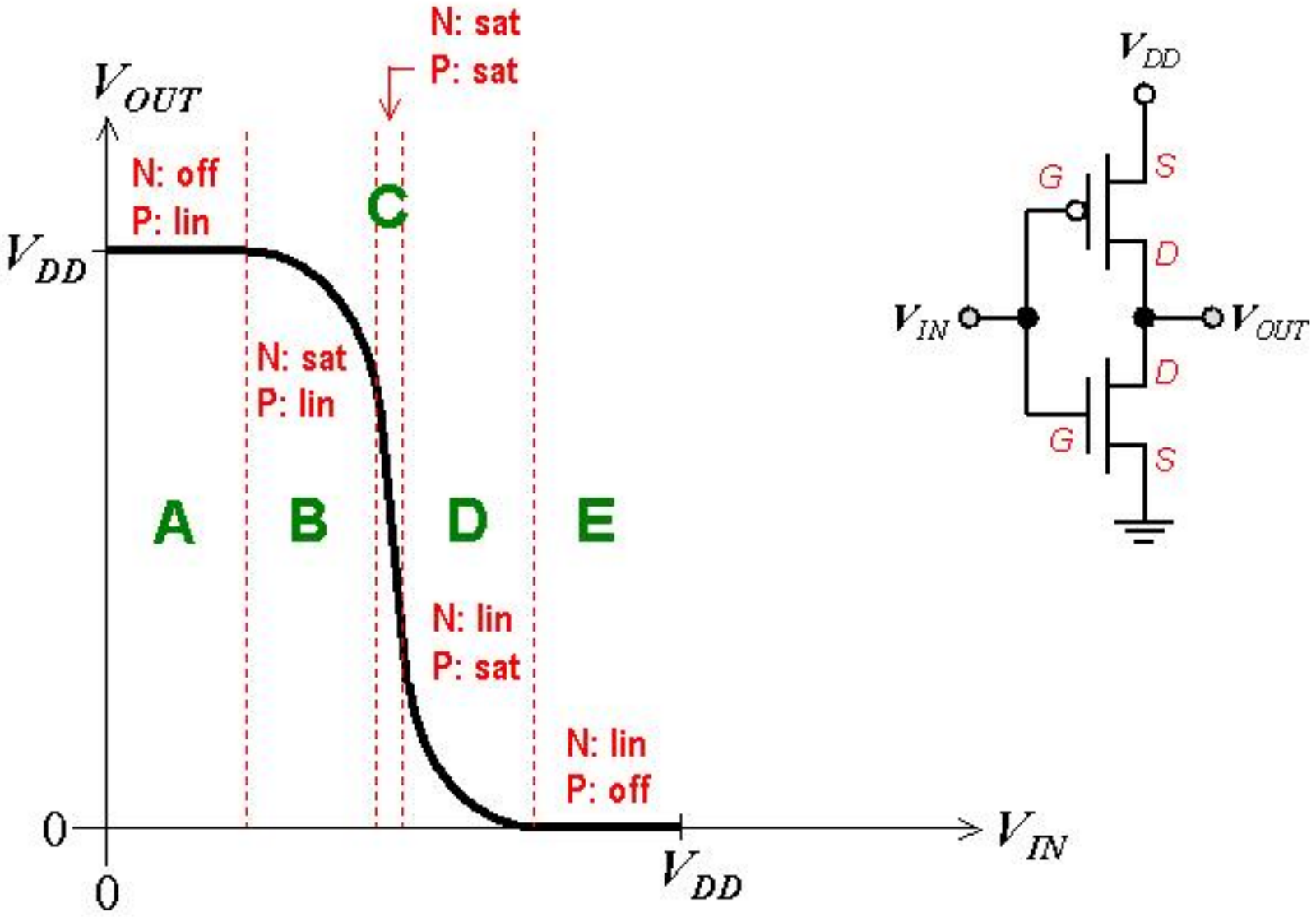


$V_{IN} = V_{DD}$



$V_{IN} = 0$ V

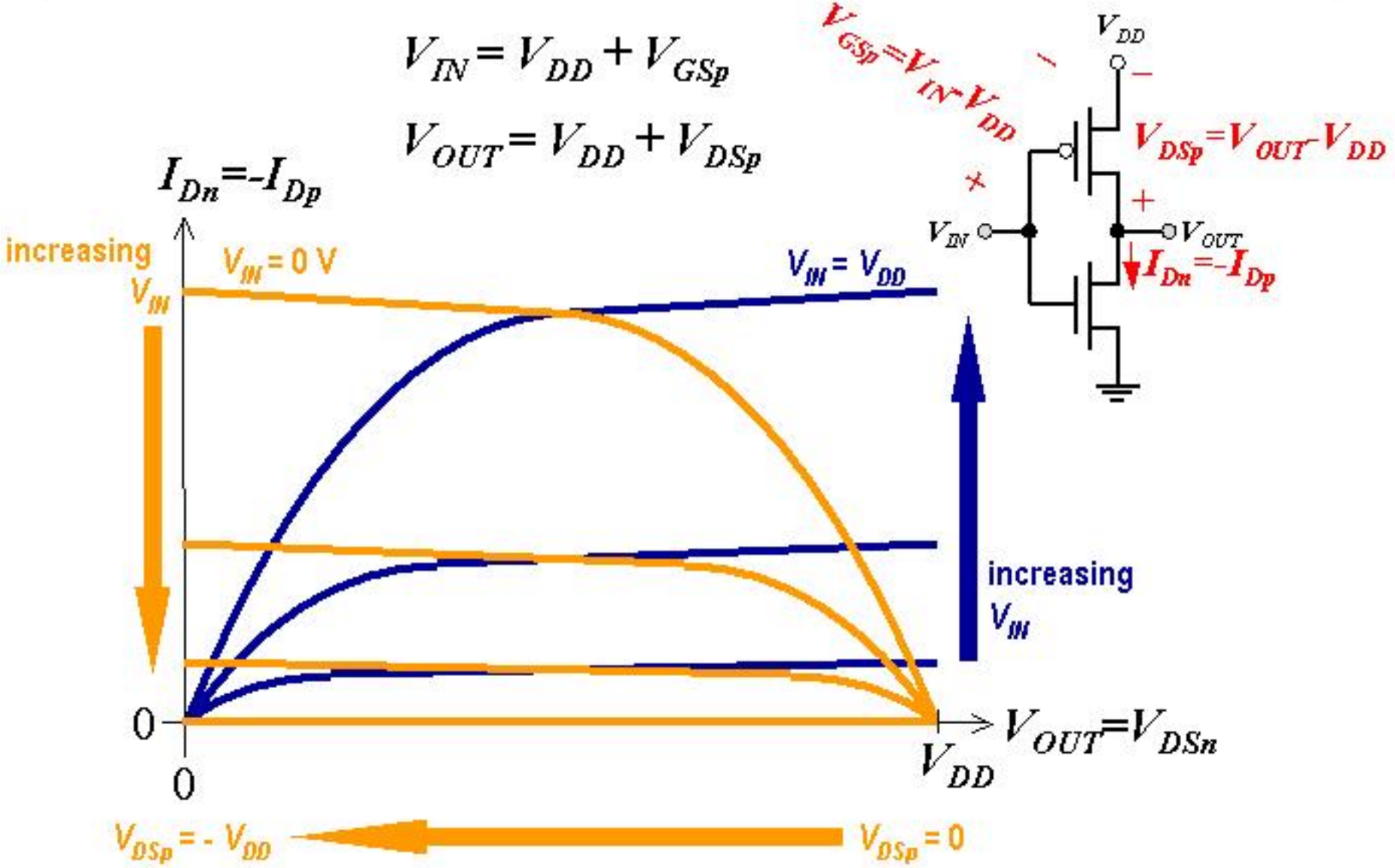
CMOS Inverter Voltage Transfer Characteristic



CMOS Inverter Load-Line Analysis

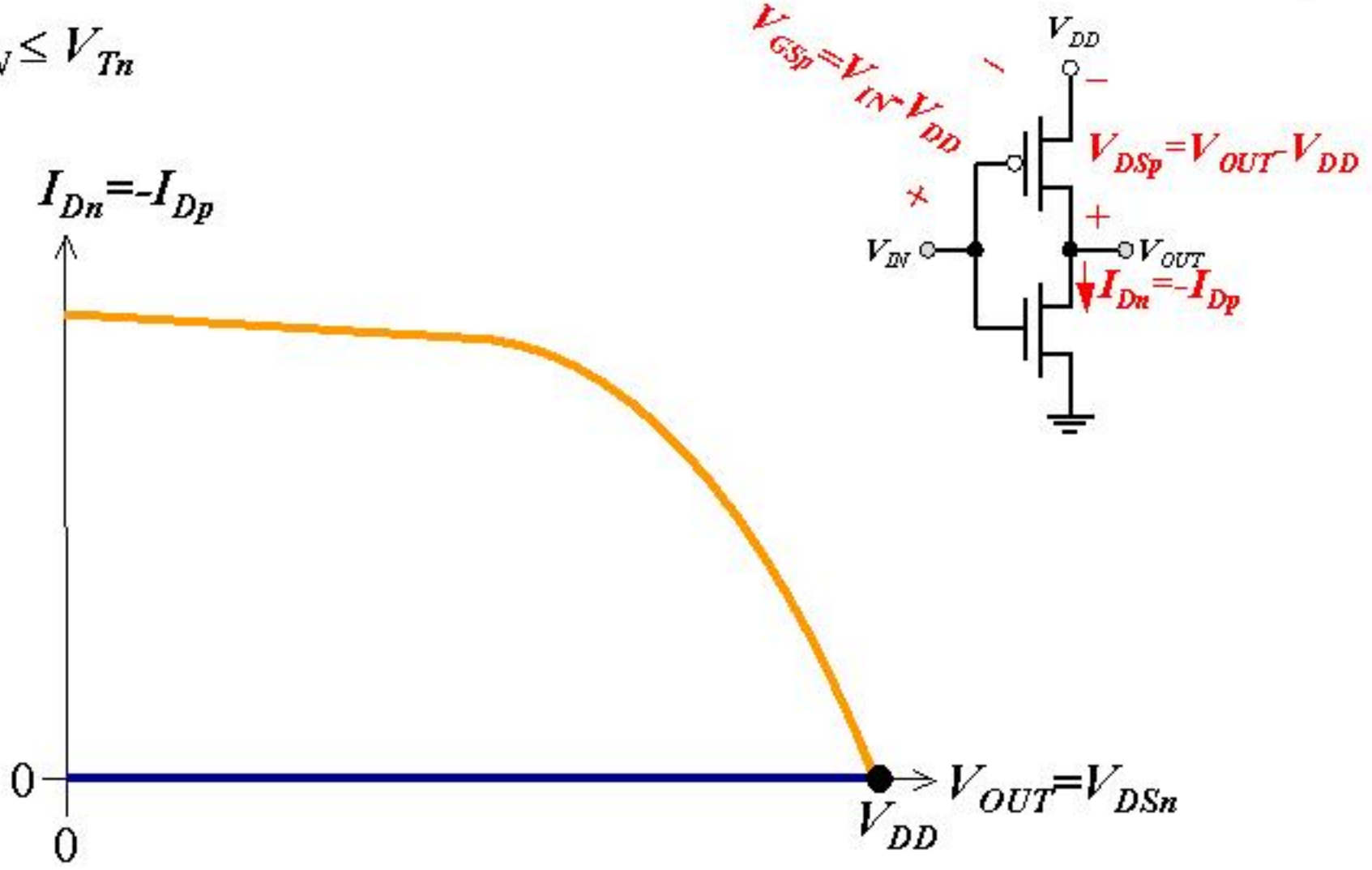
$$V_{IN} = V_{DD} + V_{GSp}$$

$$V_{OUT} = V_{DD} + V_{DSp}$$



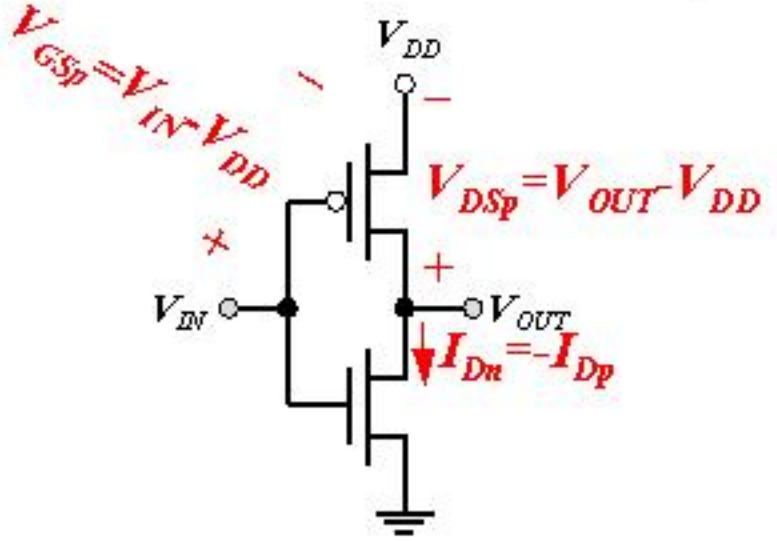
CMOS Inverter Load-Line Analysis: Region A

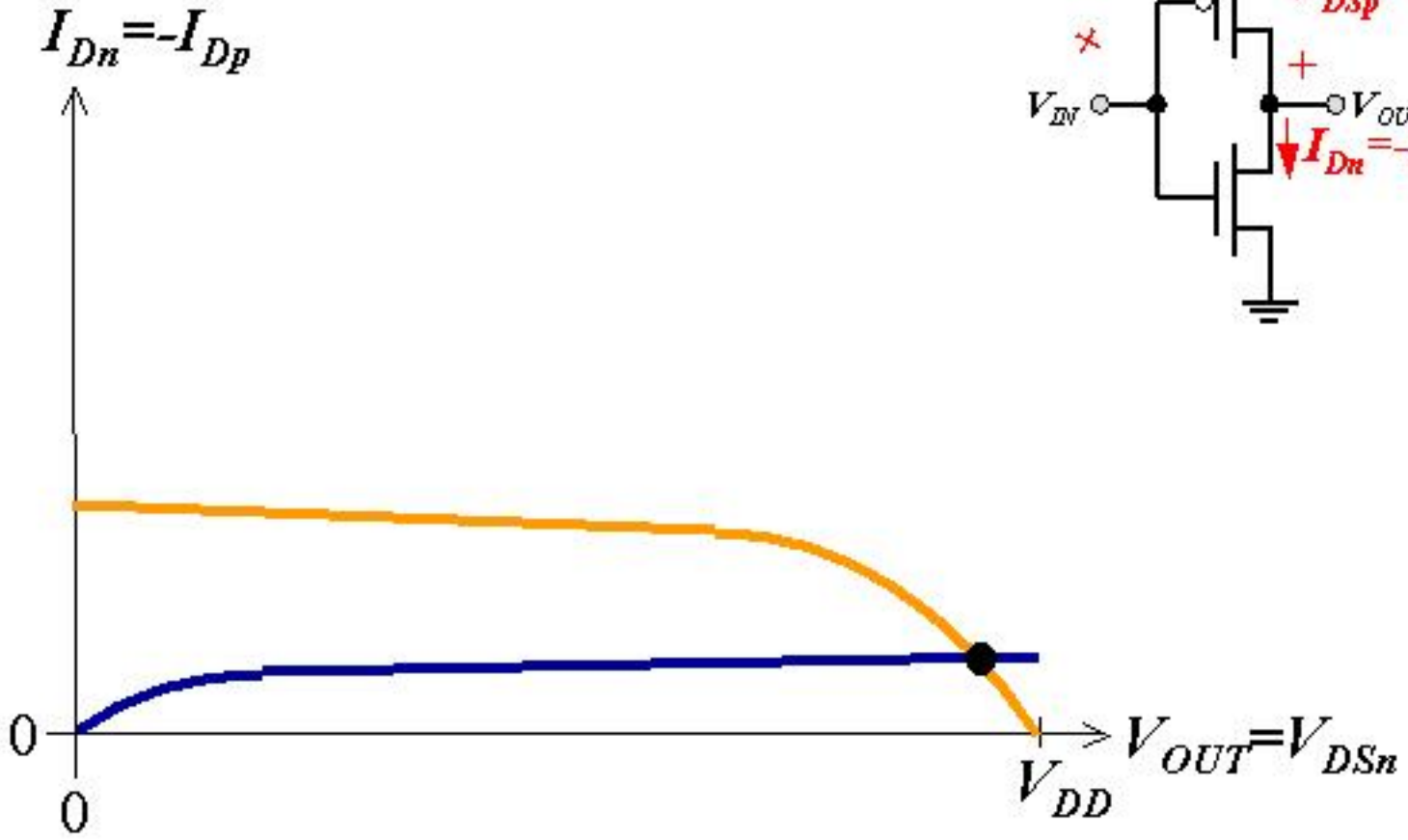
$V_{IN} \leq V_{Tn}$



CMOS Inverter Load-Line Analysis: Region B

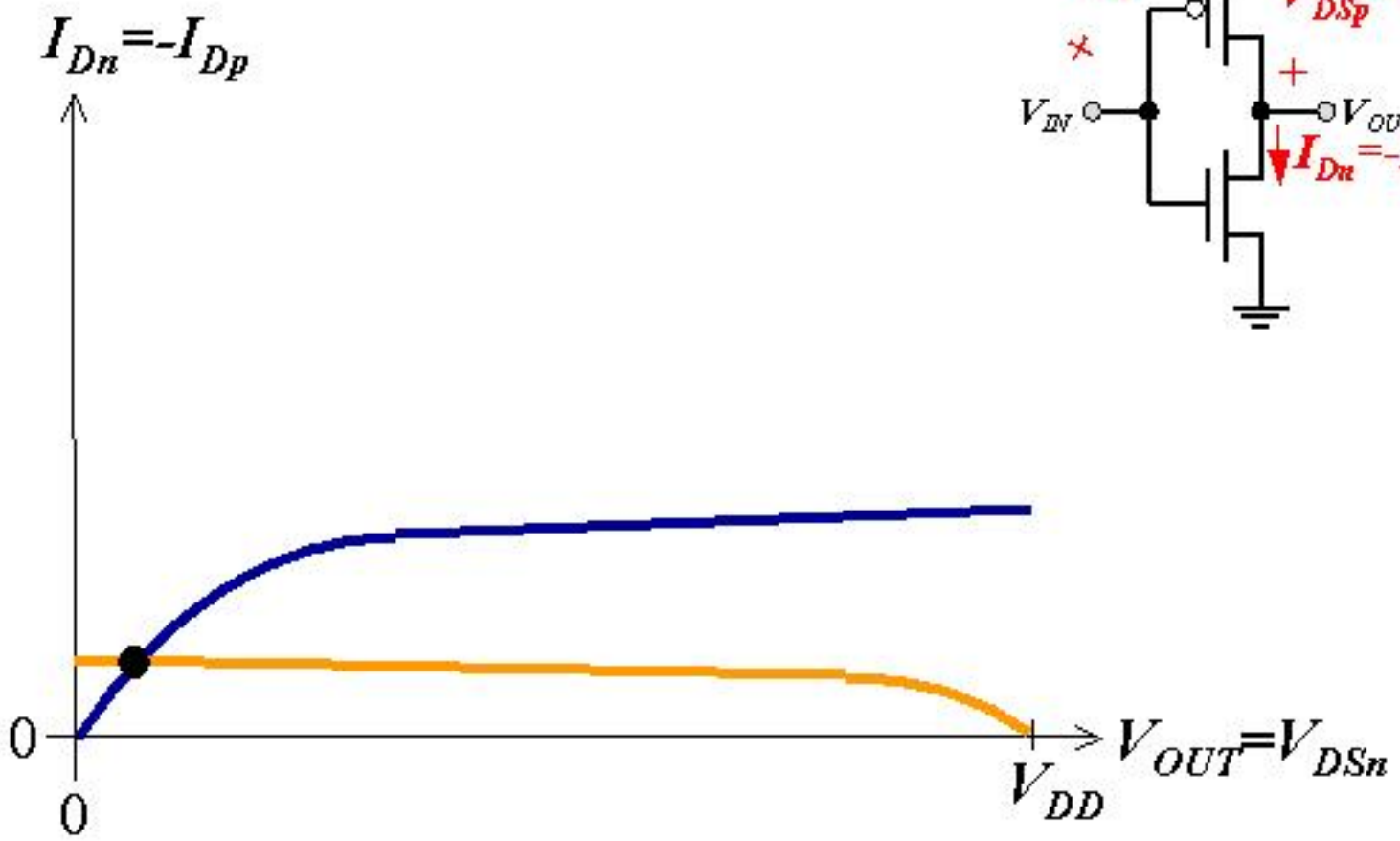
$V_{DD}/2 > V_{IN} > V_{Tn}$





CMOS Inverter Load-Line Analysis: Region D

$$V_{DD} - |V_{Tp}| > V_{IN} > V_{DD}/2$$



CMOS Inverter Load-Line Analysis: Region E

$V_{IN} > V_{DD} - |V_{Tp}|$