Lecture #19

ANNOUNCEMENTS

- Midterm 2 thurs. april 15, 9:40-11am.
- A-M initials in 10 Evans
- N-Z initials in Sibley auditorium
- Closed book, except for two 8.5 x 11 inch cheat sheets

OUTLINE

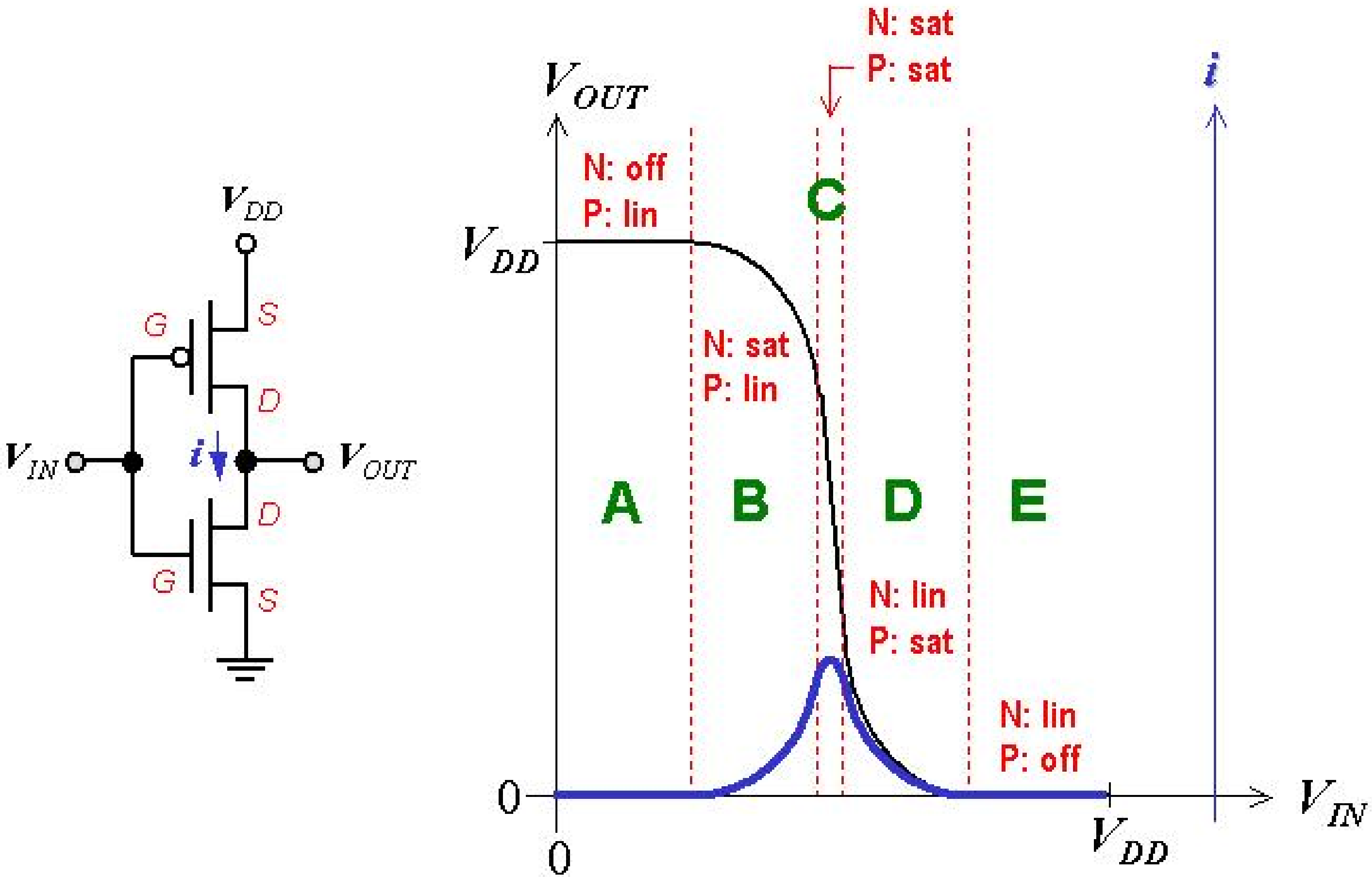
– The CMOS inverter (cont'd)
– CMOS logic gates
– The body effect

Reading (Rabaey *et al.*)
Chapter 5.5.1 (p.220); 6.2.1

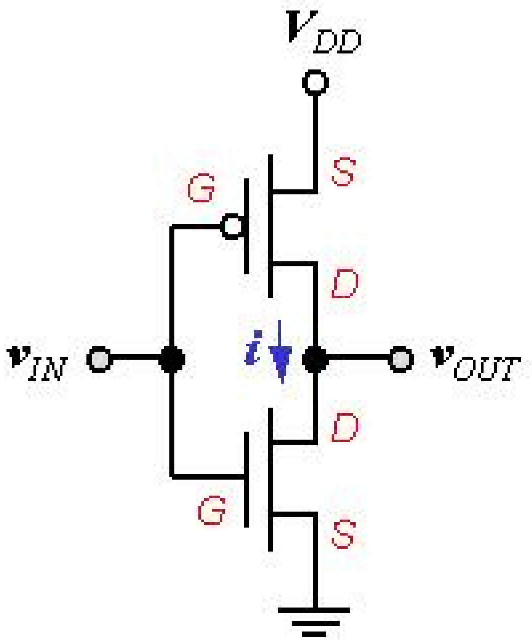
Features of CMOS Digital Circuits

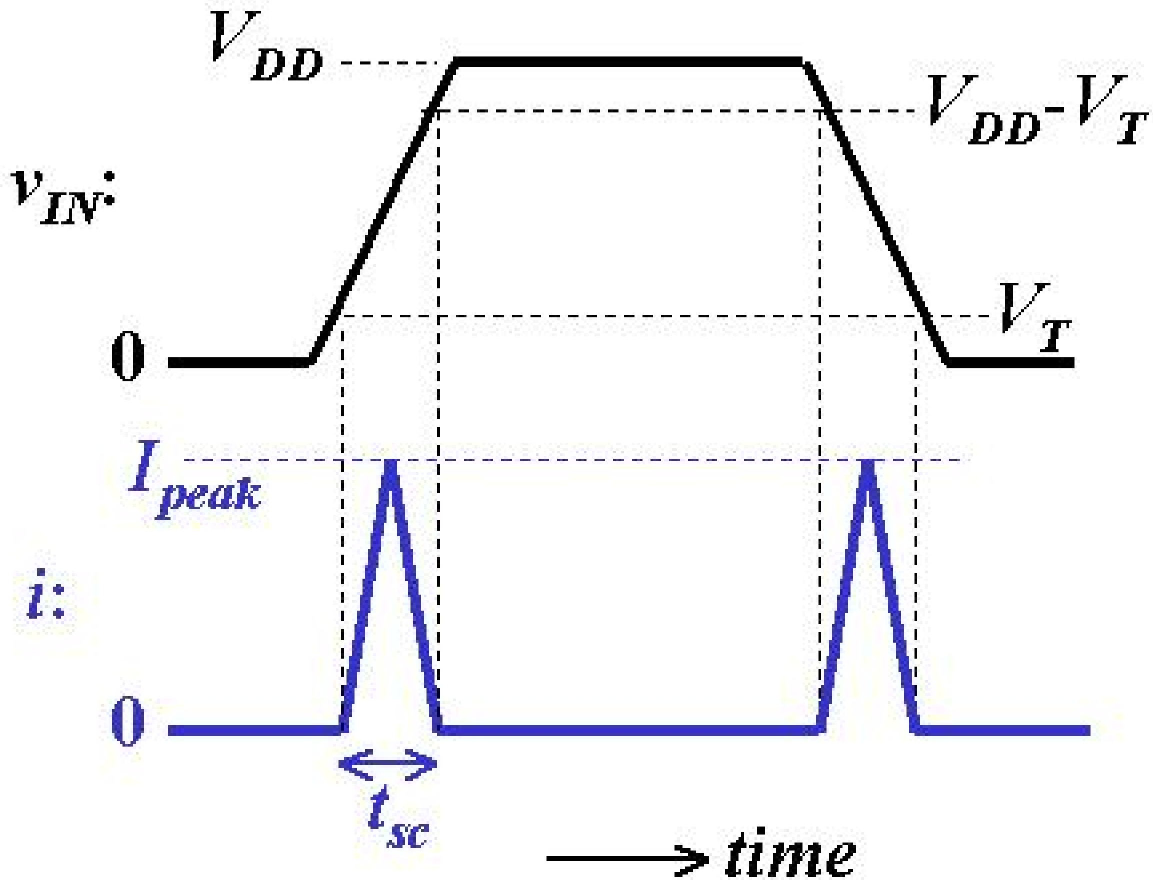
- The output is always connected to V_{DD} or **GND** in steady state
  - → Full logic swing; large noise margins
  - → Logic levels are not dependent upon the relative sizes of the devices ("ratioless")
- There is no direct path between V_{DD} and **GND** in steady state
  - → no static power dissipation

The CMOS Inverter: Current Flow during Switching



Power Dissipation due to Direct-Path Current

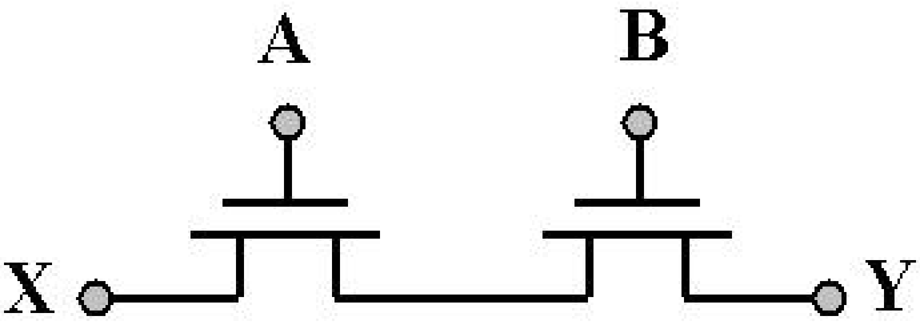




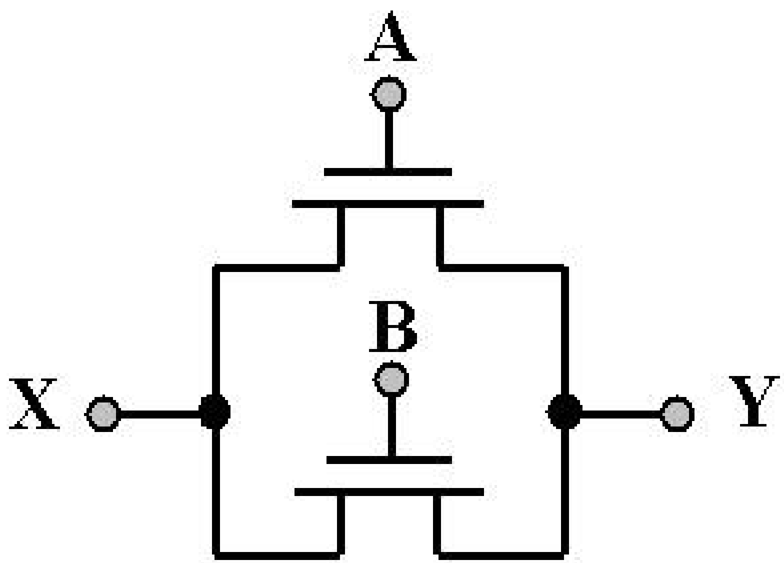
Energy consumed per switching period: $E_{dp} = t_{sc} V_{DD} I_{peak}$

N-Channel MOSFET Operation

An NMOSFET is a closed switch when the input is high



Y = **X** if **A** and **B**

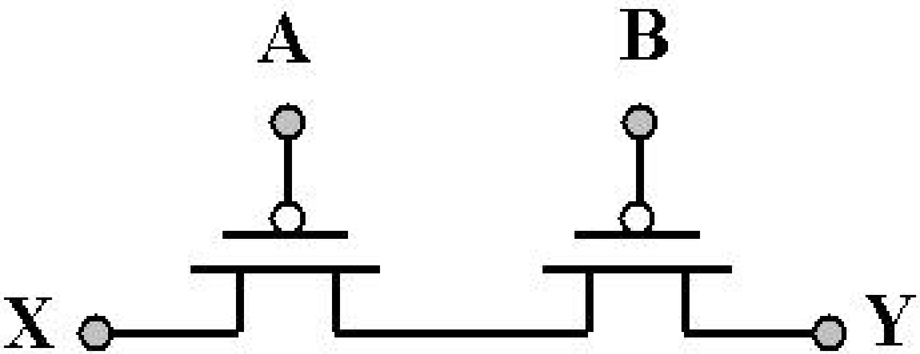


Y = **X** if **A** or **B**

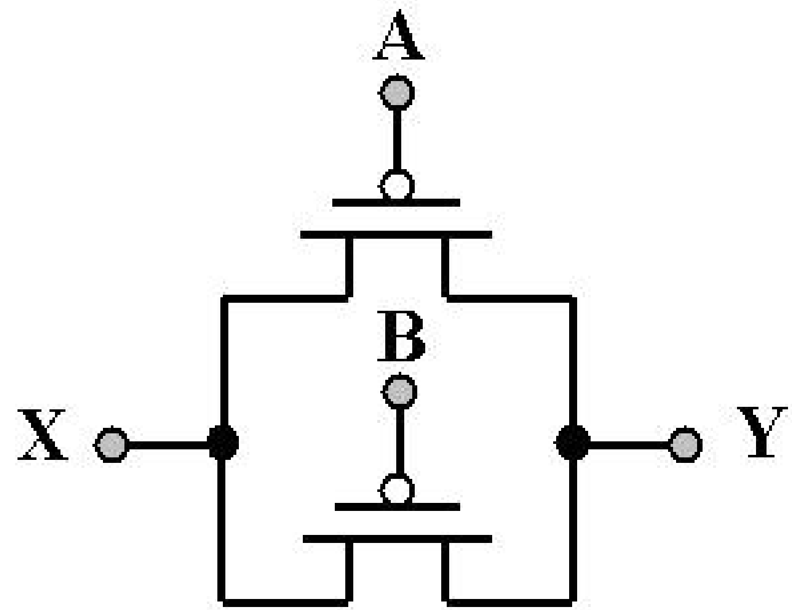
NMOSFETs pass a "strong" **0** but a "weak" **1**

P-Channel MOSFET Operation

A PMOSFET is a closed switch when the input is low



$$Y = X \text{ if } \bar{A} \text{ and } \bar{B}$$
$$= (\overline{A + B})$$

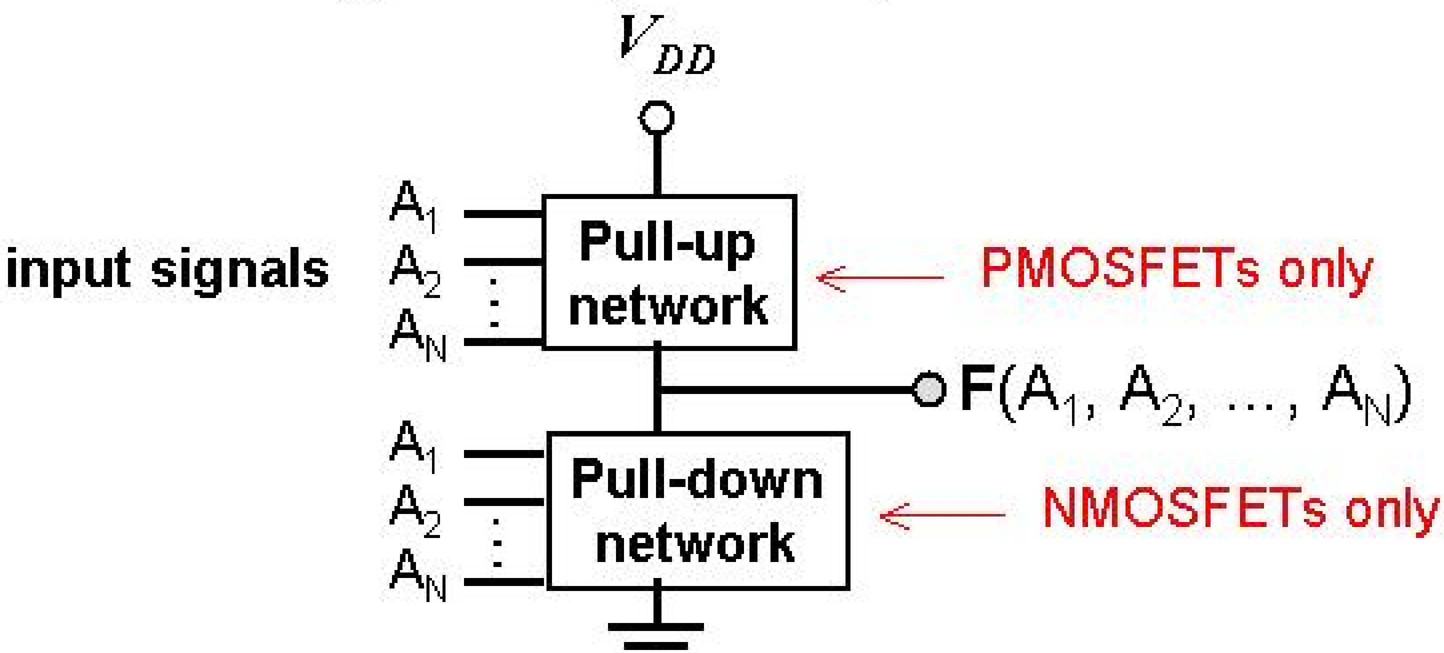


$$Y = X \text{ if } \bar{A} \text{ or } \bar{B}$$
$$= (\overline{AB})$$

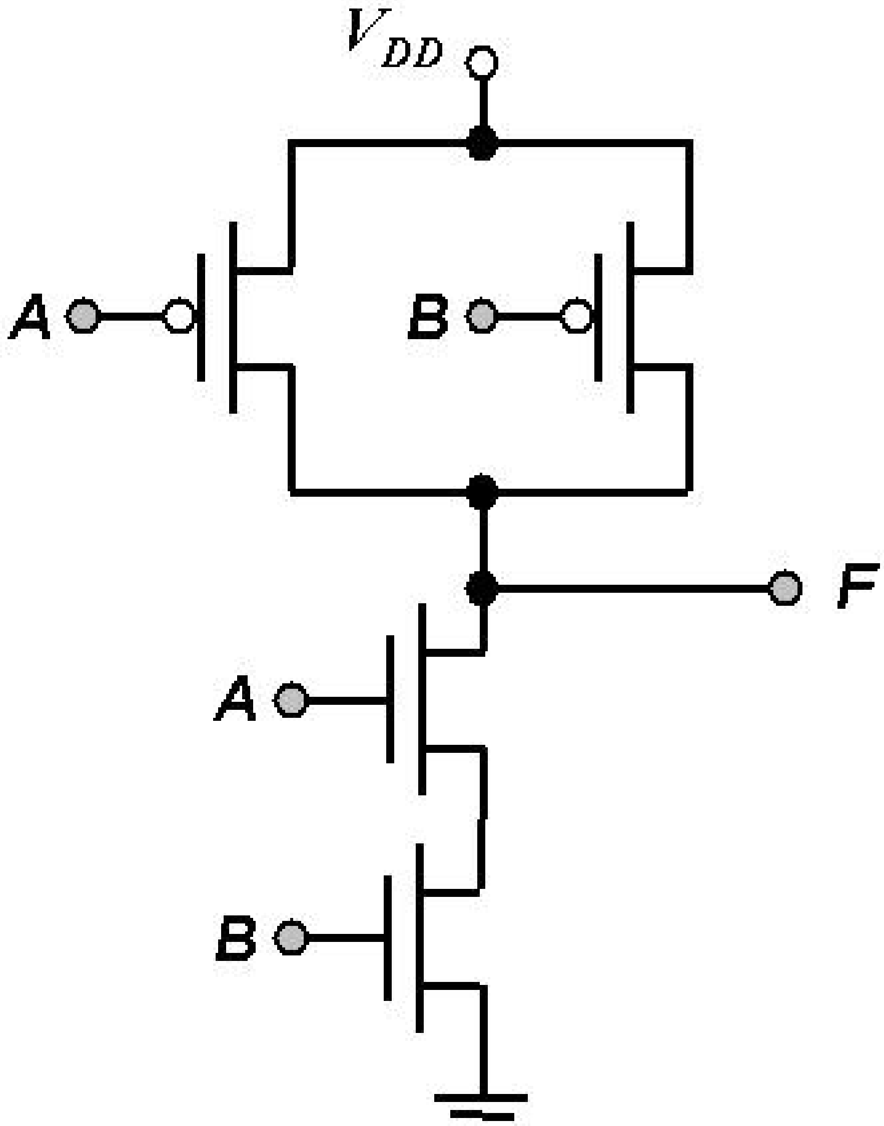
PMOSFETs pass a "strong" **1** but a "weak" **0**

Pull-Down and Pull-Up Devices

- In CMOS logic gates, NMOSFETs are used to connect the output to **GND**, whereas PMOSFETs are used to connect the output to V_{DD}.
  - An NMOSFET functions as a ***pull-down device*** when it is turned on (gate voltage = V_{DD})
  - A PMOSFET functions as a ***pull-up device*** when it is turned on (gate voltage = ***GND***)

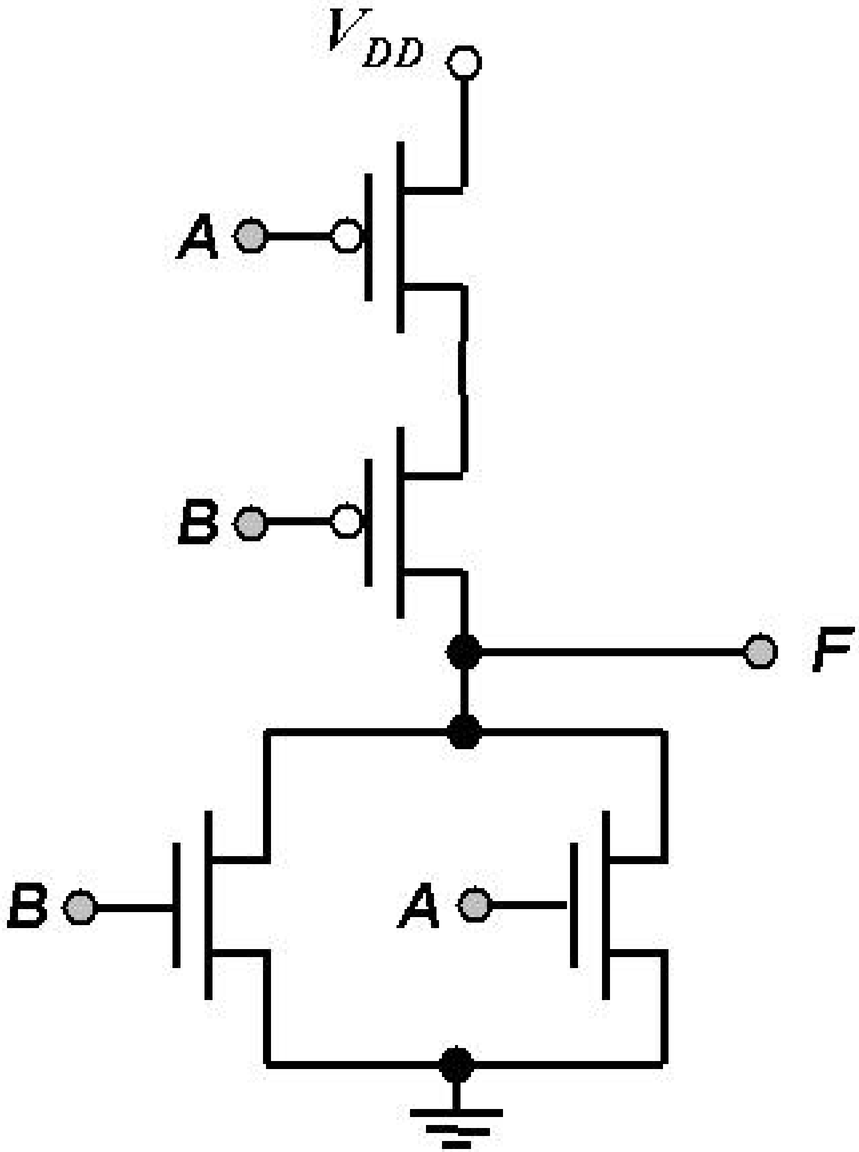


CMOS NAND Gate



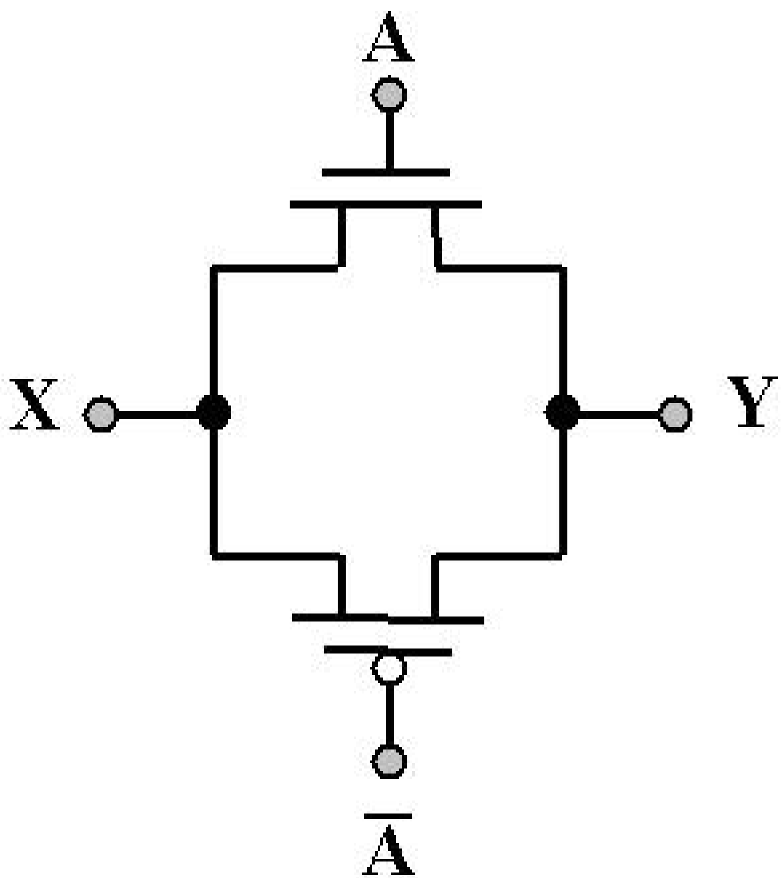
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NOR Gate



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

CMOS Pass Gate



Y = X if A

The "Body Effect"

V_T is a function of V_{SB}:

$$V_T = V_{T0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

$$\text{where} \quad \phi_F = \frac{kT}{q}\ln\left(\frac{N_B}{n_i}\right)$$

γ is the ***body effect coefficient***

When the body-source pn junction is reverse-biased, $|V_T|$ increases. Usually, we want to minimize γ so that I_{Dsat} will be the same for all transistors in a circuit.

Example (0.25μm CMOS technology)