Lecture #23

No Class on Thurs., April 22

OUTLINE

• Maximum clock frequency - three figures of merit
• Continuously-switched inverters
• Ring oscillators
• IC Fabrication Technology
  - Doping
  - Oxidation
  - Thin-film deposition
  - Lithography
  - Etch

Reading (Rabaey et al.)
• Chapters 5.4 and 2.1-2.2
Midterm 2: mean = 24.8; std = 8.6
How to measure inverter performance?

1) We have defined the unit delay $t_p$ as the time until $V_{out1}$ reaches $V_{DD}/2$ starting at either 0V (rising) or $V_{DD}$ (falling). $V_{in1}$ is a step function.

There are two other measures of performance which we can also consider:

2) The stage delay when the input is a continuous square-wave clock input.

3) The delay of a pulse through a multi-stage “ring oscillator”,
Unit gate delay performance measurement

Suppose $V_{in1}$ goes from low to high.

$V_{out1}$ goes from $V_{DD}$ to ground.

We defined the inverter delay $t_{pHL}$ as the time until $V_{out1}$ reaches $V_{DD}/2$.

Because when it reaches this value, the following stage will sense that its input has switched from high to low. Similarly $t_{pLH}$ is the time for the output to rise from zero to $V_{DD}/2$ when the input is falling. Maximum frequency is just $1/(t_{pHL} + t_{pLH})$. The properly designed stage will have similar delay time for rising input as for falling input. (Design proper ratio of $W_p$ to $W_n$.)
Driving Inverters (or gates) with Square-Wave Clock

Node X loaded by $C_X$
Inverter 1 has output resistance $R_p$ or $R_n$

Let's follow $V_X$ for $V_{IN}$ starting at $t=0$

Output slowly converges to sawtooth waveform. Let's find relationship between max and min values $v_h$ and $v_l$ after many cycles:

1. Pull down: $v_l = v_h e^{-\Delta t / R_n C_X}$
2. Pull up: $v_h = V_{DD} + (v_l - V_{DD}) e^{-\Delta t / R_p C_X}$

Example: $R_n = R_p$, $\Delta t = R_n C_X \Rightarrow v_l = 0.27V_{DD}$, $v_h = 0.73V_{DD}$
Square-Wave Drive

Inverter 2 will operate correctly so long as $V_X$ passes through $v_{il}$ and $v_{ih}$. We approximate response of devices in inverter 2 as instantaneous (remember the steep transfer curve). Let’s look at $V_X$ after a long time.

When $V_X$ crosses down through $v_{il}$, inverter 2 switches, and when it crosses up through $v_{ih}$, it switches back.
If frequency increases when will inverter fail?

If $V_x$ does not pass through $V_{il}$ or $V_{ih}$, because frequency is too high.

**MAXIMUM CLOCK FREQUENCY $f_{\text{max}}$**: Increase $f$ until inverter 2 fails to toggle because its input does not pass through its threshold(s). In general, $R_p \neq R_n$, so rise or fall is slower.
Example:

Take $R = 3\, \text{K}$, $C = 5\, \text{fF}$, $t_{pHL} = t_{pLH} = 0.69\, \text{RC} = 10\, \text{pS}$; 
So $f_{\text{max}1} = 50\, \text{GHz}$

Now consider the square-wave drive case:

Take $V_{\text{DD}} = 2.5\, \text{V}$, $V_{\text{ih}} = 1.5$, $V_{\text{il}} = 1\, \text{V}$, so in this symmetric case:

$$V_{\text{il}} = V_{\text{ih}} e^{-\Delta t/RC} \quad \text{and} \quad V_{\text{ih}} = V_{\text{DD}} + (V_{\text{il}} - V_{\text{DD}}) e^{-\Delta t/RC}$$

Solving either equation with

$RC = 15\, \text{pS}$, $\Delta t = 6.1\, \text{pS}$;

$f_{\text{max}2} = \frac{10^{12}}{12.2} = 82\, \text{GHz}$

(obviously this result depends on our somewhat arbitrary choice for $V_{\text{ih}}$ and $V_{\text{il}}$)
Ring Oscillator

Odd number of stages

As soon as the inverter 1 drives inverter 2’s input past $V_{il}$ (falling) or $V_{ih}$ (rising), inverter 2 switches and starts driving input node of 3 toward its switch point, etc. **Note:** V starts at 0V (rising) or VDD (falling) WHY?

Result: Signal propagates along chain at another kind of maximum clock frequency $f_{max}^*$ (really maximum propagation frequency)

Let the average delay per stage be $\Delta t_{MIN}$ then the time around loop is $N \times \Delta t_{MIN}$. One period is twice around the loop, so $2N\Delta t_{MIN} = \frac{1}{f_{R.O.}}$, something very easy to measure. [If $\Delta t_{MIN}$ is 20pSec but N is 1001, the period $1/f_{R.O.}$ is 40 nSec.]

Now we define $f_{max}^*$ by $\Delta t_{MIN} = \frac{1}{2f_{MAX}^*}$, so $f_{MAX}^* = f_{R.O.} \times N$ could be 1001 easy to measure (low frequency)

**NOTE:** $f_{max}^* < f_{max2}$ WHY?
**Ring Oscillator**

Odd number of stages
As soon as the switch closes inverter 5 drives inverter 1’s input up (starting at 0 V). When it reaches $V_{ih}$ inverter 1 switches and starts driving input node of inverter two down, starting at $V_{DD}$. We note that the transient always starts at 0 or $V_{DD}$ and ends at $V_{ih}$ or $V_{il}$, respectively.

This clearly takes longer than the clock-driven chain of inverter transient.

Need to solve same exponential equations as in square-wave drive, but with different limits:

**Up:** Start at 0, end at $V_{ih}$.

$$V_{ih} = V_{DD}[1 - \exp(-\Delta t_{LH}/R_p C)]$$

**Down:** Start at $V_{DD}$, end at $V_{il}$.

$$V_{il} = V_{DD}[\exp(-\Delta t_{HL}/R_n C)]$$

Solve for $\Delta t_{LH}$ and $\Delta t_{HL}$ and avg. to get $\Delta t_{MIN}$:

$$\Delta t_{MIN} = (\Delta t_{LH} + \Delta t_{HL})/2$$
Ring Oscillator Example

101 Stages, same parameters: \((RC = 15 \text{ pS})\)

From \(V_{ih} = V_{DD}[1-\exp(-\Delta t_{LH}/R_p C)]\) we find \(\Delta t_{LH} = 13.7\text{ pS}\)

Similarly from \(V_{il} = V_{DD}[\exp(-\Delta t_{HL}/R_n C)]\) \(\Delta t_{HL} = 13.7\text{ pS}\)

Thus the delay through 101 stages, twice is \(202 \times 13.7 = 2.78\text{ nS}\).

The ring oscillator frequency is \(10^9/2.78 = 360 \text{ MHz}\).

Finally, \(f_{\text{max}}^* = 360 \times 101 = 36 \text{ GHz}\).

This is of course less than either the 50GHz estimated from unit gate delay or the 82 GHz estimated from square-wave driven max toggle frequency.
Integrated Circuit Fabrication

Goal:
Mass fabrication (i.e. simultaneous fabrication) of many "chips", each a circuit (e.g. a microprocessor or memory chip) containing millions or billions of transistors

Method:
Lay down thin films of semiconductors, metals and insulators and pattern each layer with a process much like printing (lithography).

Materials used in a basic CMOS integrated circuit:
- Si substrate – selectively doped in various regions
- SiO₂ insulator
- Polycrystalline silicon – used for the gate electrodes
- Metal contacts and wiring
Si Substrates (Wafers)

Crystals are grown from a melt in boules (cylinders) with specified dopant concentrations. They are ground perfectly round and oriented (a "flat" or "notch" is ground along the boule) and then sliced like baloney into wafers. The wafers are then polished.

Typical wafer cost: $50
Sizes: 150 mm, 200 mm, 300 mm diameter
Adding Dopants into Si

Suppose we have a wafer of Si which is p-type and we want to change the surface to n-type. The way in which this is done is by ion implantation. Dopant ions are shot out of an “ion gun” called an ion implanter, into the surface of the wafer.

Typical implant energies are in the range 1-200 keV. After the ion implantation, the wafers are heated to a high temperature (∼1000°C). This “annealing” step heals the damage and causes the implanted dopant atoms to move into substitutional lattice sites.
Dopant Diffusion

- The implanted depth-profile of dopant atoms is peaked.

- In order to achieve a more uniform dopant profile, high-temperature annealing is used to diffuse the dopants.

- Dopants can also be directly introduced into the surface of a wafer by diffusion (rather than by ion implantation) from a dopant-containing ambient or doped solid source.
Formation of Insulating Films

- The favored insulator is pure silicon dioxide ($\text{SiO}_2$).
- A $\text{SiO}_2$ film can be formed by one of two methods:
  1. Oxidation of Si at high temperature in $\text{O}_2$ or steam ambient
  2. Deposition of a silicon dioxide film
Thermal Oxidation

\[ Si + O_2 \rightarrow SiO_2 \quad \text{or} \quad Si + 2H_2O \rightarrow SiO_2 + 2H_2 \]

“dry” oxidation \hspace{1cm} “wet” oxidation

- Temperature range:
  - 700°C to 1100°C
- Process:
  - \( O_2 \) or \( H_2O \) diffuses through \( SiO_2 \) and reacts with Si at the interface to form more \( SiO_2 \)
- 1 \( \mu m \) of \( SiO_2 \) formed consumes \( \sim 0.5 \mu m \) of Si

\( \alpha \propto \sqrt{t} \)

\( \alpha \propto t \)

oxide thickness

time, t
Example: Thermal Oxidation of Silicon

Silicon wafer, 100 μm thick

Thermal oxidation grows SiO$_2$ on Si, but it consumes Si, so the wafer gets thinner. Suppose we grow 1 μm of oxide:

99 μm thick Si, with 1 μm SiO$_2$ all around → total thickness = 101 μm
Effect of Oxidation Rate Dependence on Thickness

- The thermal oxidation rate slows with oxide thickness. Consider a Si wafer with a patterned oxide layer:

  \[ \text{SiO}_2 \text{ thickness} = 1 \ \mu\text{m} \]

Now suppose we grow 0.1 \( \mu\text{m} \) of \( \text{SiO}_2 \):

\[ \text{SiO}_2 \text{ thickness} = 1.02 \ \mu\text{m} \]

Note the 0.04\( \mu\text{m} \) step in the Si surface!

\[ \text{SiO}_2 \text{ thickness} = 0.1 \ \mu\text{m} \]
Selective Oxidation Techniques

Window Oxidation

Local Oxidation (LOCOS)
Chemical Vapor Deposition (CVD) of SiO$_2$

\[ \text{SiH}_4 + O_2 \rightarrow \text{SiO}_2 + 2\text{H}_2 \]

“LTO”

- Temperature range:
  - 350°C to 450°C for silane

- Process:
  - Precursor gases dissociate at the wafer surface to form SiO$_2$
  - No Si on the wafer surface is consumed

- Film thickness is controlled by the deposition time
Chemical Vapor Deposition (CVD) of Si

Polycrystalline silicon ("poly-Si"):

Like SiO₂, Si can be deposited by Chemical Vapor Deposition:
- Wafer is heated to ~600°C
- Silicon-containing gas (SiH₄) is injected into the furnace:
  \[ \text{SiH}_4 = \text{Si} + 2\text{H}_2 \]

Si film made up of crystallites

Properties:
- sheet resistance (heavily doped, 0.5 μm thick) = 20 Ω/□
- can withstand high-temperature anneals \(\rightarrow\) major advantage
Physical Vapor Deposition ("Sputtering")

Used to deposit Al films:

Highly energetic argon ions batter the surface of a metal target, knocking atoms loose, which then land on the surface of the wafer.

Sometimes the substrate is heated, to $\sim 300^\circ C$.

Gas pressure: 1 to 10 mTorr
Deposition rate $\propto I \cdot S$ sputtering yield
Ion current
Patterning the Layers

Planar processing consists of a sequence of additive and subtractive steps with lateral patterning.

- oxidation
- deposition
- etching
- ion implantation
- lithography

Lithography refers to the process of transferring a pattern to the surface of the wafer.

Equipment, materials, and processes needed:

- A mask (for each layer to be patterned) with the desired pattern
- A light-sensitive material (called photoresist) covering the wafer so as to receive the pattern
- A light source and method of projecting the image of the mask onto the photoresist ("printer" or "projection stepper" or "projection scanner")
- A method of "developing" the photoresist, that is selectively removing it from the regions where it was exposed
The Photo-Lithographic Process

1. Oxidation
2. Photoresist removal (ashing)
3. Process step
4. Spin, rinse, dry
5. Acid etch
6. Optical mask
7. Photoresist exposure
8. Photoresist develop
Photoresist Exposure

- A glass mask with a black/clear pattern is used to expose a wafer coated with \(~1 \mu m\) thick photoresist.

Image of mask appears here (3 dark areas, 4 light areas)

Mask image is demagnified by nX
- "10X stepper"
- "4X stepper"
- "1X stepper"

Areas exposed to UV light are susceptible to chemical removal.
Exposure using “Stepper” Tool

- scribe line
- images
- field size increases with technology generation
- wafer
- Translational motion

[Diagram of stepper tool with labeled parts]
Photoresist Development

- Solutions with high pH dissolve the areas which were exposed to UV light; unexposed areas are not dissolved.
Lithography Example

- Mask pattern (on glass plate)
- Look at cuts (cross sections) at various planes
  (A-A and B-B)
"A-A" Cross-Section

The resist is exposed in the ranges $0 < x < 2 \, \mu m$ & $3 < x < 5 \, \mu m$:

![Diagram showing the resist exposure ranges with a mask pattern and resist regions.]

The resist will dissolve in high pH solutions wherever it was exposed:

![Diagram showing the resist dissolution after development.]

EECS40, Spring 2004
Lecture 23, Slide 30
Prof. Sanders
The photoresist is exposed in the ranges $0 < x < 5 \, \mu m$:
Pattern Transfer by Etching

In order to transfer the photoresist pattern to an underlying film, we need a "subtractive" process that removes the film, ideally with minimal change in the pattern and with minimal removal of the underlying material(s).

→ Selective etch processes (using plasma or aqueous chemistry) have been developed for most IC materials.

First: pattern photoresist

We have exposed mask pattern, and developed the resist

Next: Etch oxide

oxide etchant … photoresist is resistant.

Last: strip resist

etch stops on silicon ("selective etchant")

only resist is attacked

Jargon for this entire sequence of process steps: "pattern using XX mask"