Lecture #23

No Class on Thurs., April 22

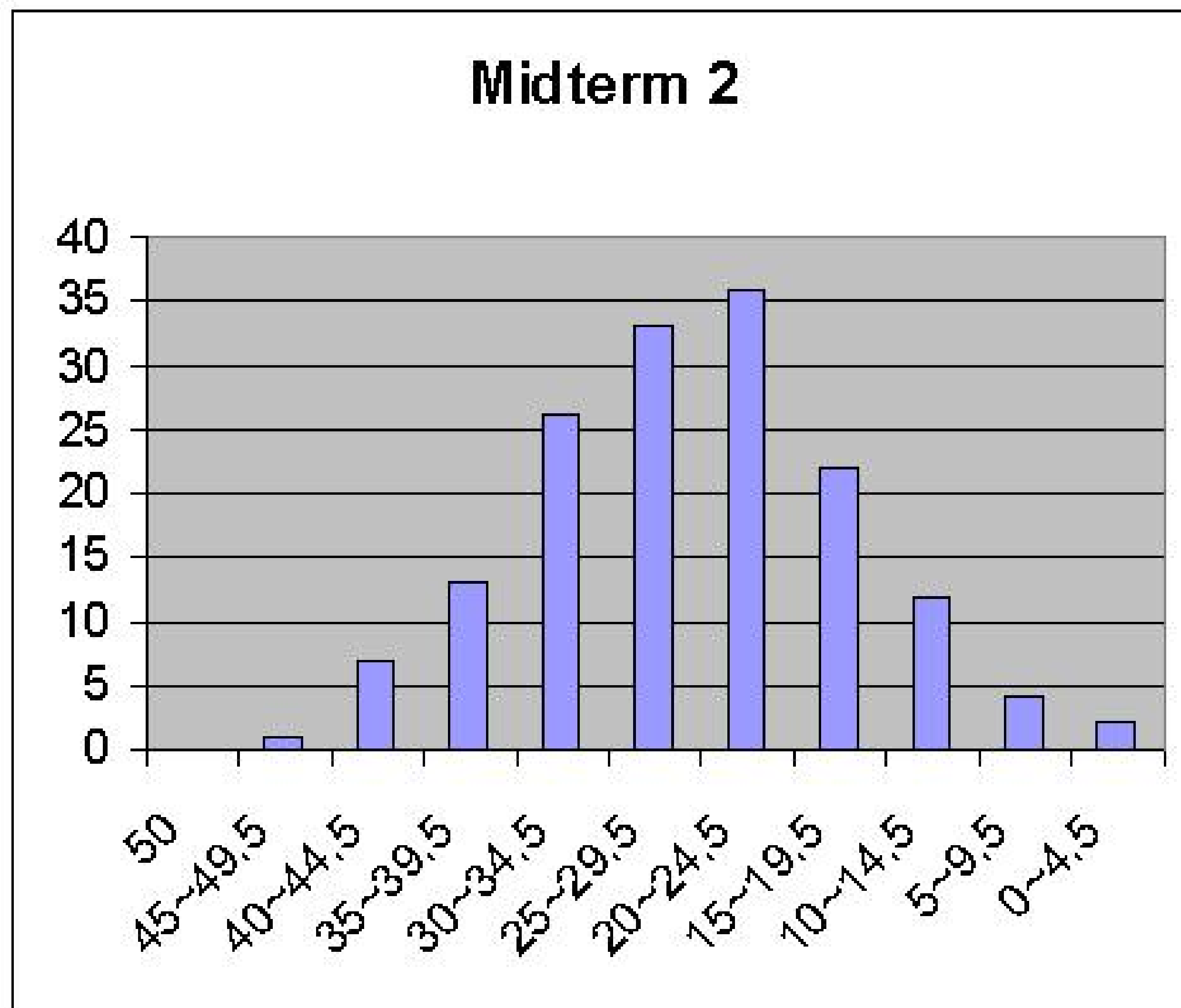
OUTLINE

- **Maximum clock frequency - three figures of merit**
- **Continuously-switched inverters**
- **Ring oscillators**
- **IC Fabrication Technology**
  - Doping
  - Oxidation
  - Thin-film deposition
  - Lithography
  - Etch

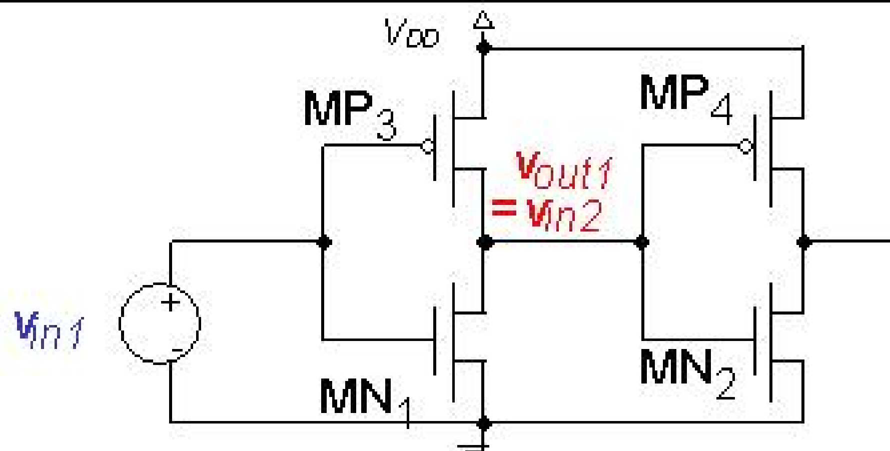
Reading (Rabaey *et al.*)

- Chapters 5.4 and 2.1-2.2

Midterm 2: mean = 24.8; std = 8.6



How to measure inverter performance?



1) **We have defined the unit delay t_p as the time until V_{out1} reaches V_{DD} /2 starting at either 0V (rising) or V_{DD} (falling) . V_{in1} is a step function.**

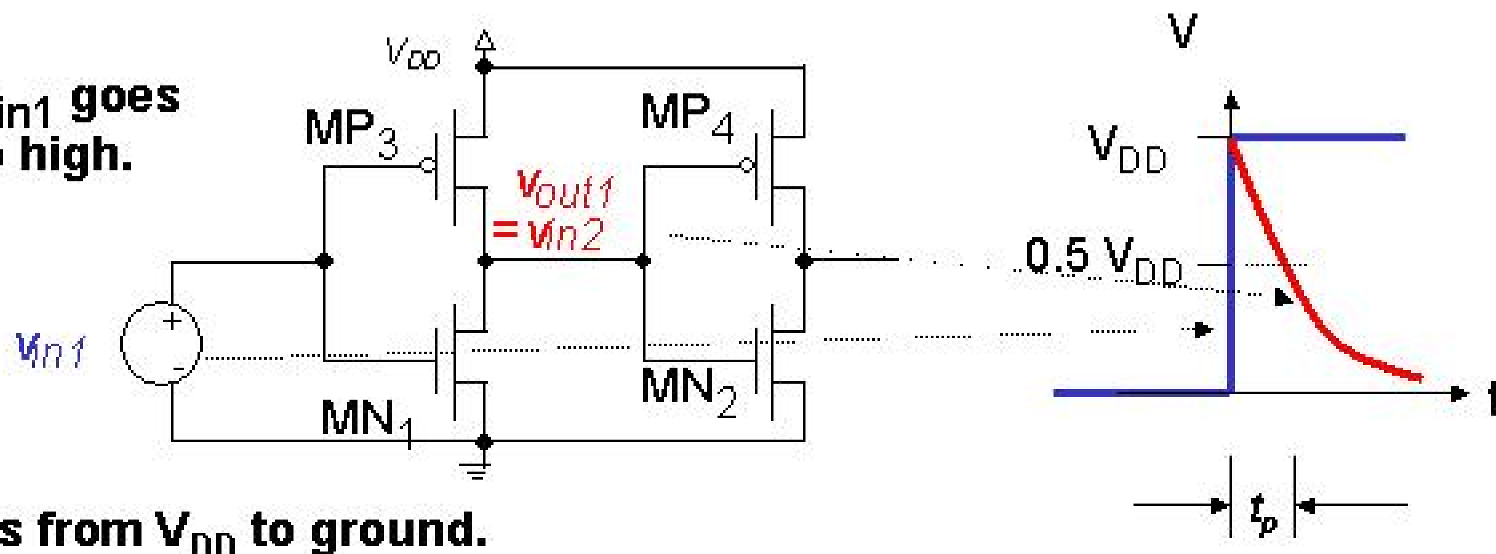
There are two other measures of performance which we can also consider:

2) **The stage delay when the input is a continuous square-wave clock input.**

3) **The delay of a pulse through a multi-stage "ring oscillator",**

Unit gate delay performance measurement

Suppose V_{in1} goes from low to high.

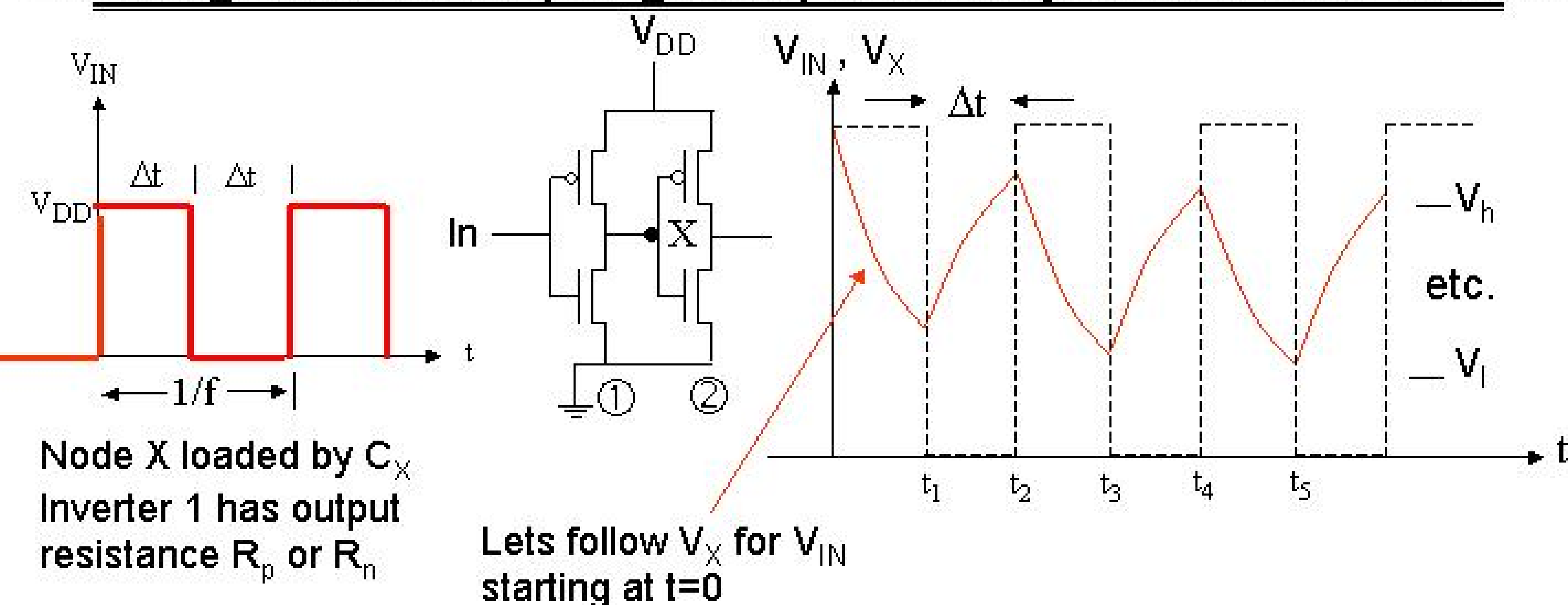


V_{out1} goes from V_{DD} to ground.

We defined the inverter delay t_{pHL} as the time until V_{out1} reaches V_{DD} /2 .

Because when it reaches this value, the following stage will sense that its input has switched from high to low. Similarly t_{pLH} is the time for the output to rise from zero to V_{DD} /2 when the input is falling.
Maximum frequency is just $1/(t_{pHL} + t_{pLH})$
The properly designed stage will have similar delay time for rising input as for falling input. (Design proper ratio of W_p to W_n)

Driving Inverters (or gates) with Square-Wave Clock



Output slowly converges to sawtooth waveform. Let's find relationship between max and min values v_h and v_l after many many cycles:

(1) Pull down: $$v_l = v_h e^{-\Delta t / R_n C_X}$$

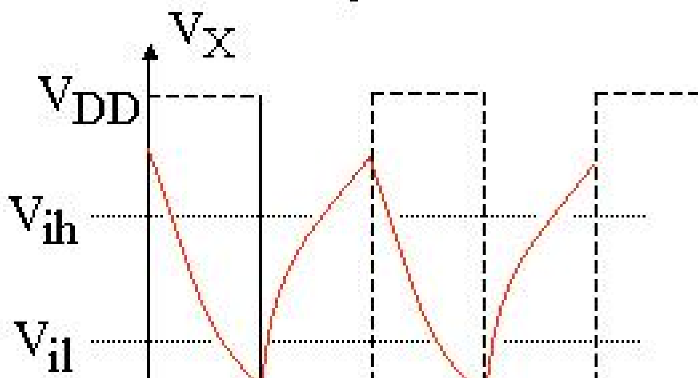
(2) Pull up: $$v_h = V_{DD} + (v_l - V_{DD}) e^{-\Delta t / R_p C_X}$$

can solve simultaneously given $\Delta t/RC$

Example: $R_n = R_p,\ \Delta t = R_n C_X \Rightarrow v_l = 0.27 V_{DD},\ v_h = 0.73 V_{DD}$

Square-Wave Drive

Inverter 2 will operate correctly so long as V_X passes through v_{il} and v_{ih}. We approximate response of devices in inverter 2 as instantaneous (remember the steep transfer curve). Let's look at V_X after a long time.



When V_X crosses down through v_{il}, inverter 2 switches, and when it crosses up through v_{ih}, it switches back

If frequency increases when will inverter fail?

If V_X does not pass through V_{il} or V_{ih}, because frequency is too high.

MAXIMUM CLOCK FREQUENCY f_{max} : Increase f until inverter 2 fails to toggle because its input does not pass through its threshold(s). In general, $R_p \neq R_n$, so rise or fall is slower.

Example:

Take R = 3 K, C = 5 fF, $t_{pHL} = t_{pLH} = 0.69\ RC = 10pS$ **;**
So $f_{max1} = 50GHz$

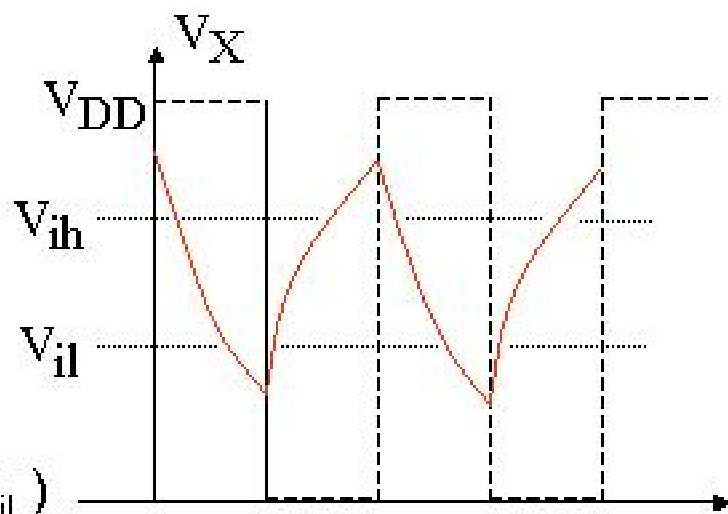
Now consider the square-wave drive case:

Take V_{DD}**=2.5V,** V_{ih} **= 1.5,** V_{il} **= 1V , so in this symmetric case:**

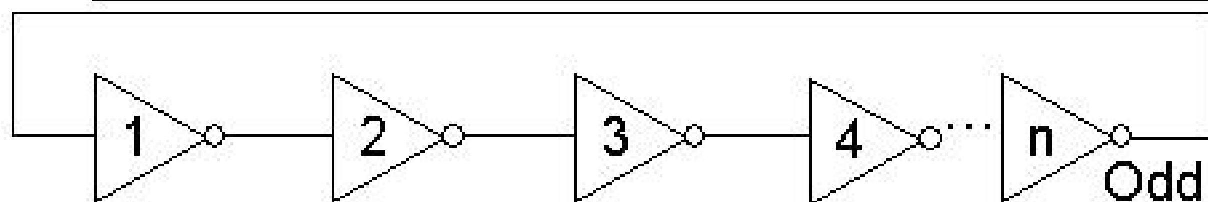
$$v_{il} = V_{ih} e^{-\Delta t / R_n C} \text{ and } v_{ih} = V_{DD} + (V_{il} - V_{DD}) e^{-\Delta t / R_p C}$$

Solving either equation with
RC = 15pS, Δt = 6.1pS;
$f_{max2} = 10^{12}/12.2 = 82GHz$

(obviously this result depends on our somewhat arbitrary choice for V_{ih} and V_{il})



Ring Oscillator



Odd number of stages

As soon as the inverter 1 drives inverter 2's input past V_{il} (falling) or V_{ih} (rising), inverter 2 switches and starts driving input node of ③ toward its switch point, etc. Note: V starts at 0V (rising) or VDD (falling) WHY?

Result: Signal propagates along chain at another kind of maximum clock frequency f_{max}^* (really maximum propagation frequency)

Let the average delay per stage be Δt_{MIN} then the time around loop is $N \times \Delta t_{MIN}$.

One period is twice around the loop, so $2N\Delta t_{MIN} = \frac{1}{f_{R.O.}}$, something very easy to measure. [If Δt_{MIN} is 20pSec but N is 1001, the period $1/f_{RO}$ is 40 nSec.]

Now we define f_{max}^* by $\Delta t_{MIN} = \frac{1}{2f_{MAX}^*}$,so

$f_{MAX}^* = f_{R.O.} \cdot N$ ← could be 1001

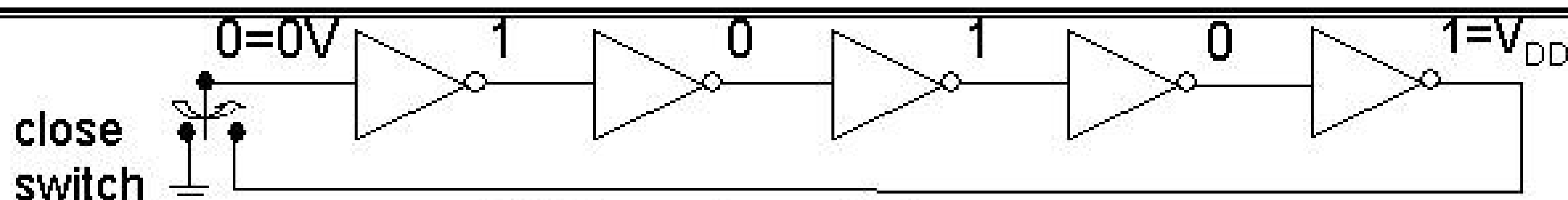
↑ easy to measure (low frequency)

NOTE:

$f_{max}^* < f_{max2}$

WHY?

Ring Oscillator



Odd number of stages

As soon as the switch closes inverter 5 drives inverter 1's input up (starting at 0 V). When it reaches V_{ih} inverter 1 switches and starts driving input node of inverter two down, starting at V_{DD}. We note that the transient always starts at 0 or V_{DD} and ends at V_{ih} or V_{il}, respectively.

This clearly takes longer than the clock-driven chain of inverter transient.

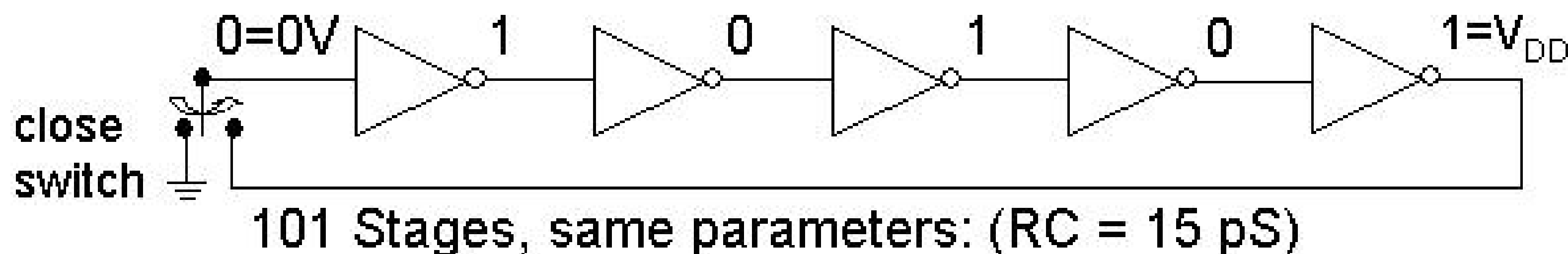
Need to solve same exponential equations as in square-wave drive, but with different limits:

Up: Start at 0, end at V_{ih}. $V_{ih} = V_{DD}[1-\exp(-\Delta t_{LH}/R_pC)]$

Down: Start at V_{DD}, end at V_{il}. $V_{il} = V_{DD}[\exp(-\Delta t_{HL}/R_nC)]$

Solve for Δt_{LH} and Δt_{HL} and avg. to get Δt_{MIN} : $\Delta t_{MIN} = (\Delta t_{LH} + \Delta t_{HL})/2$

Ring Oscillator Example



101 Stages, same parameters: (RC = 15 pS)

From $V_{ih} = V_{DD}[1-\exp(-\Delta t_{LH}/R_pC)]$ we find Δt_{LH} = 13.7pS

Similarly from $V_{il} = V_{DD}[\exp(-\Delta t_{HL}/R_nC)]$ Δt_{HL} = 13.7pS

Thus the delay through 101 stages, twice is 202 X 13.7 =2.78nS.

The ring oscillator frequency is $10^9/2.78$ = 360 MHz.

Finally, f_{max}^* = 360 X 101 = 36 GHz.

This is of course less than either the 50GHz estimated from unit gate delay or the 82 GHz estimated from square-wave driven max toggle frequency.

Integrated Circuit Fabrication

Goal:

Mass fabrication (*i.e.* simultaneous fabrication) of many "chips", each a circuit (e.g. a microprocessor or memory chip) containing millions or billions of transistors

Method:

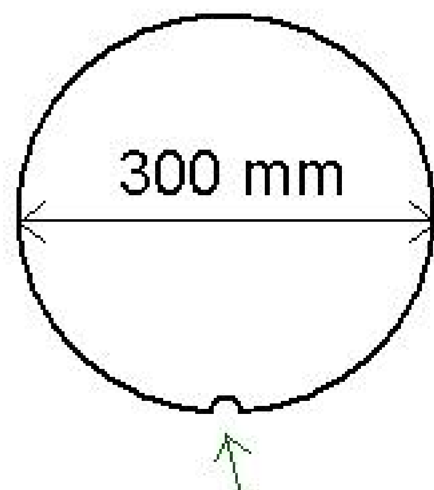
Lay down thin films of semiconductors, metals and insulators and pattern each layer with a process much like printing (lithography).

Materials used in a basic CMOS integrated circuit:

- Si substrate – selectively doped in various regions
- SiO_2 insulator
- Polycrystalline silicon – used for the gate electrodes
- Metal contacts and wiring

Si Substrates (Wafers)

Crystals are grown from a melt in boules (cylinders) with specified dopant concentrations. They are ground perfectly round and oriented (a "flat" or "notch" is ground along the boule) and then sliced like baloney into wafers. The wafers are then polished.



"notch" indicates crystal orientation

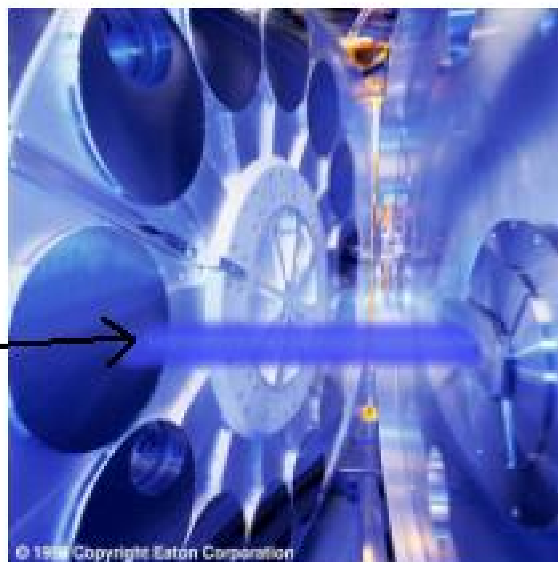
Typical wafer cost: $50

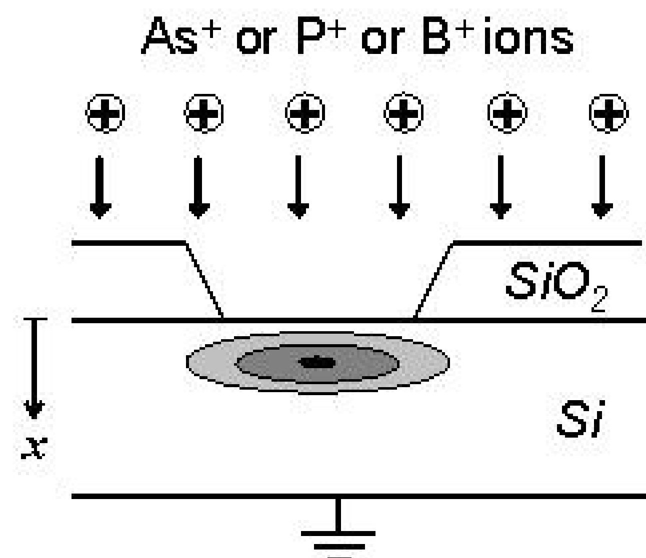
Sizes: 150 mm, 200 mm, 300 mm diameter

Adding Dopants into Si

Suppose we have a wafer of Si which is p-type and we want to change the surface to n-type. The way in which this is done is by *ion implantation*. Dopant ions are shot out of an "ion gun" called an *ion implanter,* into the surface of the wafer.

Eaton HE3 High-Energy Implanter, showing the ion beam hitting the end-station

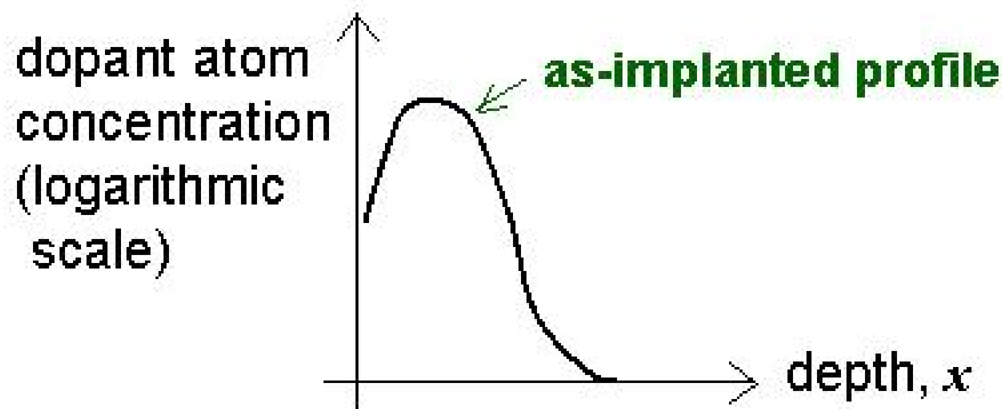


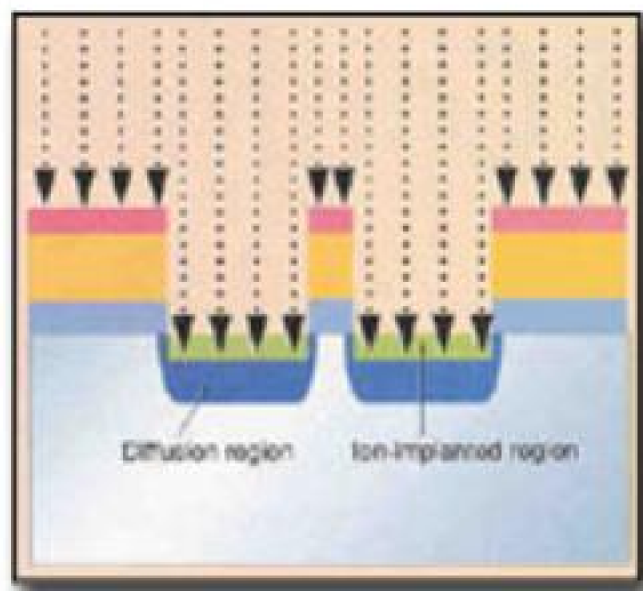


Typical implant energies are in the range 1-200 keV. After the ion implantation, the wafers are heated to a high temperature (~1000°C). This "annealing" step heals the damage and causes the implanted dopant atoms to move into substitutional lattice sites.

Dopant Diffusion

- The implanted depth-profile of dopant atoms is peaked.





- In order to achieve a more uniform dopant profile, high-temperature annealing is used to diffuse the dopants
- Dopants can also be directly introduced into the surface of a wafer by diffusion (rather than by ion implantation) from a dopant-containing ambient or doped solid source

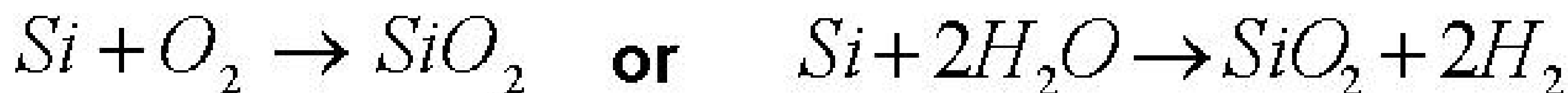
Formation of Insulating Films

- The favored insulator is pure silicon dioxide (SiO_2).
- A SiO_2 film can be formed by one of two methods:
  1. Oxidation of Si at high temperature in O_2 or steam ambient
  2. Deposition of a silicon dioxide film

ASM A412 batch oxidation furnace

Applied Materials low-pressure chemical-vapor deposition (CVD) chamber

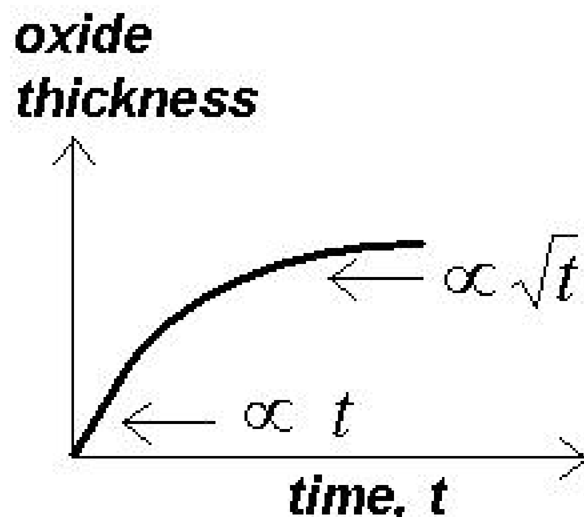
Thermal Oxidation



"dry" oxidation

"wet" oxidation

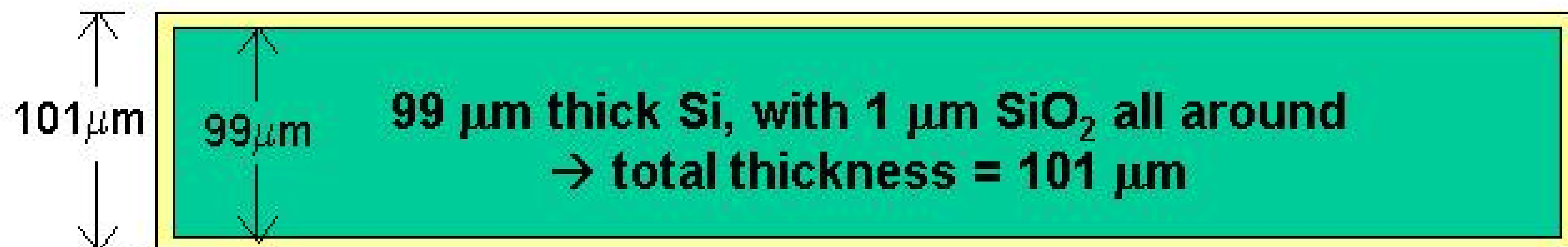
- **Temperature range:**
  - 700°C to 1100°C
- **Process:**
  - O_2 or H_2O diffuses through SiO_2 and reacts with Si at the interface to form more SiO_2
- **1 μm of SiO_2 formed consumes ~0.5 μm of Si**



Example: Thermal Oxidation of Silicon

Silicon wafer, 100 μm thick

Thermal oxidation grows SiO_2 on Si, but it consumes Si, so the wafer gets thinner. Suppose we grow 1 μm of oxide:

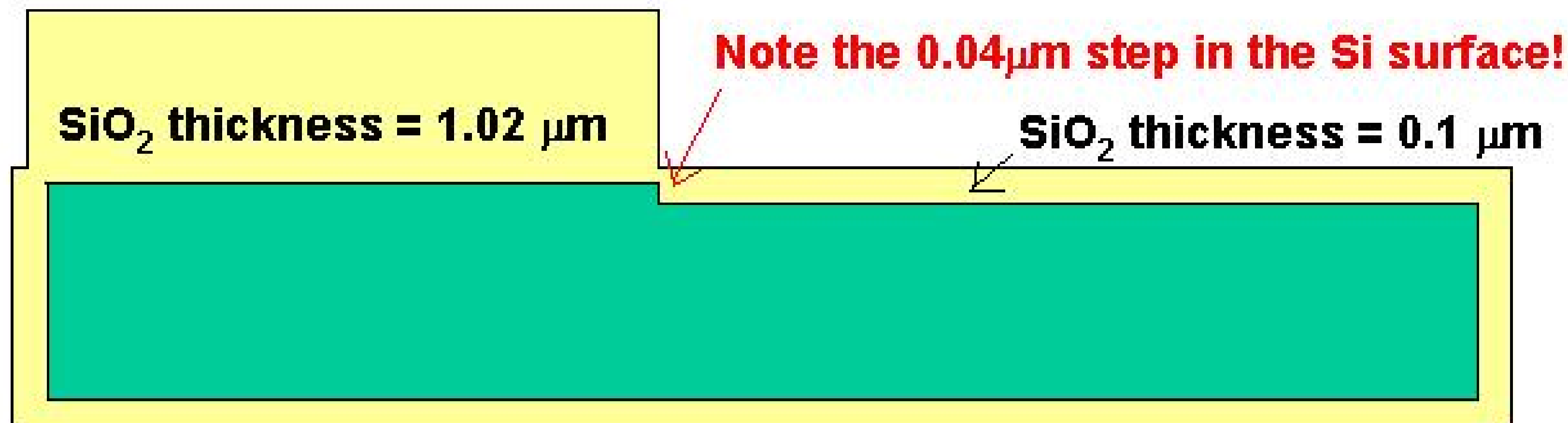


Effect of Oxidation Rate Dependence on Thickness

- **The thermal oxidation rate slows with oxide thickness.**

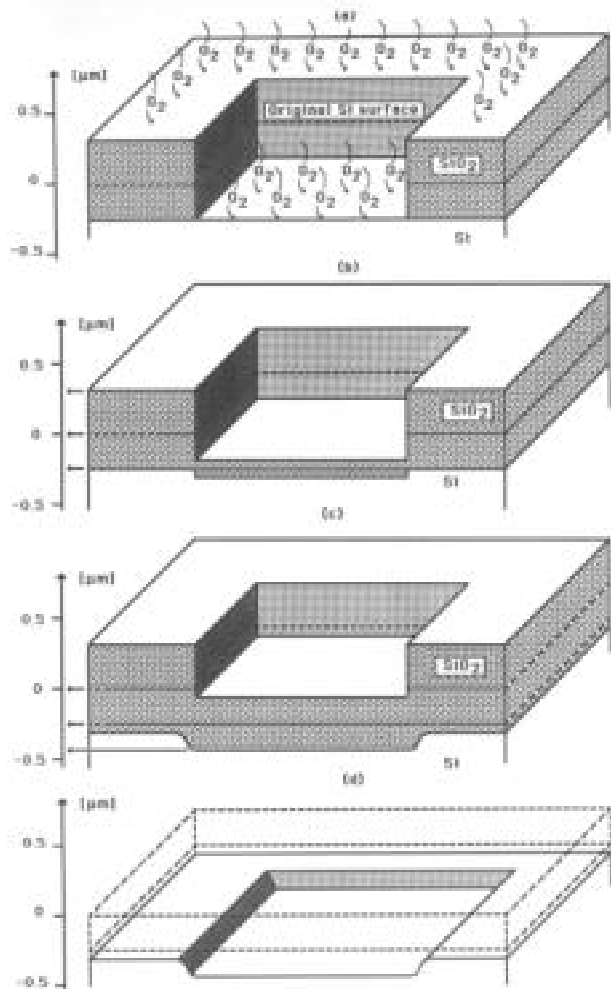
Consider a Si wafer with a patterned oxide layer:

Now suppose we grow 0.1 μm of SiO_2:

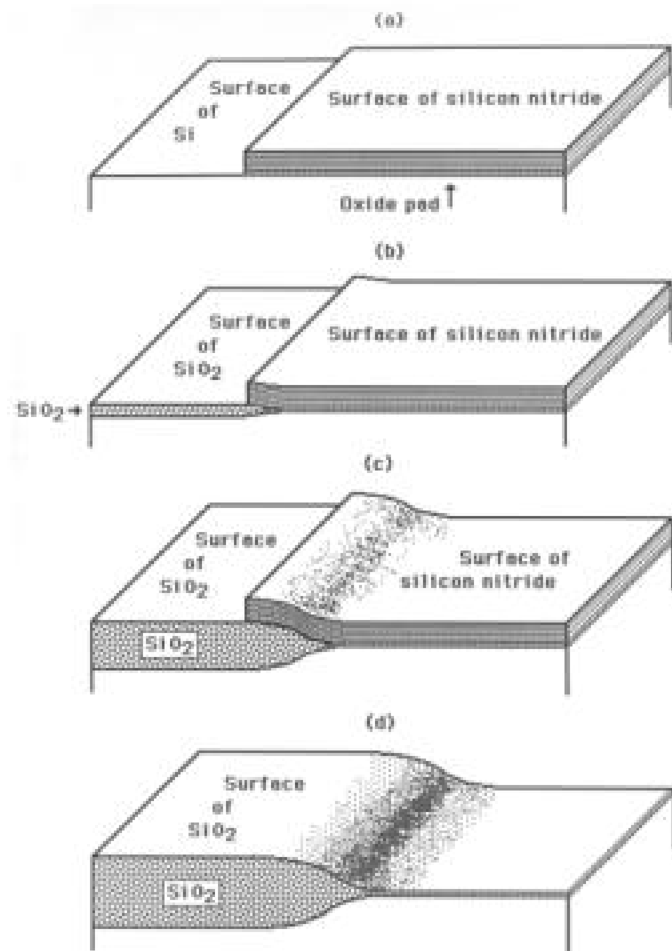


Selective Oxidation Techniques

Window Oxidation

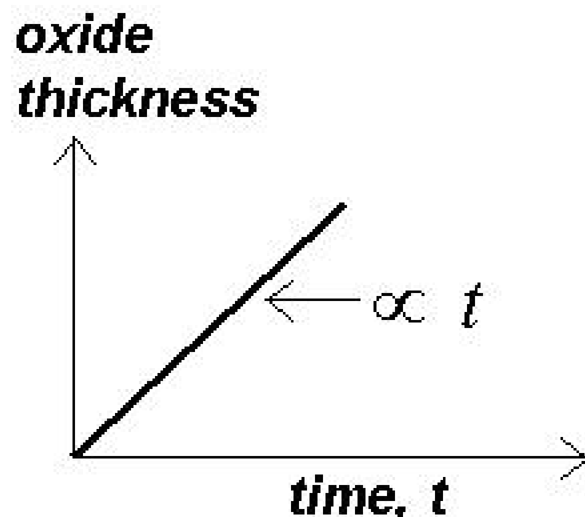


Local Oxidation (LOCOS)



Chemical Vapor Deposition (CVD) of SiO_2

- **Temperature range:**
  - 350°C to 450°C for silane
- **Process:**
  - Precursor gases dissociate at the wafer surface to form SiO_2
  - No Si on the wafer surface is consumed
- **Film thickness is controlled by the deposition time**

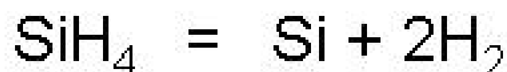


Chemical Vapor Deposition (CVD) of Si

Polycrystalline silicon ("poly-Si"):

Like SiO_2, Si can be deposited by **C**hemical **V**apor **D**eposition:

- Wafer is heated to ~600°C
- Silicon-containing gas (SiH_4) is injected into the furnace:



Si film made up of crystallites

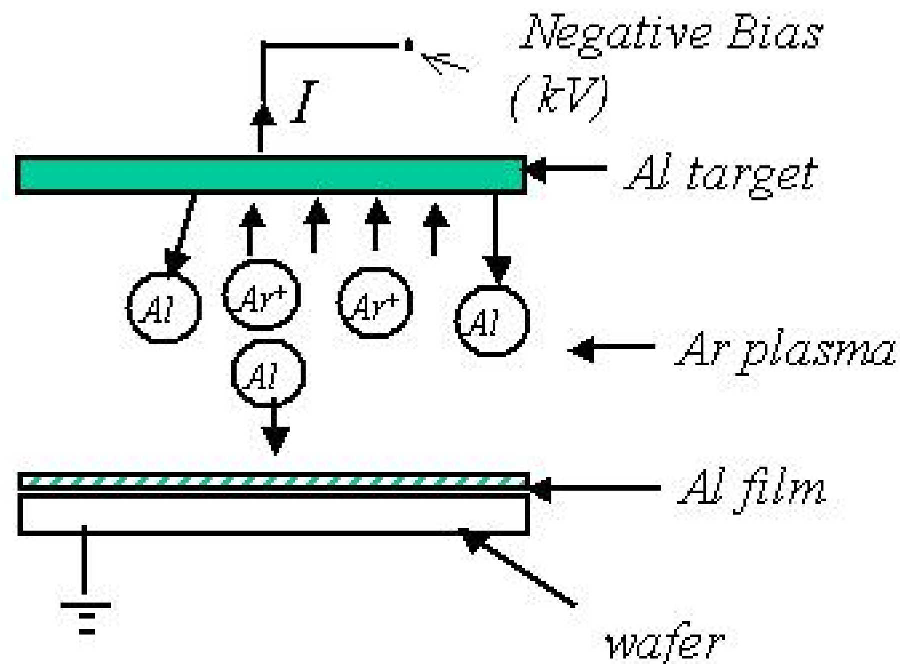
<u>Properties</u>:

- **sheet resistance (heavily doped, 0.5 μm thick) = 20 Ω/□**
- **can withstand high-temperature anneals → major advantage**

Physical Vapor Deposition ("Sputtering")

Used to deposit Al films:

Highly energetic argon ions batter the surface of a metal target, knocking atoms loose, which then land on the surface of the wafer



Sometimes the substrate is heated, to ~300°C

Gas pressure: 1 to 10 mTorr

Deposition rate $\propto I \bullet S$

sputtering yield (S)

ion current (I)

Patterning the Layers

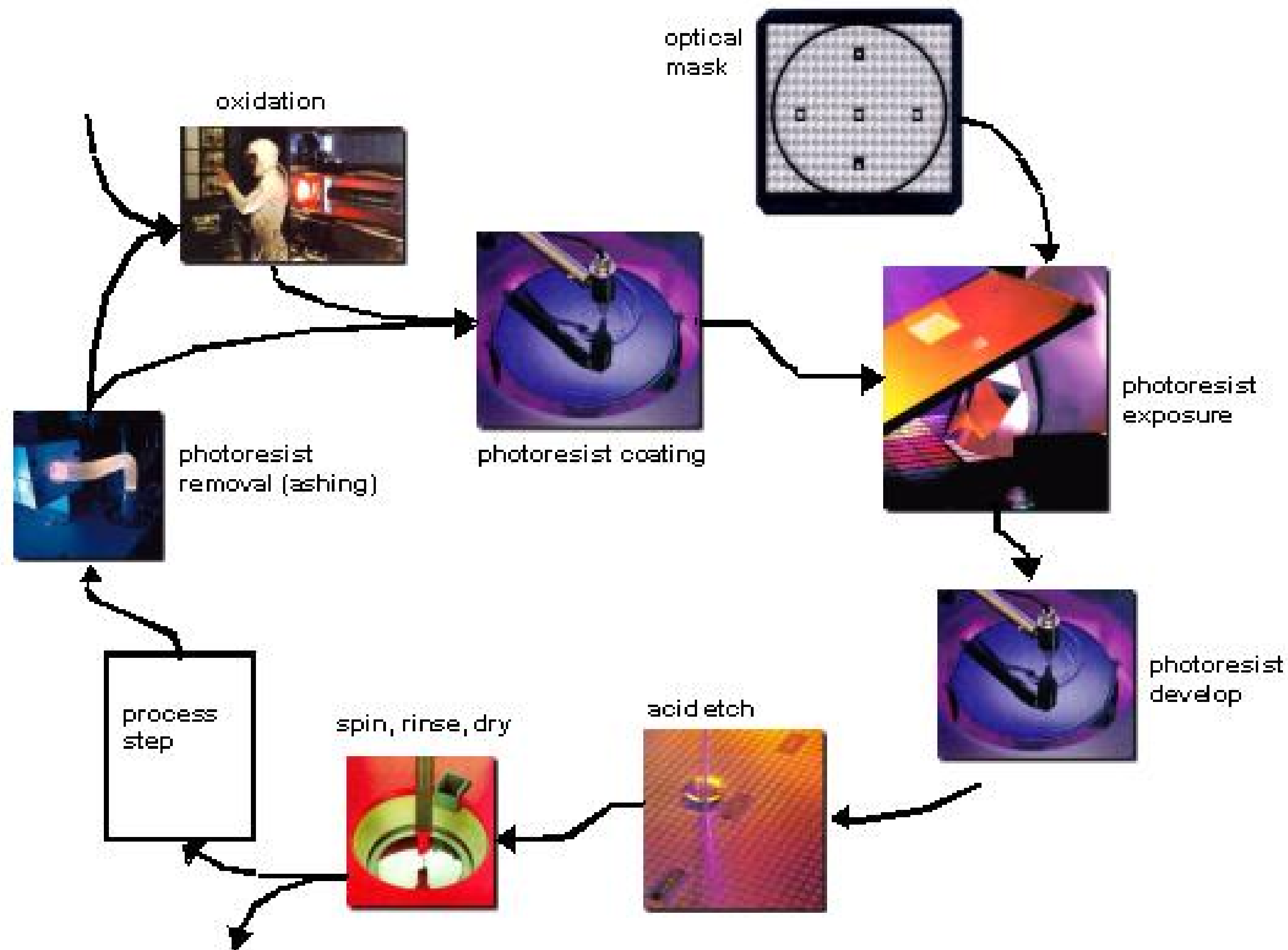
Planar processing consists of a sequence of **additive** and **subtractive** steps with **lateral patterning**

Lithography refers to the process of transferring a pattern to the surface of the wafer

Equipment, materials, and processes needed:

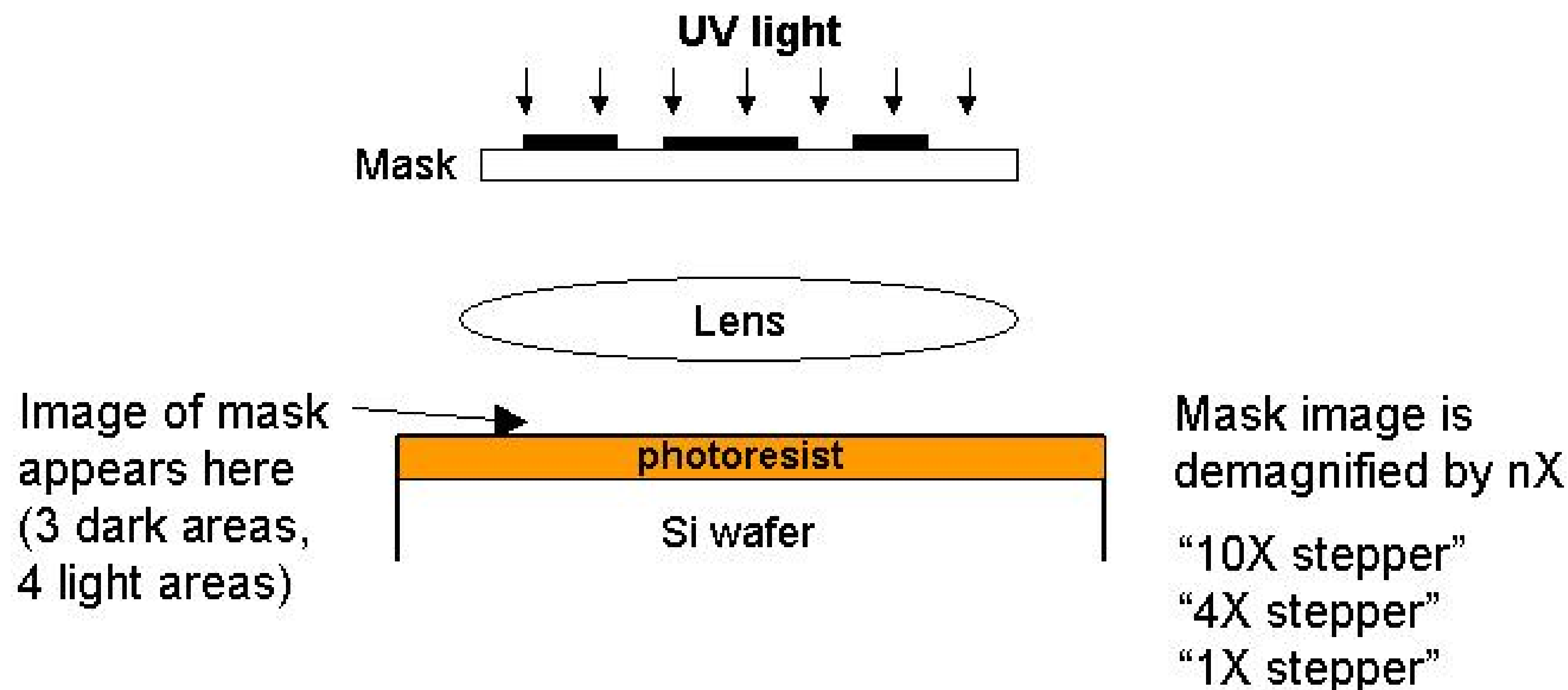
- A mask (for each layer to be patterned) with the desired pattern
- A light-sensitive material (called ***photoresist***) covering the wafer so as to receive the pattern
- A light source and method of projecting the image of the mask onto the photoresist ("*printer*" or "*projection stepper*" or "*projection scanner*")
- A method of "developing" the photoresist, that is selectively removing it from the regions where it was exposed

The Photo-Lithographic Process



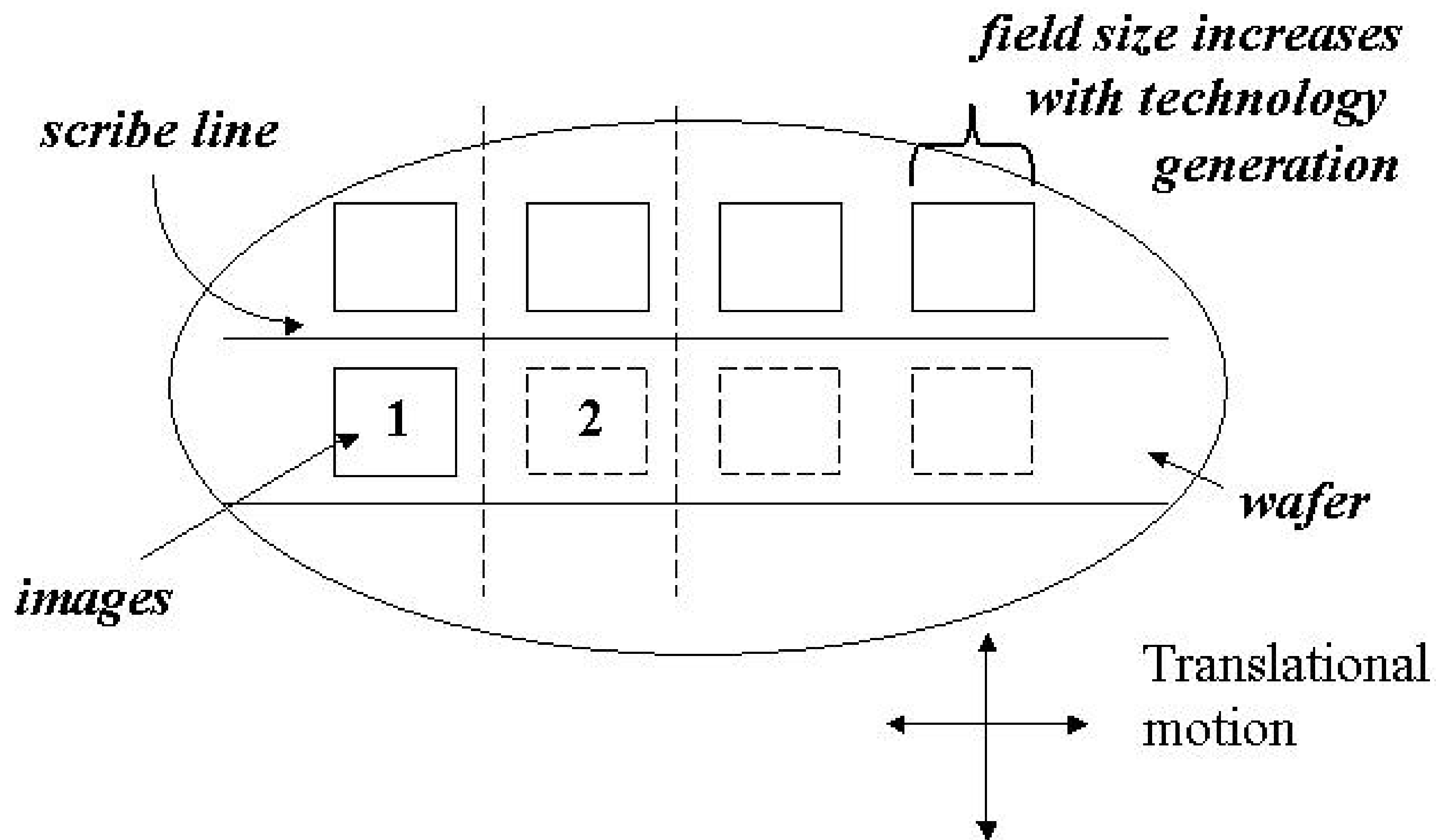
Photoresist Exposure

- A glass mask with a black/clear pattern is used to expose a wafer coated with ~1 μm thick photoresist



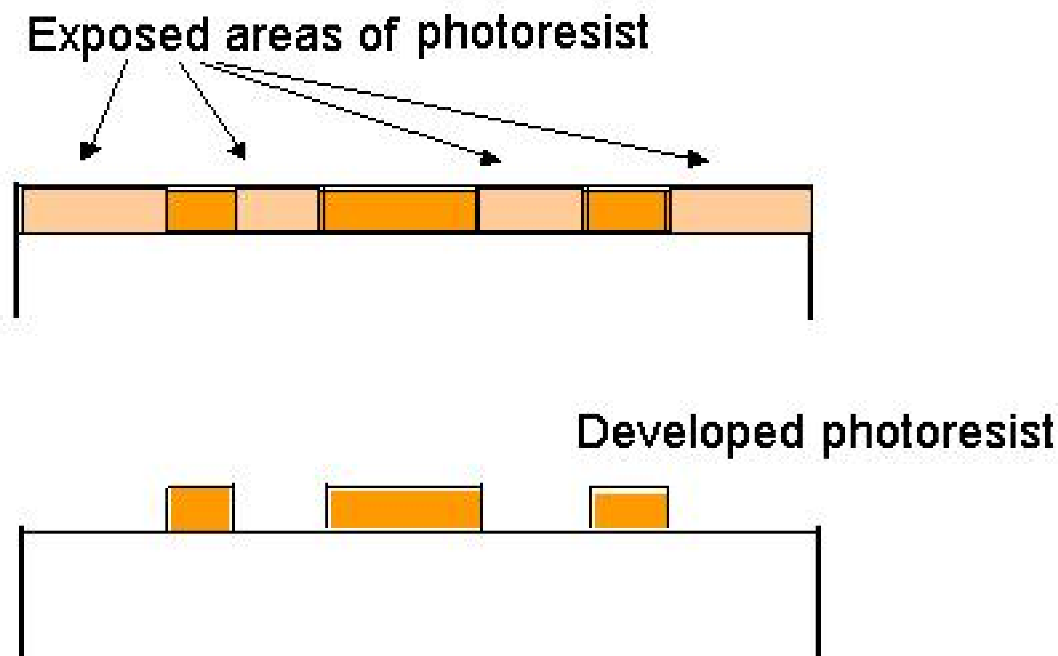
Areas exposed to UV light are susceptible to chemical removal

Exposure using "Stepper" Tool



Photoresist Development

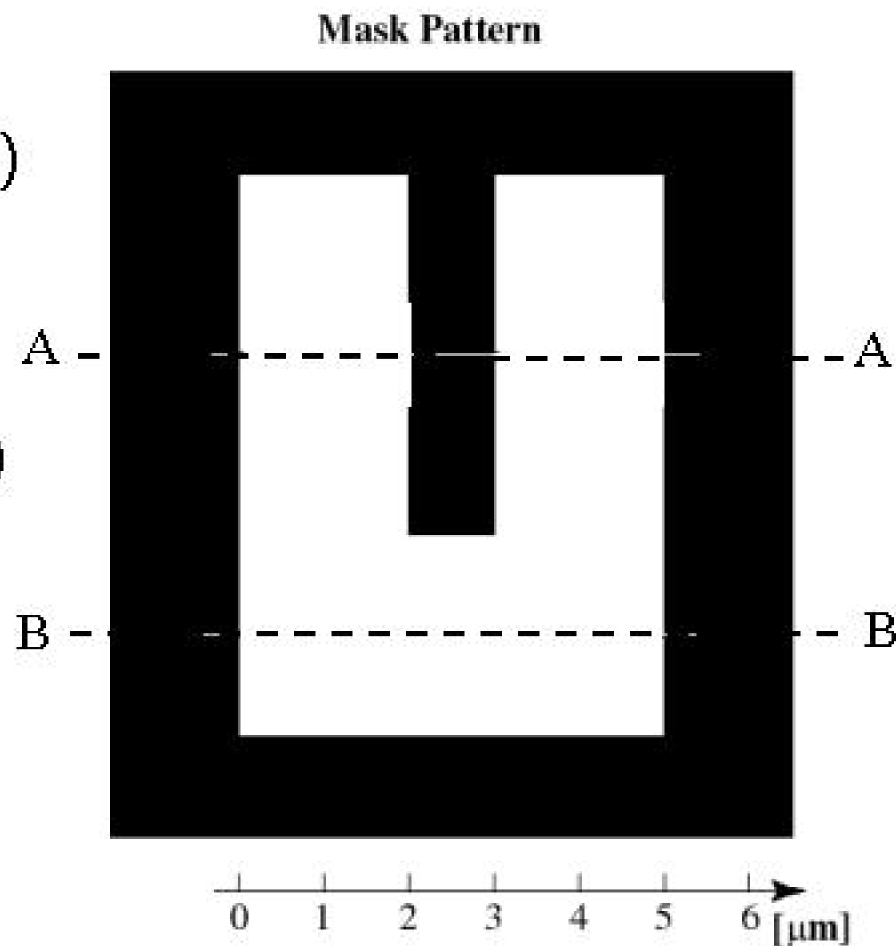
- Solutions with high pH dissolve the areas which were exposed to UV light; unexposed areas are not dissolved



Lithography Example

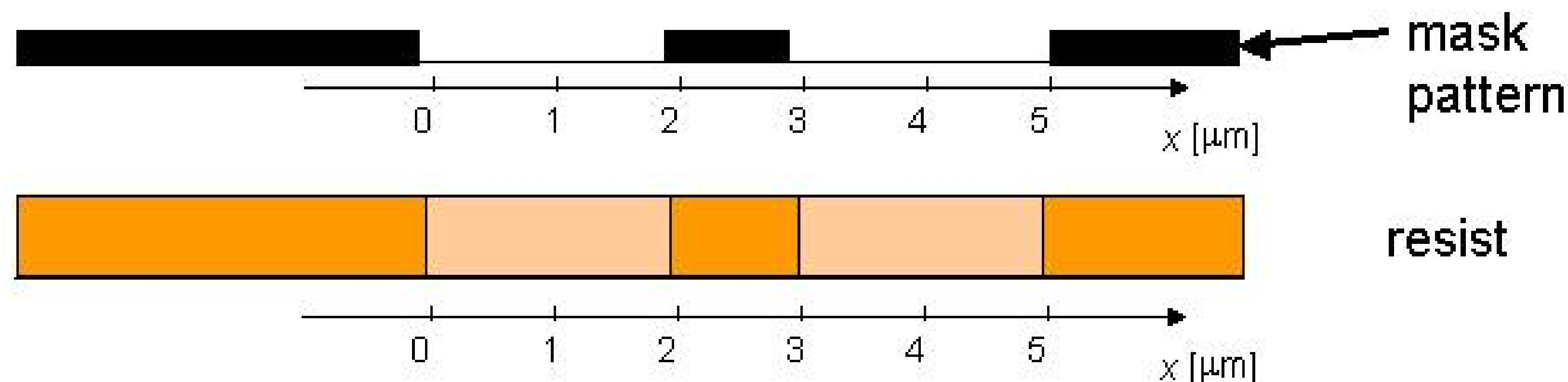
- Mask pattern (on glass plate)
- Look at cuts (cross sections) at various planes

  (*A*-*A* and *B*-*B*)

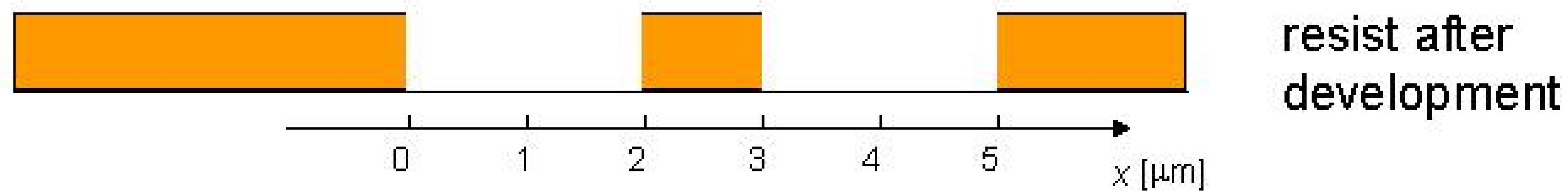


"A-A" Cross-Section

The resist is exposed in the ranges $0 < x < 2$ μm & $3 < x < 5$ μm:

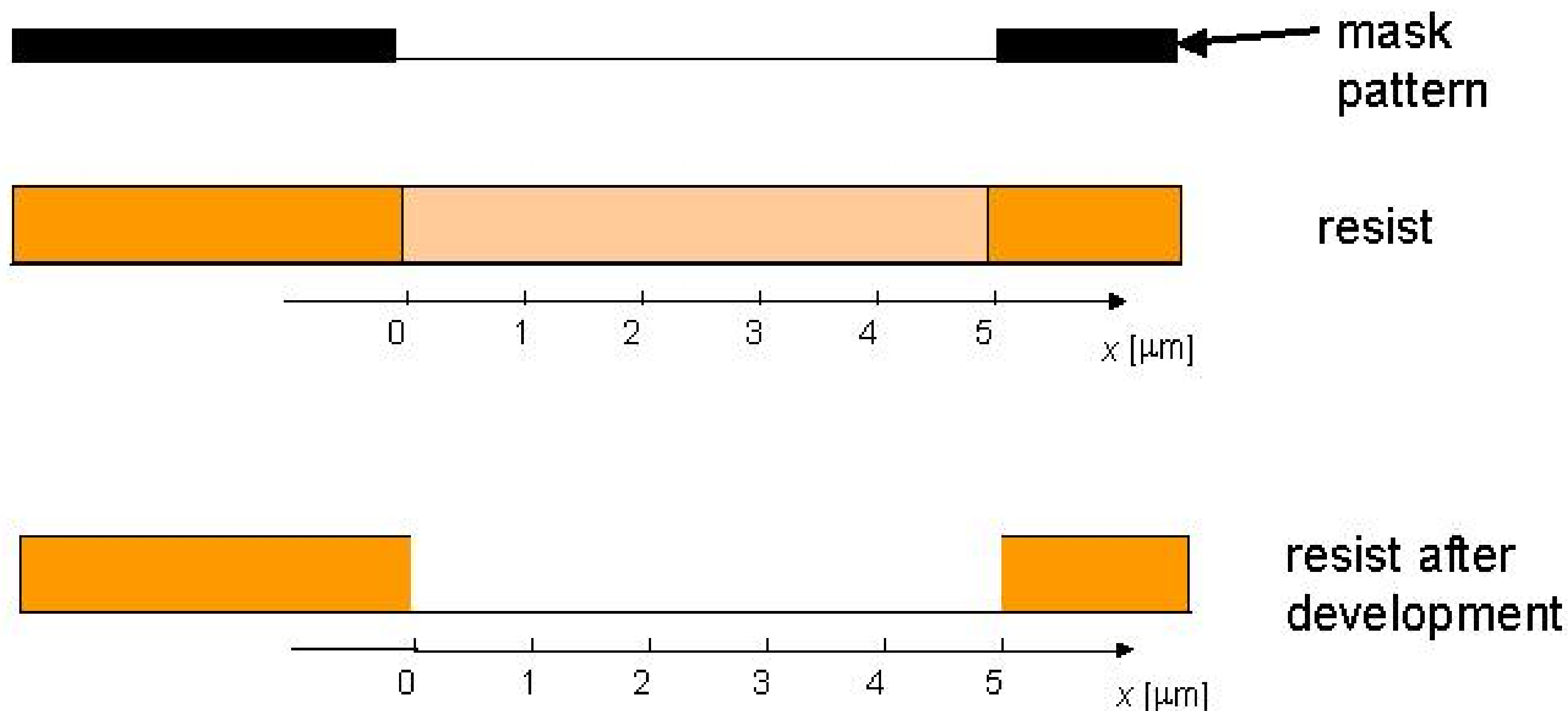


The resist will dissolve in high pH solutions wherever it was exposed:



"B-B" Cross-Section

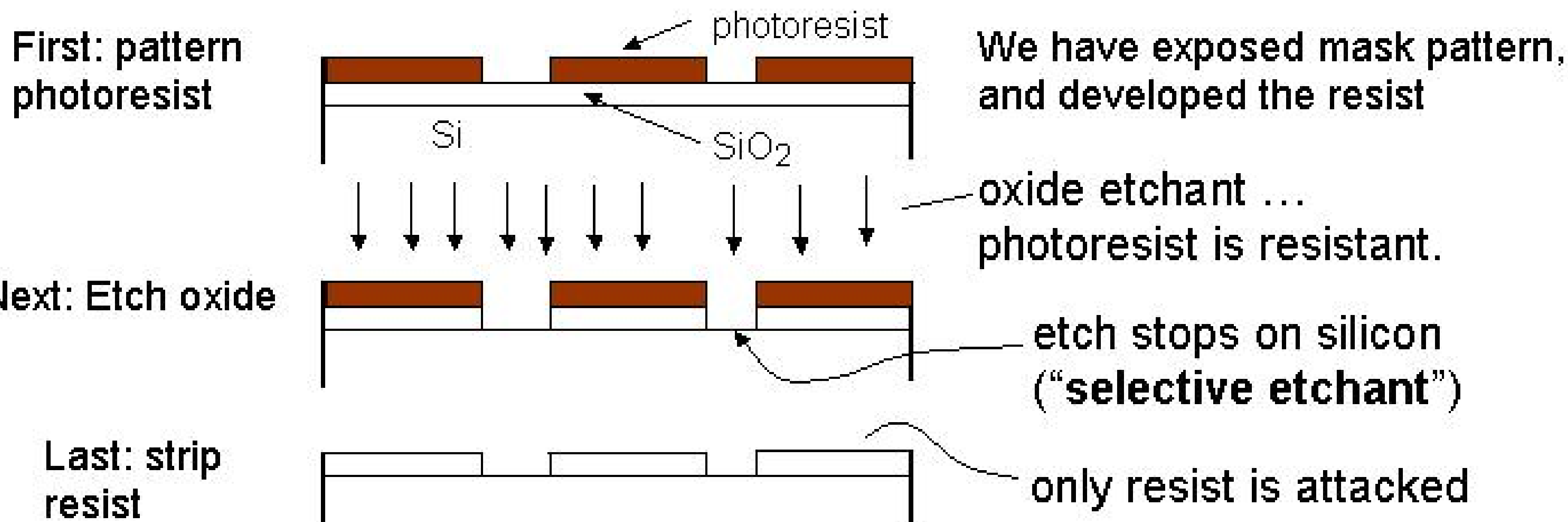
The photoresist is exposed in the ranges 0 < *x* < 5 μm:



Pattern Transfer by Etching

In order to transfer the photoresist pattern to an underlying film, we need a "subtractive" process that removes the film, ideally with minimal change in the pattern and with minimal removal of the underlying material(s)

→ **Selective etch processes (using plasma or aqueous chemistry) have been developed for most IC materials**



Jargon for this entire sequence of process steps: "pattern using XX mask"