Lecture #24

OUTLINE

- **Modern IC Fabrication Technology**
  - Doping
  - Oxidation
  - Thin-film deposition
  - Lithography
  - Etch
  - Lithography trends
  - Plasma processing
  - Chemical mechanical polishing

Reading (Rabaey *et al.*)

(Finish Chapter 2.2)

Integrated Circuit Fabrication

Goal:

Mass fabrication (*i.e.* simultaneous fabrication) of many "chips", each a circuit (e.g. a microprocessor or memory chip) containing millions or billions of transistors

Method:

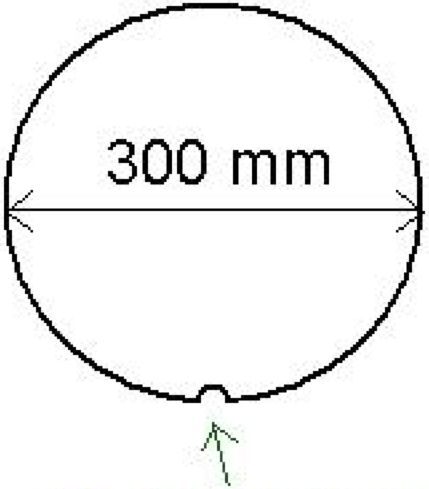
Lay down thin films of semiconductors, metals and insulators and pattern each layer with a process much like printing (lithography).

<u>Materials used in a basic CMOS integrated circuit:</u>

- Si substrate – selectively doped in various regions
- SiO_2 insulator
- Polycrystalline silicon – used for the gate electrodes
- Metal contacts and wiring

Si Substrates (Wafers)

Crystals are grown from a melt in boules (cylinders) with specified dopant concentrations. They are ground perfectly round and oriented (a "flat" or "notch" is ground along the boule) and then sliced like baloney into wafers. The wafers are then polished.



"notch" indicates crystal orientation

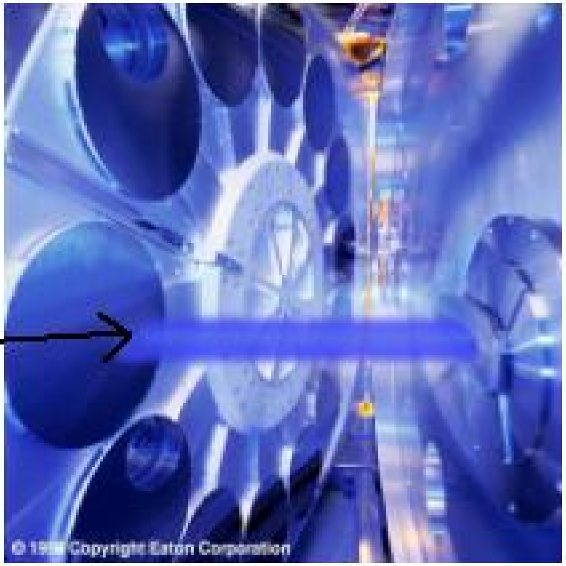
Typical wafer cost: $50

Sizes: 150 mm, 200 mm, 300 mm diameter

Adding Dopants into Si

Suppose we have a wafer of Si which is p-type and we want to change the surface to n-type. The way in which this is done is by *ion implantation*. Dopant ions are shot out of an "ion gun" called an *ion implanter,* into the surface of the wafer.

Eaton HE3 High-Energy Implanter, showing the ion beam hitting the end-station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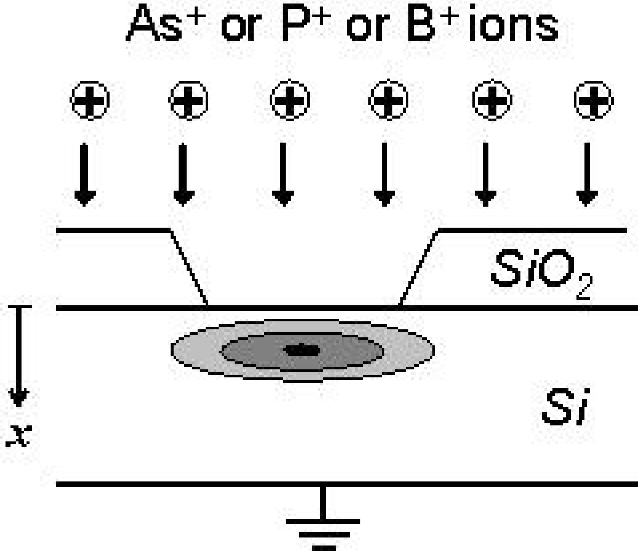
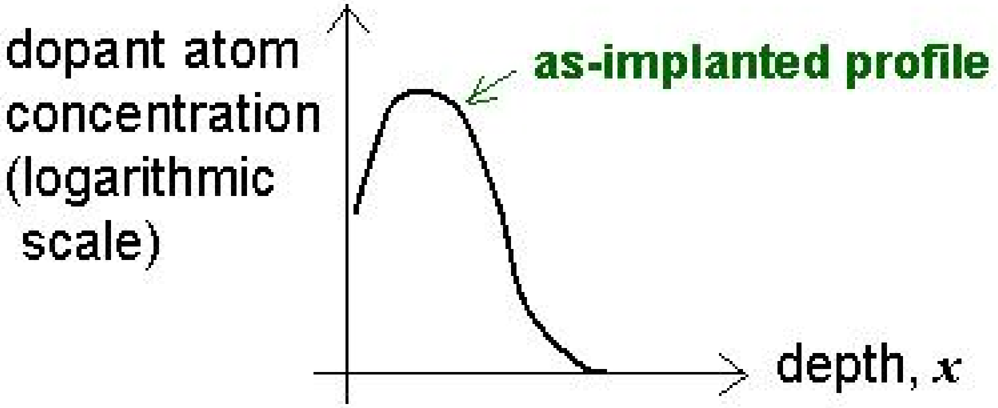
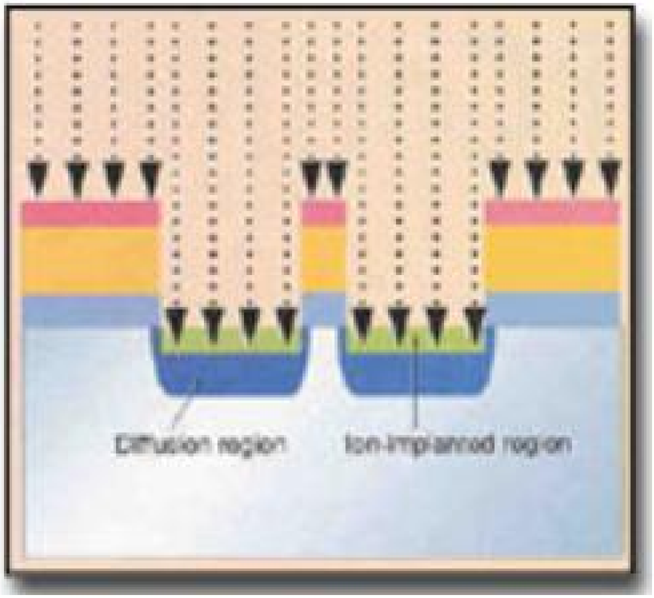


Typical implant energies are in the range 1-200 keV. After the ion implantation, the wafers are heated to a high temperature (~1000°C). This "annealing" step heals the damage and causes the implanted dopant atoms to move into substitutional lattice sites.

Dopant Diffusion

- The implanted depth-profile of dopant atoms is peaked.





- In order to achieve a more uniform dopant profile, high-temperature annealing is used to diffuse the dopants
- Dopants can also be directly introduced into the surface of a wafer by diffusion (rather than by ion implantation) from a dopant-containing ambient or doped solid source

Formation of Insulating Films

- The favored insulator is pure silicon dioxide (SiO_2).
- A SiO_2 film can be formed by one of two methods:

1. Oxidation of Si at high temperature in O_2 or steam ambient
2. Deposition of a silicon dioxide film

ASM A412 batch oxidation furnace

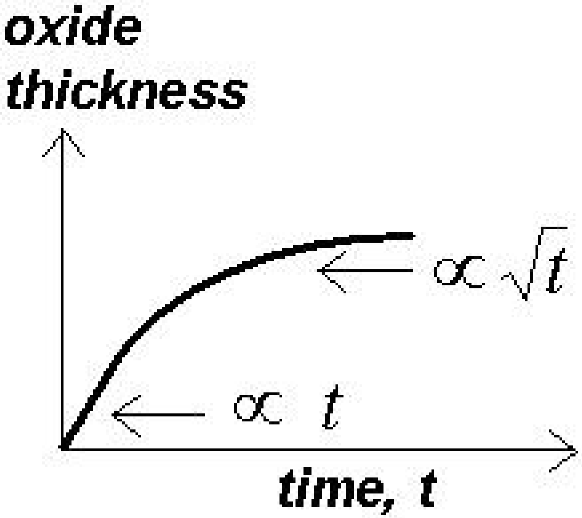
Applied Materials low-pressure chemical-vapor deposition (CVD) chamber

Thermal Oxidation

$Si + O_2 \rightarrow SiO_2$ **or** $Si + 2H_2O \rightarrow SiO_2 + 2H_2$

"dry" oxidation "wet" oxidation

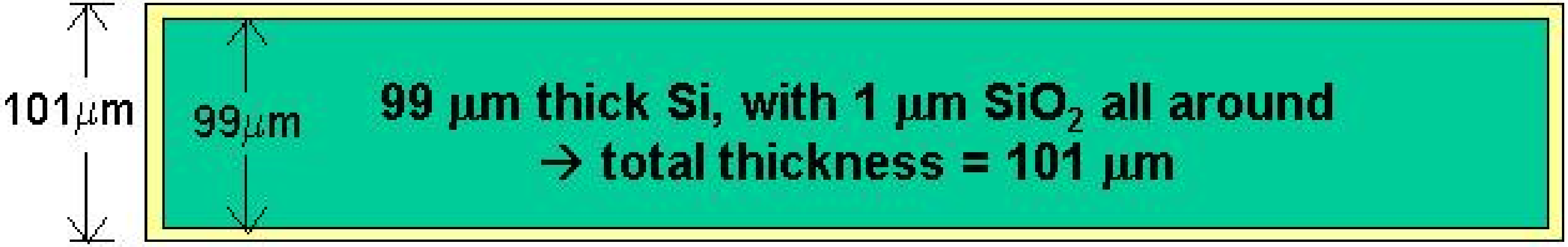
- **Temperature range:**
  - 700°C to 1100°C
- **Process:**
  - O_2 or H_2O diffuses through SiO_2 and reacts with Si at the interface to form more SiO_2
- **1 μm of SiO_2 formed consumes ~0.5 μm of Si**



Example: Thermal Oxidation of Silicon

Silicon wafer, 100 μm thick

Thermal oxidation grows SiO_2 on Si, but it consumes Si, so the wafer gets thinner. Suppose we grow 1 μm of oxide:

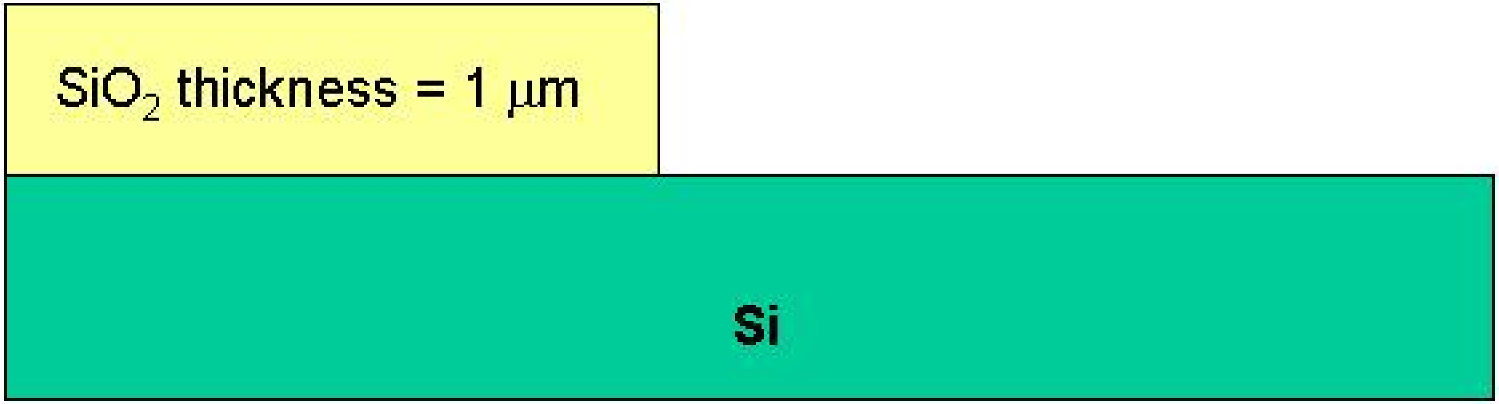


99 μm thick Si, with 1 μm SiO_2 all around
→ total thickness = 101 μm

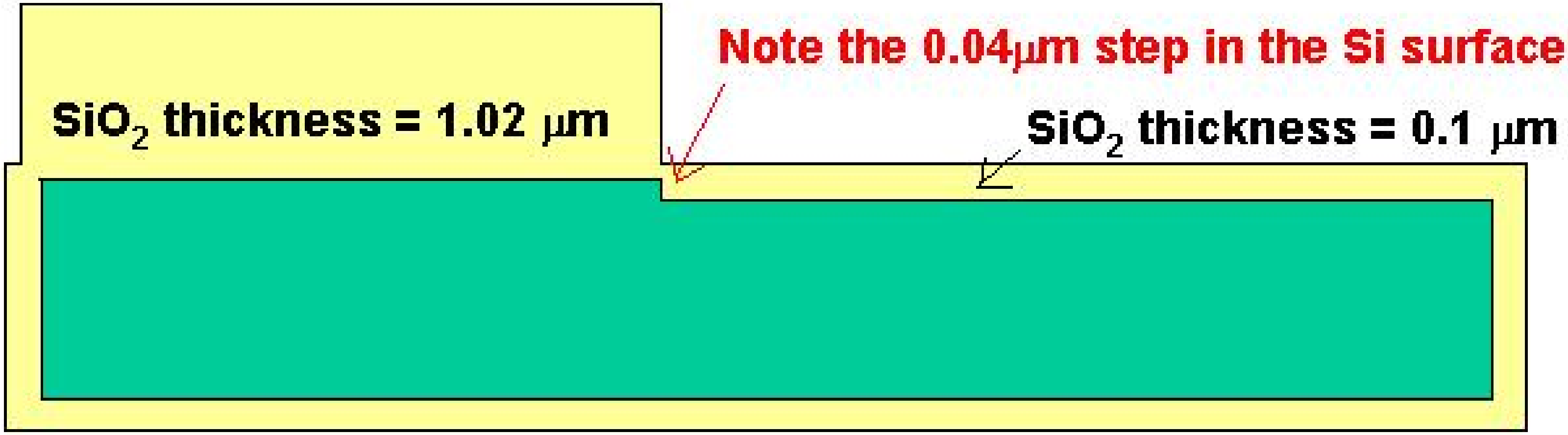
Effect of Oxidation Rate Dependence on Thickness

- **The thermal oxidation rate slows with oxide thickness.**

Consider a Si wafer with a patterned oxide layer:

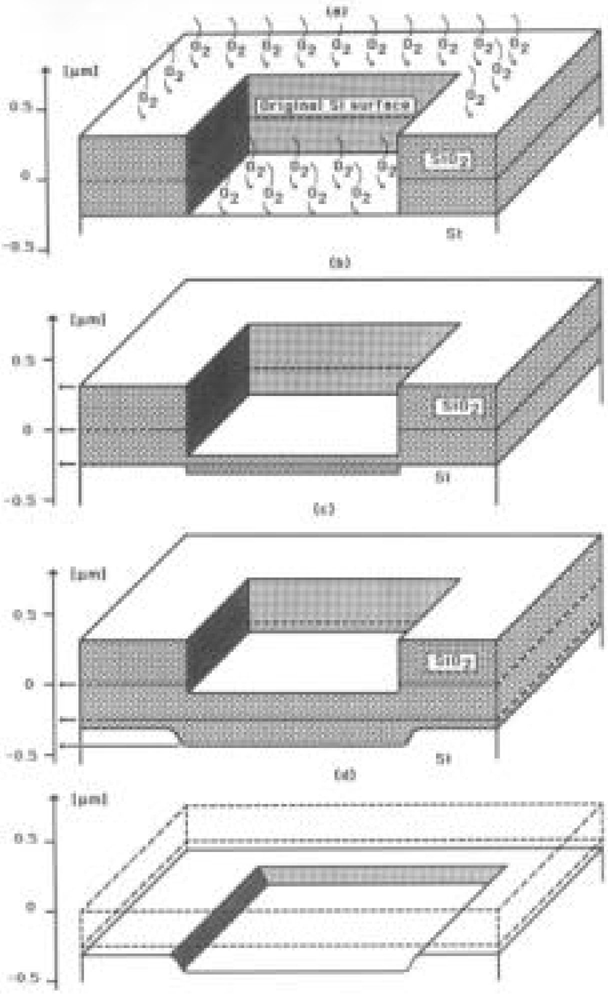


Now suppose we grow 0.1 μm of SiO_2:

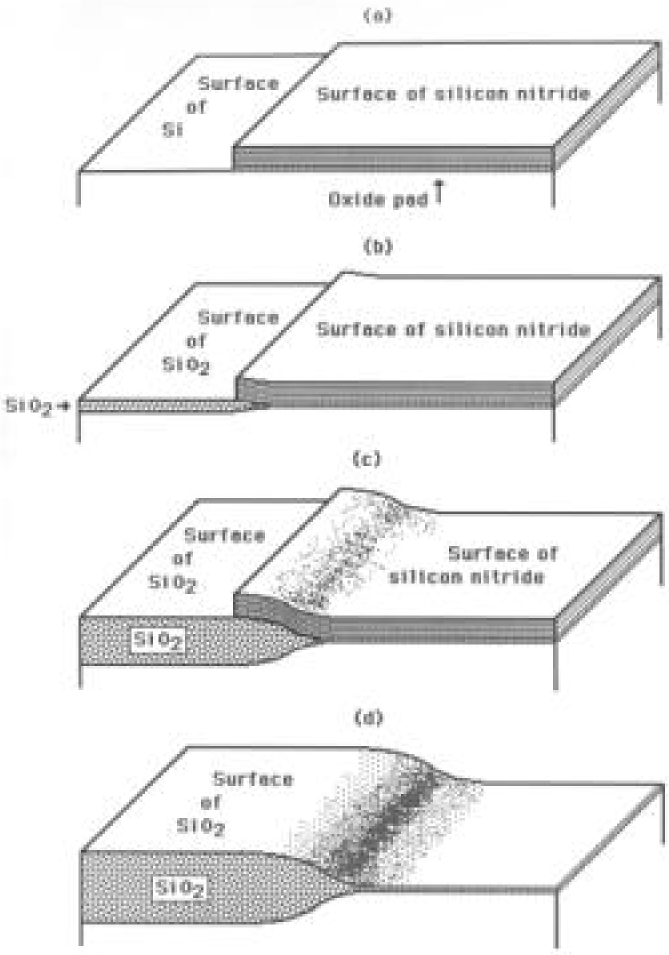


Selective Oxidation Techniques

Window Oxidation



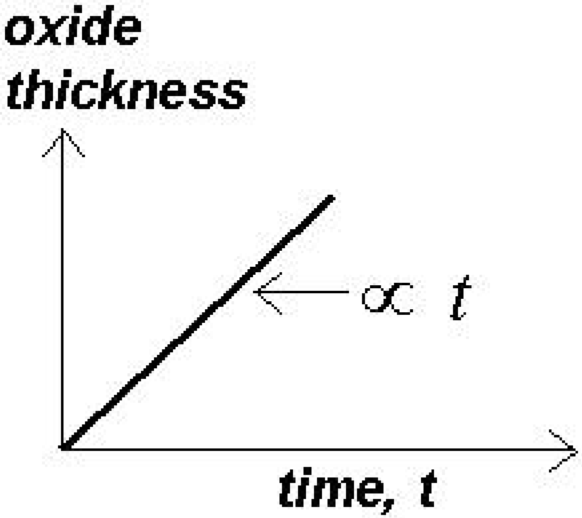
Local Oxidation (LOCOS)



Chemical Vapor Deposition (CVD) of SiO_2

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$ "LTO"

- **Temperature range:**
  - 350°C to 450°C for silane
- **Process:**
  - Precursor gases dissociate at the wafer surface to form SiO_2
  - No Si on the wafer surface is consumed
- **Film thickness is controlled by the deposition time**



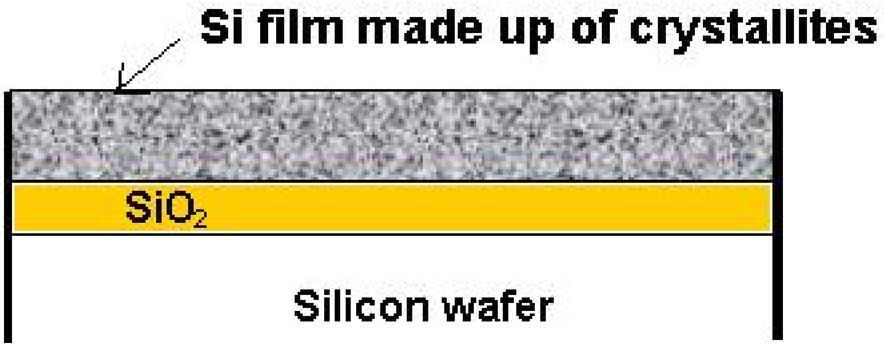
Chemical Vapor Deposition (CVD) of Si

Polycrystalline silicon ("poly-Si"):

Like SiO_2, Si can be deposited by **C**hemical **V**apor **D**eposition:

- Wafer is heated to ~600°C
- Silicon-containing gas (SiH_4) is injected into the furnace:

$$SiH_4 \quad = \quad Si + 2H_2$$



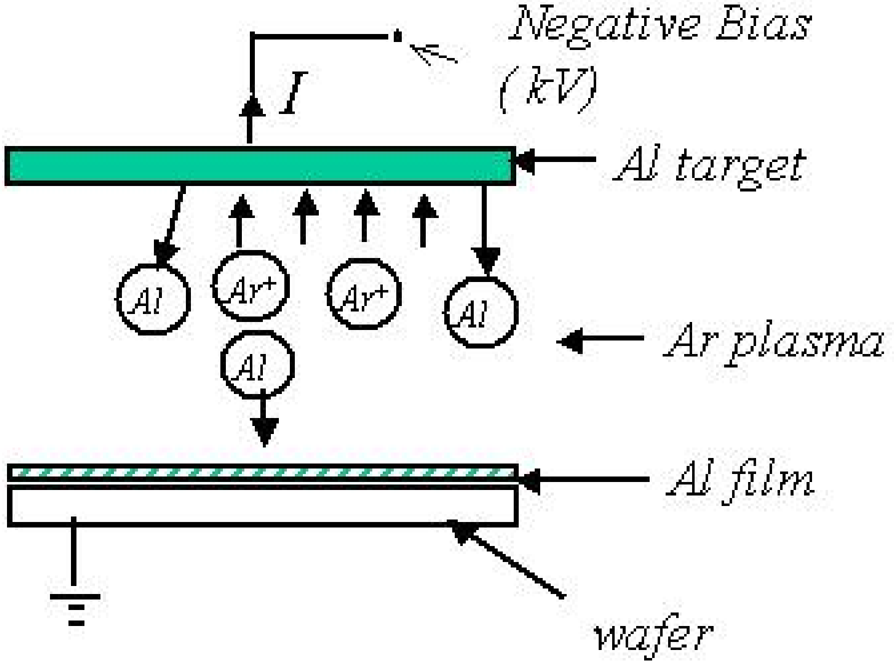
<u>Properties</u>:

- **sheet resistance (heavily doped, 0.5 μm thick) = 20 Ω/□**
- **can withstand high-temperature anneals → major advantage**

Physical Vapor Deposition ("Sputtering")

Used to deposit Al films:

Highly energetic argon ions batter the surface of a metal target, knocking atoms loose, which then land on the surface of the wafer



Sometimes the substrate is heated, to ~300ºC

Gas pressure: 1 to 10 mTorr

Deposition rate $\propto I \bullet S$

sputtering yield

ion current

Patterning the Layers

Planar processing consists of a sequence of **additive** and **subtractive** steps with **lateral patterning**

oxidation
deposition
ion implantation

etching

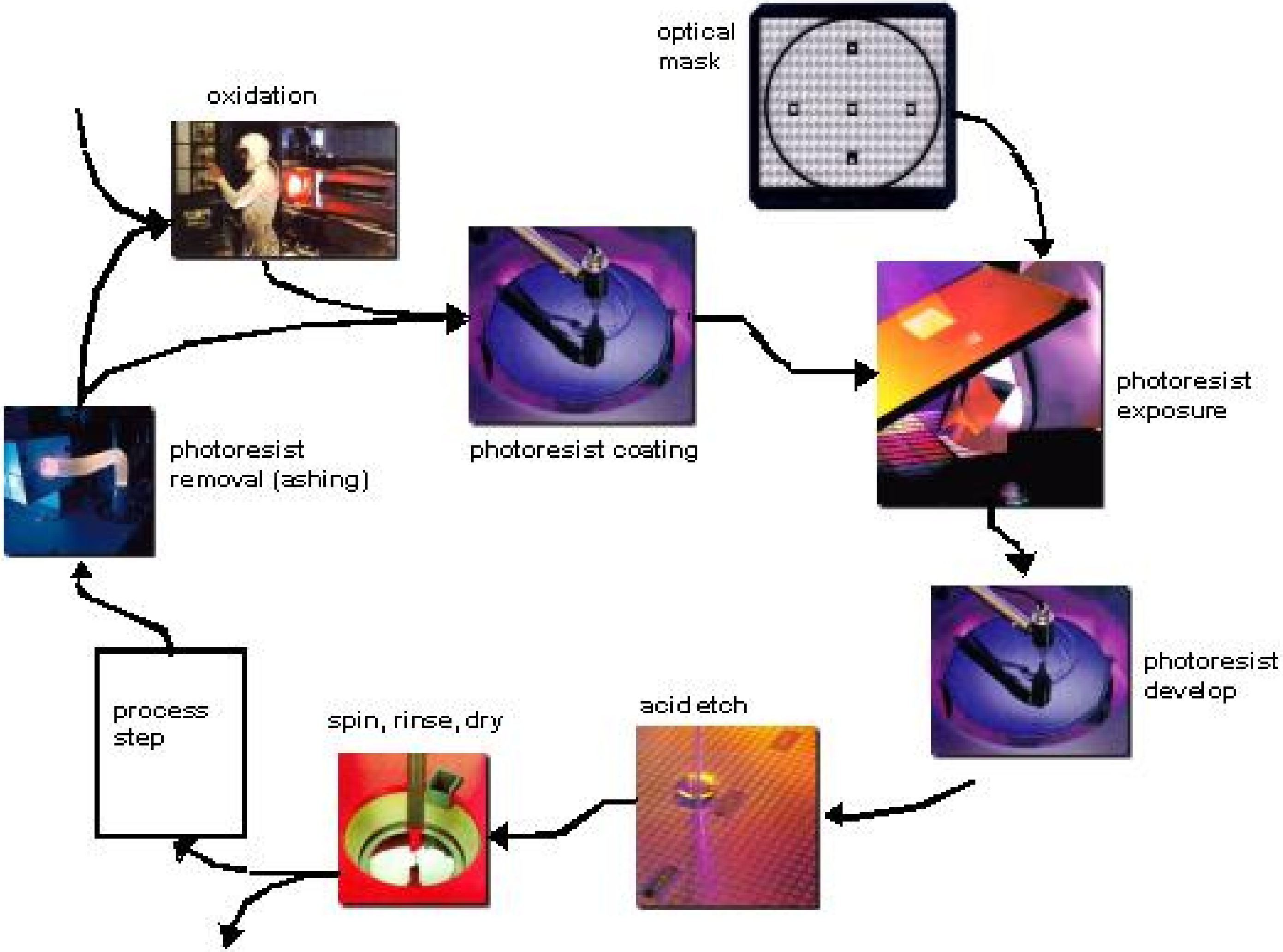
lithography

Lithography refers to the process of transferring a pattern to the surface of the wafer

Equipment, materials, and processes needed:

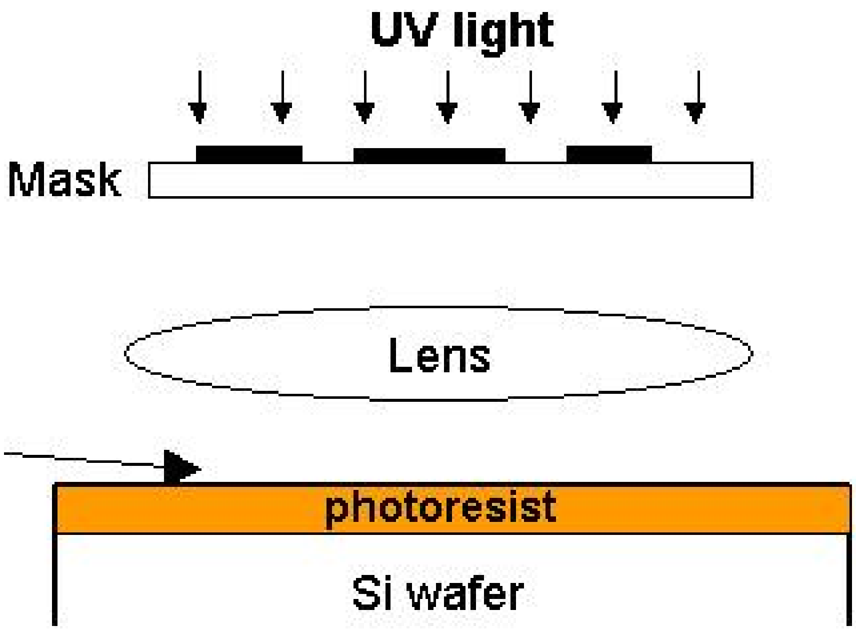
- A mask (for each layer to be patterned) with the desired pattern
- A light-sensitive material (called ***photoresist***) covering the wafer so as to receive the pattern
- A light source and method of projecting the image of the mask onto the photoresist (“*printer*” or “*projection stepper*” or “*projection scanner*”)
- A method of “developing” the photoresist, that is selectively removing it from the regions where it was exposed

The Photo-Lithographic Process



Photoresist Exposure

- A glass mask with a black/clear pattern is used to expose a wafer coated with ~1 μm thick photoresist



UV light

Mask

Lens

photoresist

Si wafer

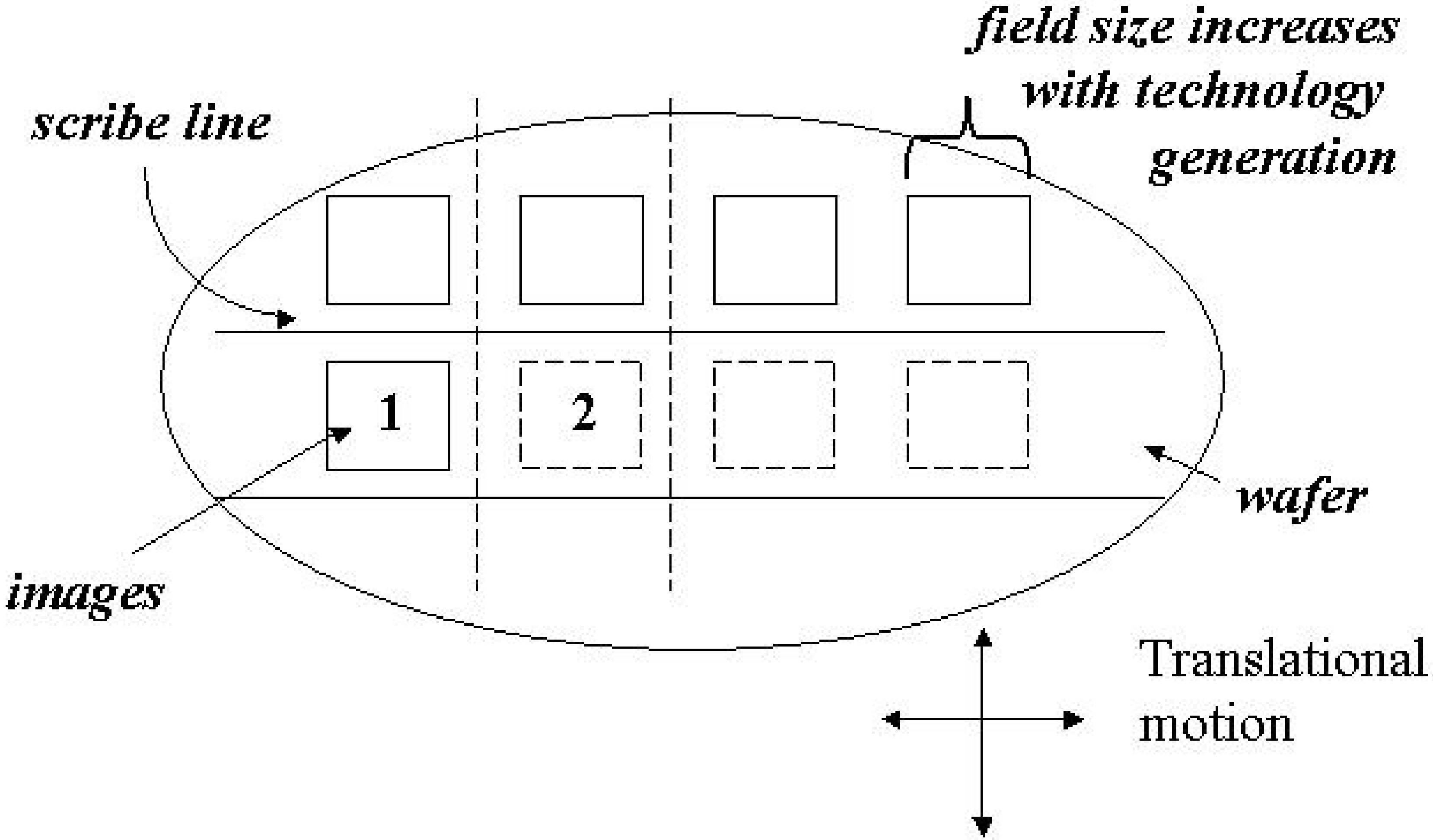
Image of mask appears here (3 dark areas, 4 light areas)

Mask image is demagnified by nX

"10X stepper"
"4X stepper"
"1X stepper"

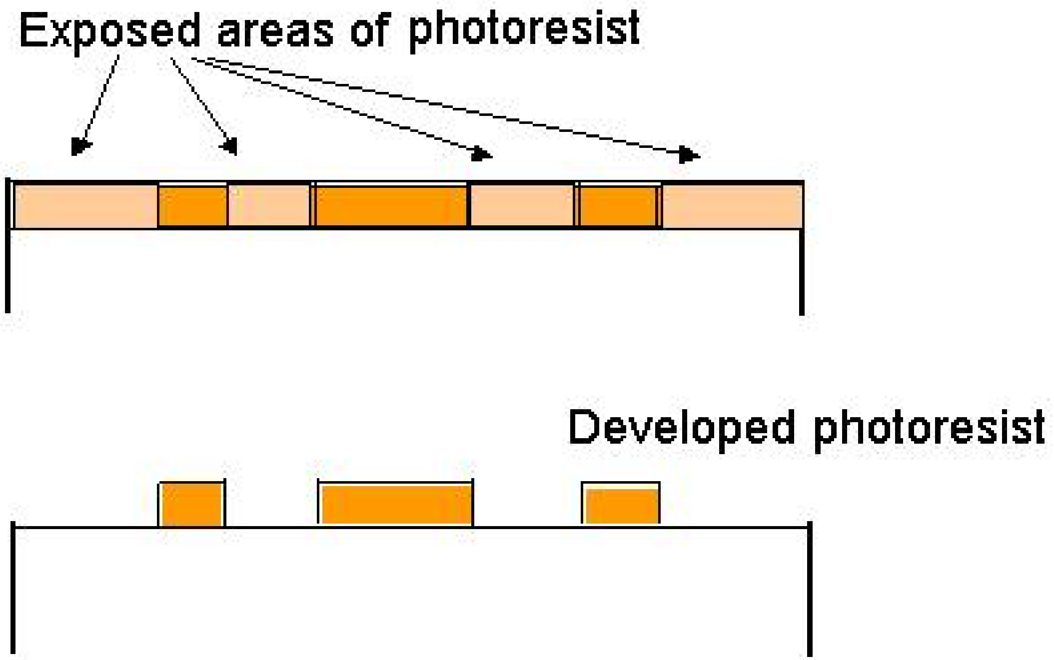
Areas exposed to UV light are susceptible to chemical removal

Exposure using "Stepper" Tool



Photoresist Development

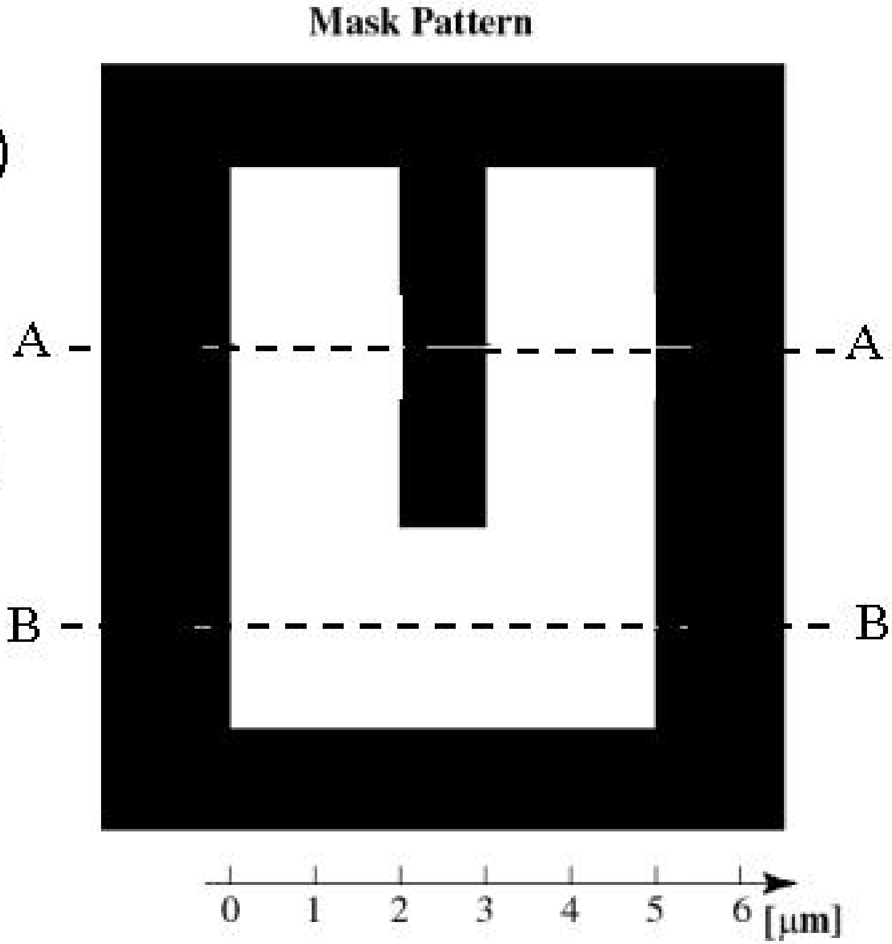
- Solutions with high pH dissolve the areas which were exposed to UV light; unexposed areas are not dissolved



Lithography Example

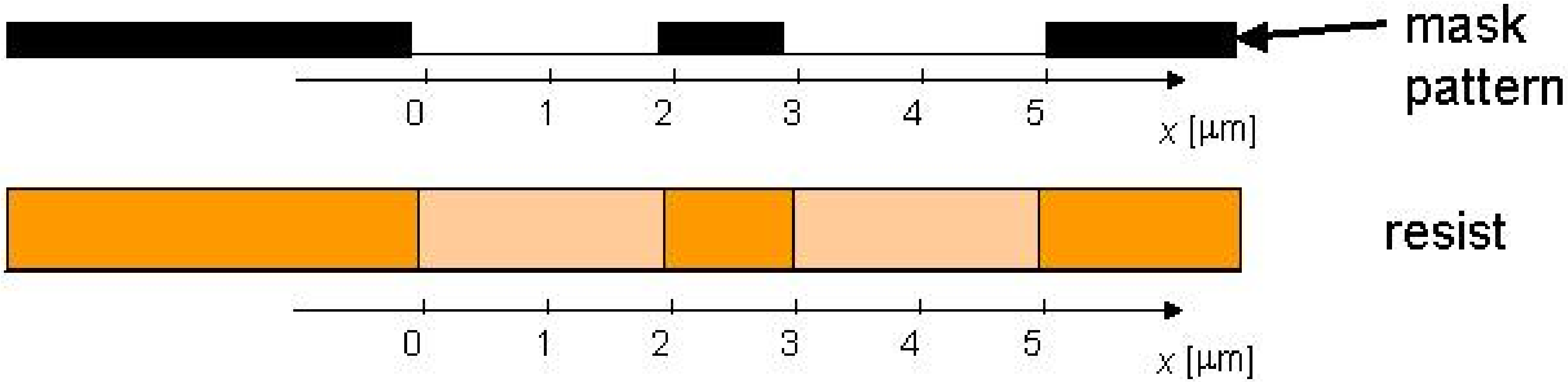
- Mask pattern (on glass plate)
- Look at cuts (cross sections) at various planes

  (*A*-*A* and *B*-*B*)



"A-A" Cross-Section

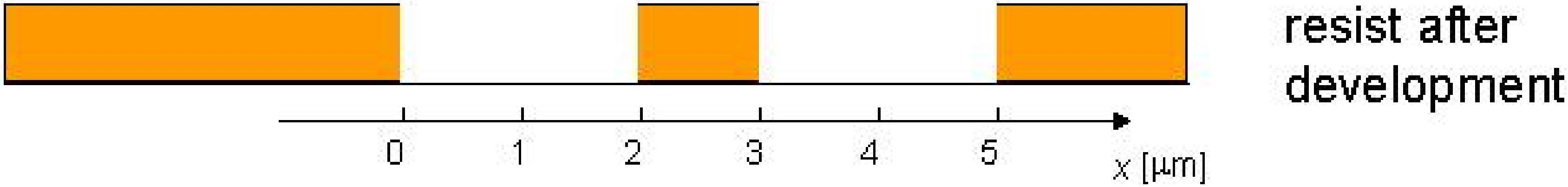
The resist is exposed in the ranges $0 < x < 2\ \mu m$ & $3 < x < 5\ \mu m$:



mask pattern

resist

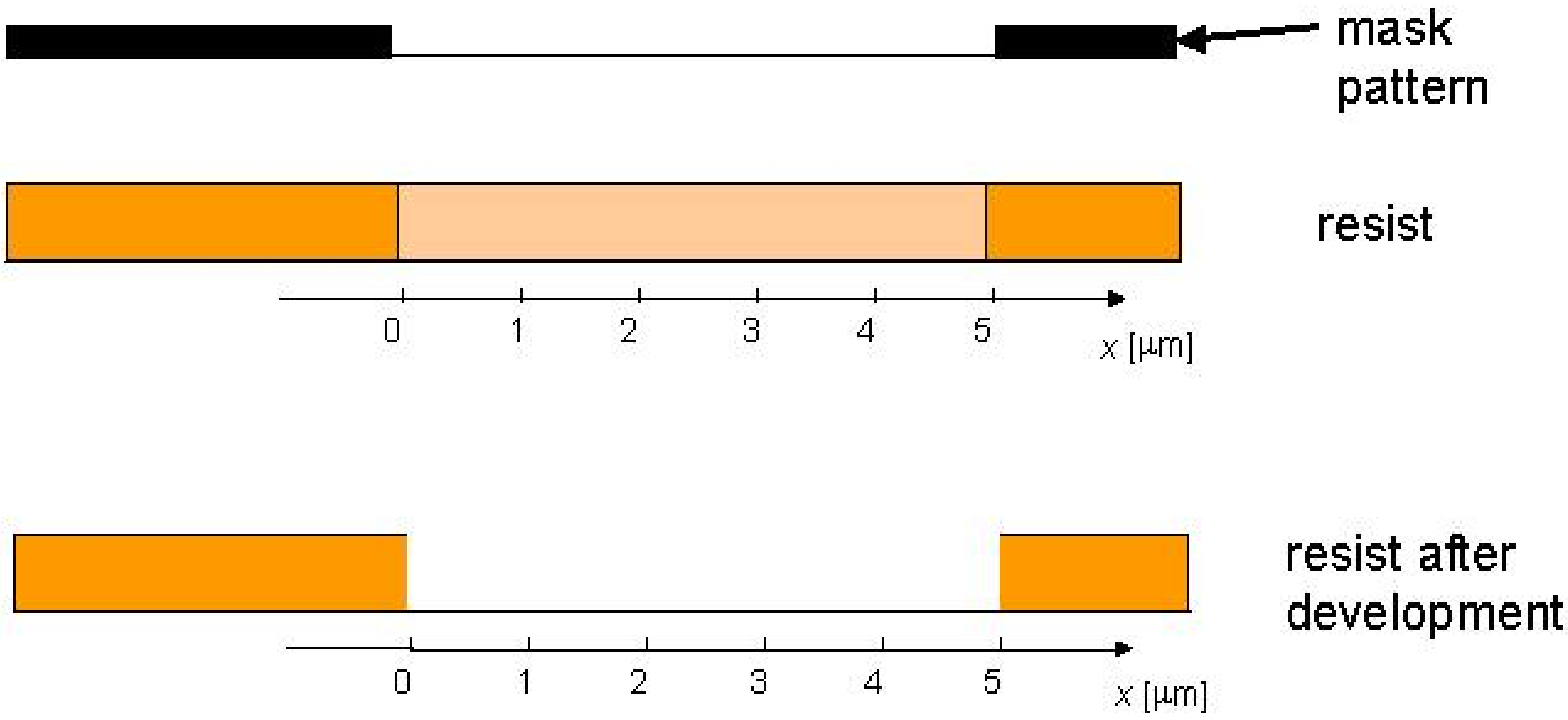
The resist will dissolve in high pH solutions wherever it was exposed:



resist after development

“B-B” Cross-Section

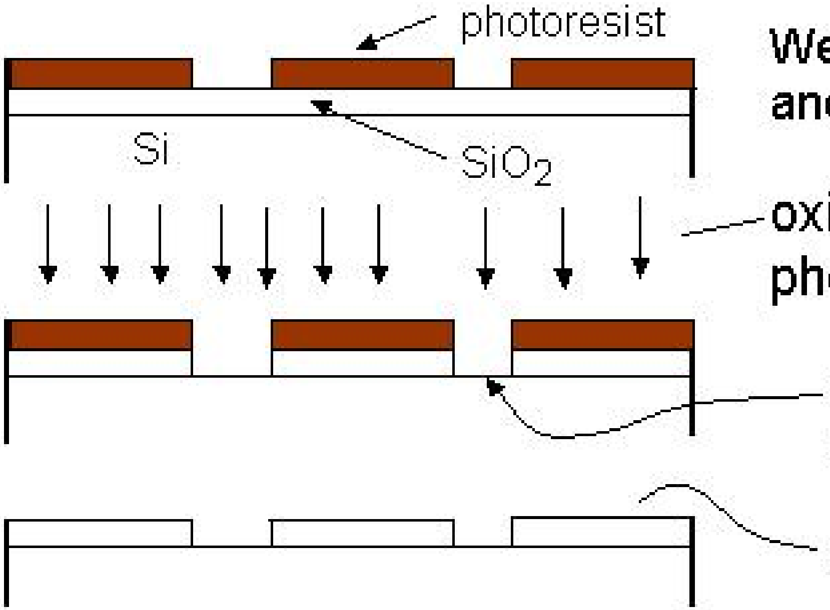
The photoresist is exposed in the ranges $0 < x < 5\ \mu m$:



Pattern Transfer by Etching

In order to transfer the photoresist pattern to an underlying film, we need a "subtractive" process that removes the film, ideally with minimal change in the pattern and with minimal removal of the underlying material(s)

→ **<u>Selective</u> etch processes (using plasma or aqueous chemistry) have been developed for most IC materials**



First: pattern photoresist

We have exposed mask pattern, and developed the resist

oxide etchant … photoresist is resistant.

Next: Etch oxide

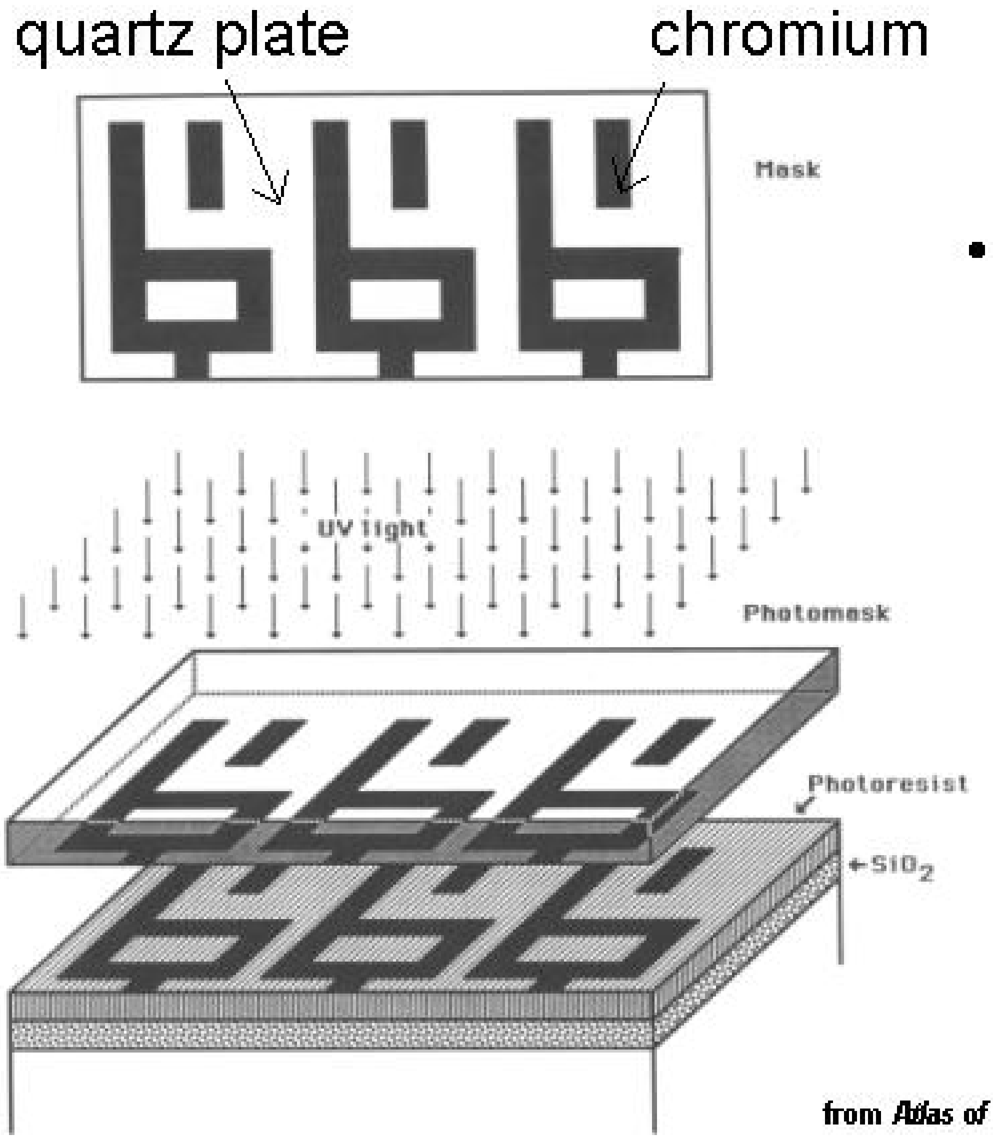
etch stops on silicon ("**selective etchant**")

Last: strip resist

only resist is attacked

Jargon for this entire sequence of process steps: "pattern using XX mask"

Photolithography



- 2 types of photoresist:
  - positive tone:

    portion exposed to light will be dissolved in developer solution
  - negative tone:

    portion exposed to light will NOT be dissolved in developer solution

from ***Atlas of IC Technologies*** by W. Maly

Lithography Trends

- **Lithography determines the minimum feature size and limits the throughput that can be achieved in an IC manufacturing process. Thus, lithography research & development efforts are directed at**

1. **achieving higher resolution**

   → shorter wavelengths

   365 nm → 248 nm → 193 nm → 13 nm
   "i-line" "DUV" "EUV"

2. **improving resist materials**

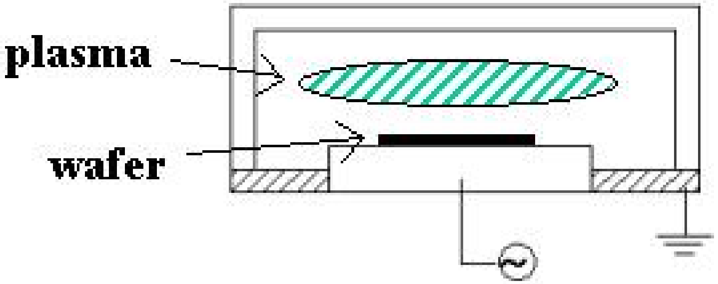
   → higher sensitivity, for shorter exposure times

   (throughput target is 60 wafers/hr)

Plasma Processing

- **Plasmas are used to enhance various processes:**
  - CVD: Energy from RF electric field assists the dissociation of gaseous molecules, to allow for thin-film deposition at higher rates and/or lower temperatures.
  - Etch: Ionized etchant species are more reactive and can be accelerated toward wafer (biased at negative DC potential), to provide directional etching for more precise transfer of lithographically defined features.

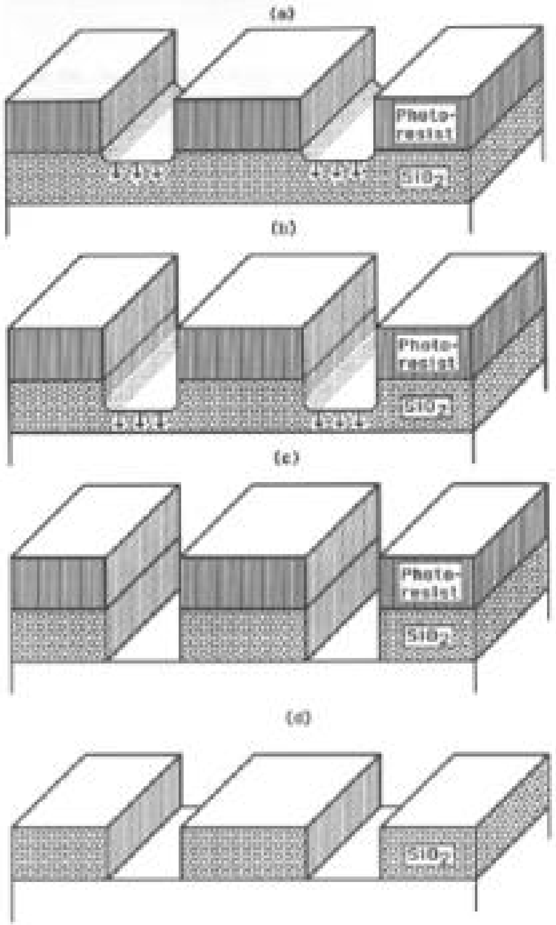
Reactive Ion Etcher



RF: 13.56 MHz

Dry Etching *vs.* Wet Etching

from *Atlas of IC Technologies* by W. Maly



Anisotropic
(e.g. Reactive Ion Etching)

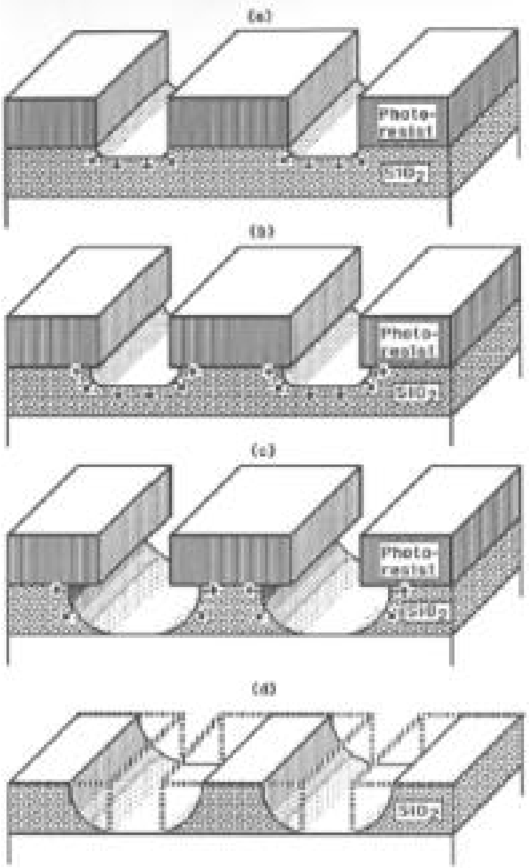
✓ better control of etched feature sizes

Pattern resist mask

Etching thin film

Etching completed

Remove resist mask



Isotropic
(e.g. Wet etching)

✓ better etch selectivity

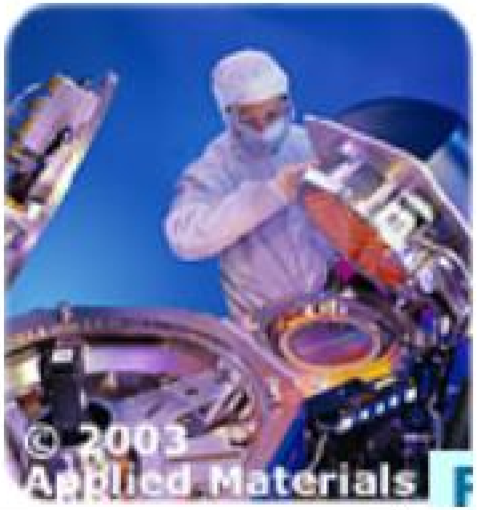
Rapid Thermal Annealing (RTA)

Sub-micron MOSFETs need ultra-shallow junctions (x_j<50 nm)

→ Dopant diffusion during "activation" anneal must be minimized

→ Short annealing time (<1 min.) at high temperature is required

- Ordinary furnaces (*e.g.* used for thermal oxidation and CVD) heat and cool wafers at a slow rate (<50°C per minute)
- Special annealing tools have been developed to enable much faster temperature ramping, and precise control of annealing time
  - ramp rates as fast as 200°C/second
  - anneal times as short as 0.5 second
  - typically single-wafer process chamber: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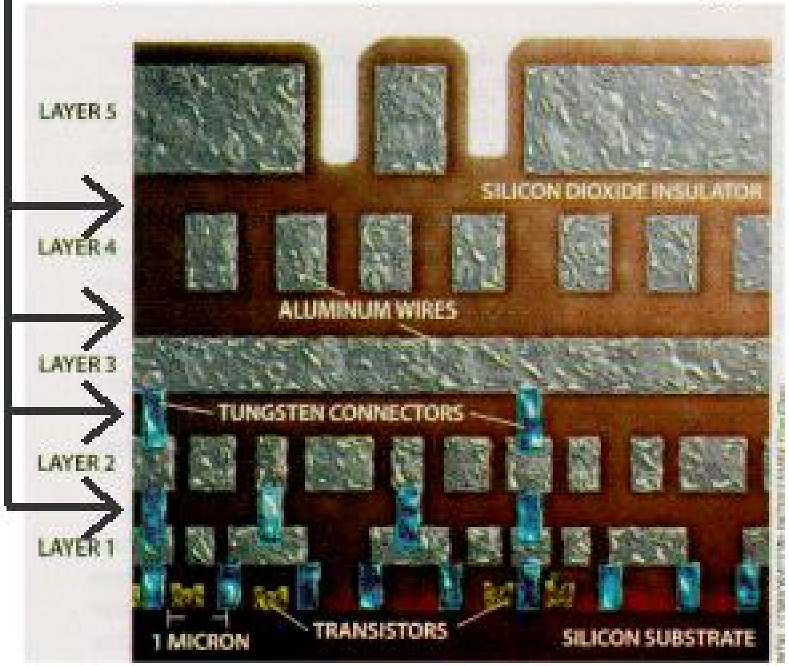
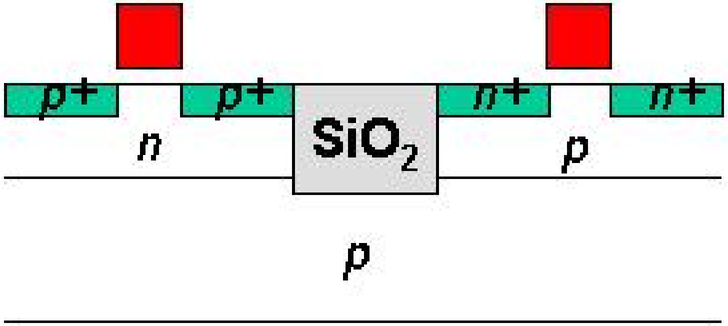
Chemical Mechanical Polishing (CMP)

- ***Chemical mechanical polishing*** is used to planarize the surface of a wafer at various steps in the process of fabricating an integrated circuit.
  - interlevel dielectric (ILD) layers
  - shallow trench isolation (STI)
  - copper metallization
    "damascene" process

IC with 5 layers of Al wiring



Oxide Isolation of Transistors



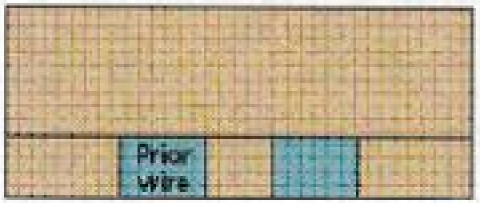
Copper Metallization

"Dual Damascene Process"

(IBM Corporation)

(1)

- Oxide deposition



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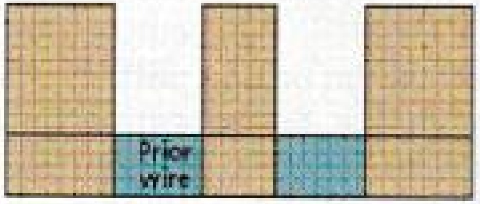
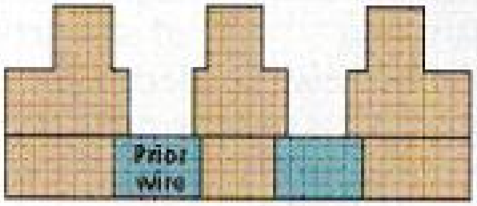
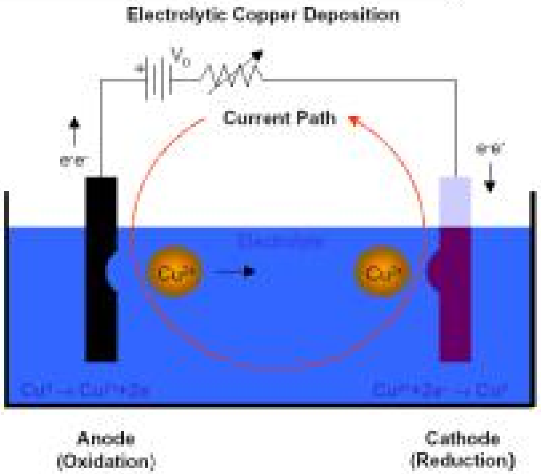
- Stud lithography and reactive ion etch



(3)

- Wire lithography and reactive ion etch

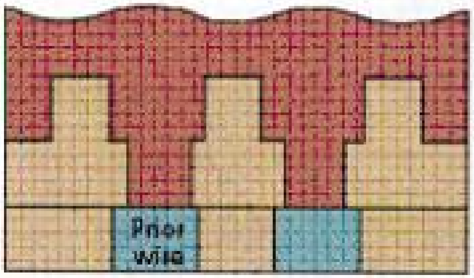




courtesy of Sung Gyu Pyo, Hynix Semiconductor

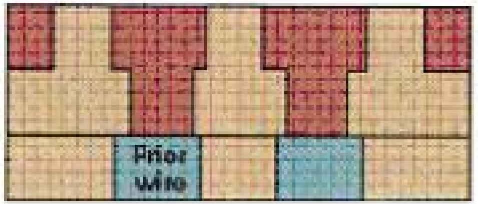
(4)

- Stud and wire metal deposition



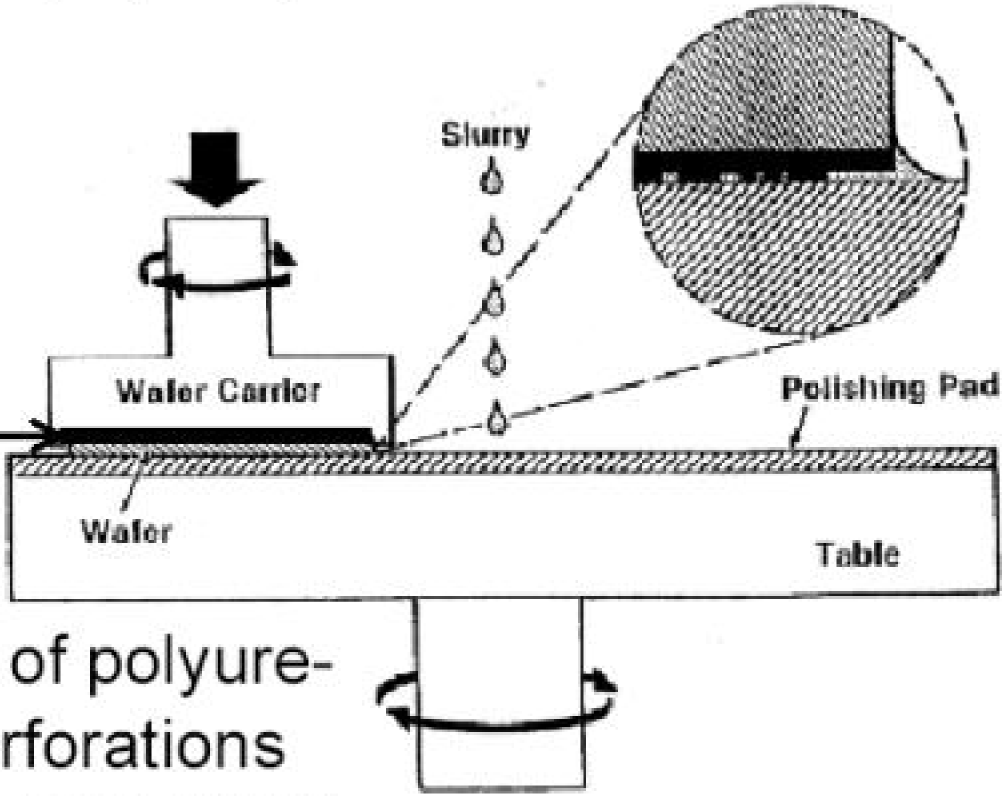
(5)

- Metal chemical-mechanical polish



CMP Tool

- Wafer is polished using a slurry containing
  - silica particles (10-90nm particle size)
  - chemical etchants (*e.g.* HF)



- Backing film provides elasticity between carrier and wafer

- Polishing pad made of polyurethane, with 1 mm perforations
  - rough surface to hold slurry