Lecture #26

ANNOUNCEMENTS

- Basic Tutebot demonstration due by Fri. May 7 in lab section
- Tutebot demonstration contest on Tues., May 11, 9:30-11am, 10 Evans – possible extra credit for strong efforts. Class staff will judge.

OUTLINE

- Interconnect modeling
- Propagation delay with interconnect
- Inter-wire capacitance
- Pi model for capacitive coupling
- Coupling capacitance effects
  - loading
  - crosstalk

Reading (Rabaey et al.)
Chapter 4: Secs. 4.1-4.4.4 ; Chapter 5: pp. 212-213
Interconnects

- An *interconnect* is a thin-film wire that electrically connects 2 or more components in an integrated circuit.

- Interconnects can introduce parasitic (unwanted) components of capacitance, resistance, and inductance. These "**parasitics**" detrimentally affect
  - performance (e.g. propagation delay)
  - power consumption
  - reliability

- As transistors are scaled down in size and the number of metal wiring layers increases, the impact of interconnect parasitics increases.
  → Need to model interconnects, to evaluate their impact
Interconnect Resistance & Capacitance

Metal lines run over thick oxide covering the substrate

→ contribute RESISTANCE & CAPACITANCE to the output node of the driving logic gate
Wire Resistance

\[ R_{wire} = \frac{\rho L}{H W} = R_s \frac{L}{W} \]

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet Res. (Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n, p well diffusion</td>
<td>1000 to 1500</td>
</tr>
<tr>
<td>n+, p+ diffusion</td>
<td>50 to 150</td>
</tr>
<tr>
<td>n+, p+ diffusion with silicide</td>
<td>3 to 5</td>
</tr>
<tr>
<td>polysilicon</td>
<td>150 to 200</td>
</tr>
<tr>
<td>polysilicon with silicide</td>
<td>4 to 5</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 to 0.1</td>
</tr>
</tbody>
</table>

- Silver (Ag): \(1.6 \times 10^{-8}\) Ω-m
- Copper (Cu): \(1.7 \times 10^{-8}\) Ω-m
- Gold (Au): \(2.2 \times 10^{-8}\) Ω-m
- Aluminum (Al): \(2.7 \times 10^{-8}\) Ω-m
- Tungsten (W): \(5.5 \times 10^{-8}\) Ω-m
Interconnect Resistance Example

Typical values of $R_n$ and $R_p$ are $\sim 10 \ \text{k}\Omega$, for $W/L = 1$

... but $R_n$, $R_p$ are much lower for large transistors (used to drive long interconnects with reasonable $t_p$)

Compare with the resistance of a 0.5\(\mu\)m-thick Al wire:

$$R_\square = \rho / H = (2.7 \ \mu\Omega\text{-cm}) / (0.5 \ \mu\text{m}) = 5.4 \times 10^{-2} \ \Omega /$$

Example: $L = 1000 \ \mu\text{m}$, $W = 1 \ \mu\text{m}$

$\rightarrow R_{\text{wire}} = R \ (L / W)$

$$= (5.4 \times 10^{-2} \ \Omega / ) (1000/1) = 54 \ \Omega$$
Wire Capacitance: The Parallel Plate Model

single wire over a substrate:

\[ C_{pp} = \frac{\varepsilon_{di} WL}{t_{di}} \]

Relative Permittivities

<table>
<thead>
<tr>
<th>Material</th>
<th>( \varepsilon_r )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free space</td>
<td>1</td>
</tr>
<tr>
<td>Aerogels</td>
<td>(~1.5)</td>
</tr>
<tr>
<td>Polyimides (organic)</td>
<td>3-4</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>3.9</td>
</tr>
<tr>
<td>Glass-epoxy (PC board)</td>
<td>5</td>
</tr>
<tr>
<td>Silicon Nitride (Si₃N₄)</td>
<td>7.5</td>
</tr>
<tr>
<td>Alumina (package)</td>
<td>9.5</td>
</tr>
<tr>
<td>Silicon</td>
<td>11.7</td>
</tr>
</tbody>
</table>
Parallel-Plate Capacitance Example

- Oxide layer is typically ~500 nm thick
- Interconnect wire width is typically ~0.5 \( \mu \text{m} \) wide (1st level)
  \[ \Rightarrow \text{capacitance per unit length} = 345 \text{ fF/cm} = 34.5 \text{ aF/\( \mu \text{m} \)} \]

Example: \( L = 30 \mu \text{m} \)

\[ \Rightarrow C_{pp} \approx 1 \text{ fF} \] (compare with \( C_n \sim 2 \text{ fF} \))
Fringing-Field Capacitance

For $W / t_{di} < 1.5$, $C_{fringe}$ is dominant

Wire capacitance per unit length:

$$C_{wire} \approx C_{pp} + C_{fringe} = \frac{w \varepsilon_{di}}{t_{di}} + \frac{2 \pi \varepsilon_{di}}{\log(t_{di} / H)}$$

$$w = W - \frac{H}{2}$$
Modeling an Interconnect

Problem: Wire resistance and capacitance to underlying substrate is spread along the length of the wire

"Distributed RC line"

We will start with a simple model...
Lumped RC Model

Model the wire as single capacitor and single resistor:

- $C_{wire}$ is placed at the end of the interconnect
  → adds to the gate capacitance of the load
- $R_{wire}$ is placed at the logic-gate output node
  → adds to the MOSFET equivalent resistance
Cascaded CMOS Inverters w/ Interconnect

Equivalent resistance $R_{dr}$

$V_{in}$

$C_{intrinsic}$

$(r_{wire}, c_{wire}, L)$

$C_{fanout}$

Using “lumped RC” model for interconnect:

$\tau_D = R_{dr} C_{intrinsic} + (R_{dr} + R_{wire})(C_{wire} + C_{fanout})$

$= R_{dr} C_{intrinsic} + (R_{dr} + R_{wire})C_{fanout} + (R_{dr} + R_{wire})C_{wire}$
Effect of Interconnect Scaling

\[ R_{\text{wire}} C_{\text{wire}} = \left[ \rho \frac{L}{WH} \right] \left[ \frac{\varepsilon_{\text{di}}}{t_{\text{di}}} (WL) + \frac{2\pi \varepsilon_{\text{di}} L}{\log(t_{\text{di}}/H)} \right] \propto \rho \varepsilon_{\text{di}} L^2 \]

- Interconnect delay scales as square of \( L \)
  \[ \Rightarrow \] minimize interconnect length!

- If \( W \) is large, then it does not appear in \( R_{\text{wire}} C_{\text{wire}} \)
  - Capacitance due to fringing fields becomes more significant as \( W \) is reduced; \( C_{\text{wire}} \) doesn’t actually scale with \( W \) for small \( W \)
Propagation Delay with Interconnect

Using the lumped-RC interconnect model:

\[ t_p = 0.69 \tau_d \]

\[ = 0.69 R_{dr} C_{\text{intrinsic}} + 0.69(R_{dr} + R_{wire})C_{\text{fanout}} \]

\[ + 0.69(R_{dr} + R_{wire})C_{wire} \]

In reality, the interconnect resistance & capacitance are distributed along the length of the interconnect.

→ The interconnect delay is actually less than \( R_{wire}C_{wire} \):

\[ t_p = 0.69 R_{dr} C_{\text{intrinsic}} + 0.69(R_{dr} + R_{wire})C_{\text{fanout}} \]

\[ + (0.69 R_{dr} + 0.38 R_{wire})C_{wire} \]

The 0.38 factor accounts for the fact that the wire resistance and capacitance are distributed.
Interconnect Wire-to-Wire Capacitance

Wire A simply has capacitance \((C_{pp} + C_{fringe})\) to substrate.

Wire B has additional sidewall capacitance to neighboring wires.

Wire C has additional capacitance to the wire above it.
Wiring Examples - Intel Processes

Advanced processes: narrow linewidths, taller wires, close spacing → relatively large inter-wire capacitances

Intel 0.25µm Process (Al)
5 Layers - Tungsten Vias
Source: Intel Technical Journal 3Q98

Intel 0.13µm Process (Cu)
Source: Intel Technical Journal 2Q02
Effects of Inter-Wire Capacitance

- Capacitance between closely spaced lines leads to two major effects:
  1. Increased capacitive loading on driven nodes (speed loss)
  2. Unwanted transfer of signals from one place to another through capacitive coupling "crosstalk"

- We will use a very simple model to estimate the magnitude of these effects. In real circuit designs, very careful analysis is necessary.
Pi Model for Capacitive Coupling

There are three capacitances as illustrated:

- Wire 1 has resistance $R_1$
- Wire 2 has resistance $R_2$

Using a simple lumped model for each wire we have three capacitances and two resistances:

Which, when redrawn in a plane, has a "π" shape.
Coupling Capacitance: Loading Effect

A) Coupling to grounded adjacent line

B) Coupling to floating adjacent line

C) Coupling to driven adjacent line

Case C is well-approximated to be the same as case A
Case A: Coupling to Grounded Line

Insert the Pi model:

\[ \tau_D = R_{dr1} C_{out1} + \left( R_1 + R_{dr1} \right) \left( C_1 + C_C + C_{in2} \right) \]

- \( C_1 \) and \( C_C \) are in parallel with the input capacitance of inverter 2, \( C_{in2} \).
- This combined \( C \) is driven by the output resistance of inverter 1 in series with the line resistance \( R_1 \).
Case B: Coupling to Floating Line

Insert the Pi model:

$C_1$ is in parallel with the series combination of $C_C$ and $C_2$. This combined $C$ is driven by the output resistance of inverter 1 in series with the line resistance $R_1$.

$$\tau_D = R_{dr1}C_{out1} + (R_1 + R_{dr1}) \left( C_1 + \frac{C_2C_C}{C_2 + C_C} + C_{in2} \right)$$
Coupling Capacitance: Crosstalk

Wire 1

Signal from (1) couples to adjacent line

Wire 2

Insert Pi model:

1

R1

R2

C1

C2

CC

2

3

4

Note that (4) receives both from (3) and from (1). The latter is undesired crosstalk.

Similarly, (2) receives signal both from (1) and from (3).

Let's assume (3) is quiet, and (1) is broadcasting...
We want to estimate the magnitude of the crosstalk signal at the input to (4).

We cannot easily treat this problem exactly (yet), but we can see that:

1. The crosstalk signal is attenuated by the capacitive voltage divider \( C_C \) in series with \( (C_2 \parallel C_{in4}) \).

2. If \( C_C \) is very large, about half the signal from (1) is coupled into (4) because of the voltage divider \( R_1 + R_{dr1} \) in series with \( R_2 + R_{dr3} \) where \( V_{in4} \) is tapped off at the center.
Approaches to Reducing Crosstalk

1. Increase inter-wire spacing (decrease $C_C$)
2. Decrease field-oxide thickness (decrease $C_C/C_2$)
   …but this loads the driven nodes and thus decreases circuit speed.
3. Place ground lines (or $V_{DD}$ lines) between signal lines

[Diagram of ground lines and silicon substrate]