Homework #10
Solutions

Due at 6 pm in 240 Cory on Wednesday, 04/18/07
Total Points: 100
• Put (1) your name and (2) discussion section number on your homework.
• You need to put down all the derivation steps to obtain full credits of the problems. Numerical answers alone will at best receive low percentage partial credits.
• No late submission will be accepted except those with prior approval from Prof. Chang-Hasnain.

1. Hambley, P10.46

(a) The integral of $V_m = \sin(\omega t)$ over one cycle is zero, so the dc voltmeter reads zero. [2pts]

(b) $V_{avg} = \frac{1}{T} \left[ \int_0^{T/2} V_m \sin(\omega t) dt + \int_{T/2}^T 0 dt \right] = \frac{1}{T} \left[ -\frac{V_m}{\omega} \cos(\omega t) \right]_{t=0}^{t=T/2} = \frac{V_m}{\pi}$ [4pts]

(c) $V_{avg} = \frac{1}{T} \left[ \int_0^{T/2} V_m \sin(\omega t) dt + \int_{T/2}^T -V_m \sin(\omega t) dt \right] = \frac{2V_m}{\pi}$ [4pts]

2. Hambley, P10.48

As in Problem P10.47, the peak voltage must be 10 V. For a full-wave rectifier, the capacitance is given by Equation (10.12) in the text:

$C = \frac{I_L T}{2V_r} = \frac{0.1(1/60)}{2(2)} = 417 \mu F$ [4pts]

The circuit diagram is: [6pts]
3. Hambley, P10.52

(a) The current pulse starts and ends at the times for which \[ v_s(t) = V_B \]
\[ 20\sin(200\pi t) = 12 \]

Solving we find that \[ t_{\text{start}} = \frac{\sin^{-1}(0.6)}{200\pi} = 1.024\text{ms} \text{ and } t_{\text{end}} = \frac{T}{2} - t_{\text{start}} = 3.976\text{ms} \]

Between these two times the current is
\[ i(t) = \frac{20\sin(200\pi t) - 12}{80} \]

A sketch of the current to scale versus time is
(b) The charge following through the battery in one period is [5pts]

\[ Q = \int_{t_{\text{start}}}^{t_{\text{end}}} i(t) dt = \int_{t_{\text{start}}}^{t_{\text{end}}} \frac{20 \sin(200\pi t) - 12}{80} dt \]

\[ = \left[ -\frac{1}{800\pi} \cos(200\pi t) - \frac{12t}{80} \right]_{t_{\text{start}}}^{t_{\text{end}}} \]

Finally, the average current is the charge divided by the period

\[ I_{\text{avg}} = \frac{Q}{T} = \frac{194 \times 10^{-6}}{10 \times 10^{-9}} = 19.4 \text{mA} \]

4. Hambley, P10.55 [10pts]

Refer to Figure P10.55 in the book. When the source voltage is negative, diode D₃ is on and the output \( v_o(t) \) is zero. For source voltage between 0 and 10 V, none of the diodes conducts and \( v_o(t) = v_s(t) \). Finally when the source voltage exceeds 10 V, D₁ is on and D₂ is in the breakdown region so the output voltage is 10 V. The waveform is:
5. Hambley, P10.57 [10pts]
6. Hambley, P10.60 (EE40 Only) [10pts]

Refer to the circuit shown in Figure P10.60 in the book. If the output voltage attempts to become less than -5 V, the Zener diode breaks down and current flows, charging the capacitance. Thus the negative peak is clamped to -5 V. The input and output waveforms are:

![Waveform Diagram]

6. Hambley, P10.62 [EE100 Only] [10pts]

A suitable circuit is:

![Circuit Diagram]
7. Consider the following circuit: 

Use the 0.7 model for all the diodes, and let \( R_2 = 2R_1 \).

Sketch the voltage transfer characteristic \( (v_o \text{ vs } v_{in}) \).

The input voltage is between -3V and +3V.

Using the voltage divider formula, the voltage across R1 is \( \frac{1}{3}v_{in} \). Therefore, if the voltage across R1 is between -0.7 and 1.4, all the diodes are “off”. Notice that D3 has a reverse polarity than D1 and D2. This means that if \(-2.1 < v_{in} < 4.2\), then all the diodes are off. Given the max \( v_{in} = +3 \), D1 and D2 are always off. As a result, \( v_o = \frac{2}{3}v_{in} \) or \(-1.4 < v_o < 2\).

If \(-2.1 > v_{in} > -3\), then the voltage across D3 is greater than 0.7 and the diode turns on. As a result, all the current goes through the diode (since it’s short) and the voltage across D3 is 0.7 Volt, \(-2.3 < v_o < -1.4\).
Diode Logic: In this problem, we will compare 2 implementations in diode logic of the same logic function.

(a) The logic function performed is the AND of the inputs A, B, C. [2pts]
b) In Figure (a), when all the inputs are low, D1 is off and the other diodes are on so $V_{out} = 0.7V$. In figure (b), all the diodes will be on, so $V_{out} = 0.7$.[3pts]

c) The power dissipated in circuit (a) is: $P_1 = (3-0.7)^2/100k$ and $P_2 = (3-1.4)^2/100k$ and total power is $P = P_1 + P_2 = 7.85 \times 10^5$ Watt. The power dissipation in circuit (b) is; $P = 5.29 \times 10^5$ Watt [3pts]

d) For the circuit in Figure (b), when inputs A and B are low and C is high, D1 and D2 are on and D3 is off, so the output $F$ is 0.7 since the diodes that are on and carry a 0.7V across them. However, in Figure (a), when the inputs A and B are all low and C is high, D1, D2, and D3 are on and D4 is off. Therefore, the output $F$ is 1.4, which is very close to being logic high and could result in an error. [2pts]

9. Hambley, P10.64 [EE 100 Only]

(a) A suitable circuit is: [5pts]

We choose the resistors $R_1$ and $R_2$ to achieve the desired slope.
\[ \text{Slope} = \frac{1}{3} = \frac{R_2}{R_1 + R_3} \]

Thus, choose \( R_1 = 2R_2 \). For example, \( R_1 = 2 \, \text{k}\Omega \) and \( R_2 = 1 \, \text{k}\Omega \)

(b) A suitable circuit is: \( \textbf{[5pts]} \)

Other resistor values will work, but we must make sure that \( D_2 \) remains forward biased for all values of \( v_{in} \), including \( v_{in} = -10 \text{V} \). To achieve the desired slope (i.e., the slope is 0.5) for the transfer characteristic, we must have \( R_1 = R_2 \).

10. \textbf{Diode + Op-Amp}: Consider the following circuit: \( \text{[EE40 Only]} \)

Use the 0.7V model for the diode.
a) When the diode is on, the voltage across it is 0.7V. Using the Summing point constraint, the voltage at the inverting input of the op-amp is 2. Now we use KCL at the inverting input node: \( \frac{2 - (Vin - 0.7)}{5k\Omega} = 20\mu F \cdot \frac{d(Vc)}{dt} \) where \( Vc = 2 - Vout(t) \). Substituting \( Vc \) in the KCL equation and integrating gives \( Vout \) in terms of \( Vin \).

\[
\frac{1}{RC} \int_{t_1}^{t_2} (-v_{in} + 2.7)dt
\]

b) When the diode is off, there is not current in the resistor. Therefore, \( Vc \) is constant and \( Vout \) is also constant. [2pts]
c) When the diode is on, the voltage across it has to be greater than 0.7 (with the correct polarity applied). Given the voltage at the inverting input of the op-amp is 2V (Summing point constraint), the input voltage \( Vin \) has to be greater than 2.7V in order for the diode to turn on. [2pts]
d) The periods is \( T = 1/50 = 0.02 \) sec. \( Vin \) is a triangle wave with a peak-to-peak value of 20 V, so the height of the triangle is \( Vpp/2 = 10 \) V. In order to find the output voltage \( Vout \), we have to integrate the input wave between \( t_1 = 0 \) and \( t_2 = 0.06 \) sec. Given the period is 0.02, we can integrate the input wave over one period and multiply the results by 3. \( Vout = 3 \times 0.1 = 0.3 \) V [3pts]

10. Doping [10pts]

a) The majority carrier for Silicon doped with Phosphorus is electron, and the resulting material is n-type. Concentration of holes=\( 10^{15} \) and concentration of electrons is \( 10^{20}/10^{15} \) [3pts]
b) The majority carrier for Silicon doped with Arsenic and Boron is holes, and the resulting material is p-type since the concentration of Boron is more than Arsenic. Concentration of holes=\( 5 \times 10^{16} \) and concentration of electrons=\( 10^{20}/5 \times 10^{16} \) [3pts]
c) The majority carrier for Silicon doped with all three is electron, and the resulting material is n-type. Concentration of electrons=\( 10^{15} \) and concentration of holes is \( 10^{20}/10^{15} \) [4pts]