

EE43/EE100 — LAB REPORT #9
Digital Logic

Name: _____

TA: _____

Section: _____

Step 1: Draw the layout of the 4-inverter chain using the Quad NAND IC. Show the actual physical layout of the circuit – “top view” – on the breadboard. Also show the internal wiring of the breadboard.

Step 4: Measure the propagation delays through 1, 2, 3, and 4 gates for $V_{dd} = 5V$ and $2V$.

$V_{dd} = 5V$	1 gate	2 gates	3 gates	4 gates
t_{pHL}, Output				
t_{pLH}, Output				
Average t_{pavg}				

$V_{dd} = 2V$	1 gate	2 gates	3 gates	4 gates
t_{pHL}, Output				
t_{pLH}, Output				
Average t_{pavg}				

Step 5:

Average gate delay = _____ at $V_{dd} = 5V$

Average gate delay = _____ at $V_{dd} = 2V$

Step 6: Draw the layout of an XOR circuit using two 74HC00 packages and your breadboard. Show all wires including the “hidden” wires in the breadboard.

Step 7: Verify static operation of the XOR circuit:

Verify $V_{dd} = 5V$ static logic			Verify $V_{dd} = 2V$ static logic		
A	B	Output	A	B	Output
0	0		0	0	
0	1		0	1	
1	0		1	0	
1	1		1	1	

TA initials: _____

Step 9: Measure propagation delays for the XOR circuit:

Set $V_{dd} = 5V$, wire B = 0, then measure delay:

from A(0 to 1) to Output: _____

from A(1 to 0) to Output: _____

Now wire A = 1, then measure delay:

from B(0 to 1) to Output: _____

from B(1 to 0) to Output: _____

Set $V_{dd} = 2V$, wire B = 0, measure delay:

from A(0 to 1) to Output: _____

from A(1 to 0) to Output: _____

Now wire A = 1, then measure delay:

from B(0 to 1) to Output: _____

from B(1 to 0) to Output: _____

Optional:

Logic probe functionality (TA initials): _____