EE 40: Introduction to Microelectronic Circuits
Spring 2008: HW 7
(due 4/11, 5 pm)

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Referenced problems from Hambley, 4th edition.

1. P14.11

First check for negative feedback: If $v_o \uparrow$, then $v_2 \uparrow$, hence $v_1 - v_2 \downarrow$, hence $v_o \downarrow$.

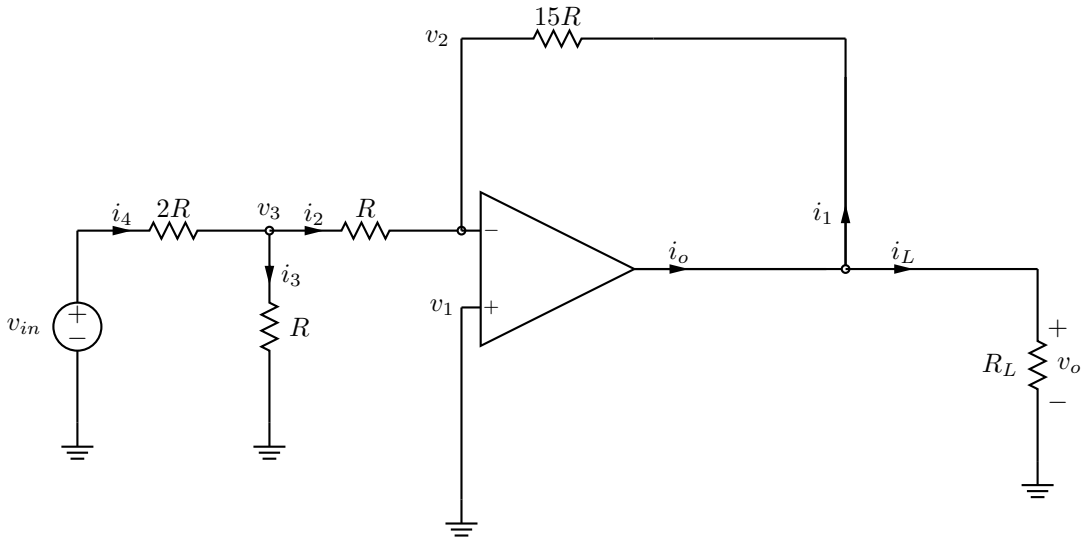

Figure 1: Circuit Analyzed in P14.11

Next, using the summing point constraint and $v_1 = 0$, we get $v_2 = 0$. Since

$$v_3 = v_2 + i_2 R = i_2 R$$

and

$$v_3 = i_3 R$$

we get $i_2 = i_3$. Hence,

$$i_4 = i_2 + i_3 = 2i_2$$

We also have

$$v_{in} = i_4(2R) + i_3 R = (2i_2)(2R) + i_2 R = 5i_2 R$$

Hence

$$i_2 = \frac{v_{in}}{5R}$$

and

$$v_3 = \frac{v_{in}}{5}$$

We have $i_1 + i_2 = 0$, because no current is drawn at the op-amp's $-$ input.
Hence,

$$\begin{aligned} v_o &= v_2 + (15R)i_1 \\ &= -(15R)i_2 \\ &= -3v_{in} \end{aligned}$$

This establishes that the closed loop voltage gain is -3.
To complete the analysis of the circuit, not that

$$i_L = \frac{v_o}{R_L} = \frac{-3v_{in}}{R_L}$$

and

$$\begin{aligned} i_o &= i_1 + i_L \\ &= -i_2 + i_L \\ &= -\frac{v_{in}}{5R} - \frac{v_{in}}{R_L} \end{aligned}$$

2. P14.16
First we check for negative feedback: $v_L \uparrow \rightarrow v_2 \uparrow \rightarrow v_1 - v_2 \downarrow \rightarrow v_L \downarrow$.
We have the circuit in Figure 2. Using the summing point constraint gives

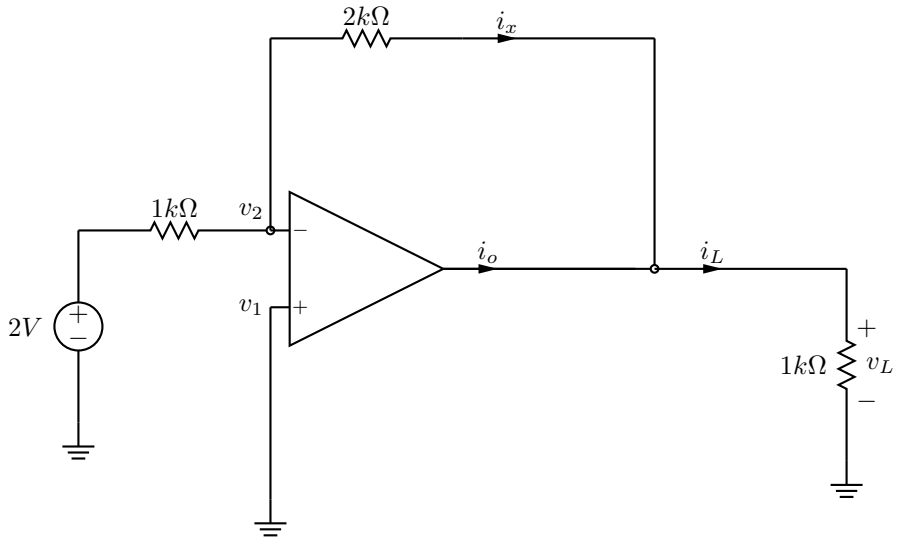

Figure 2: Circuit of P14.16

$$v_2 = v_1 = 0$$

The second equation is because the '+' input of the op-amp is connected to ground. This gives

$$2 = i_x 10^3$$

Hence,

$$i_x = 2 * 10^{-3} A$$

Also,

$$v_L = -i_x 2k\Omega = -4V$$

We also have

$$i_L = \frac{v_L}{1k\Omega} = -4mA$$

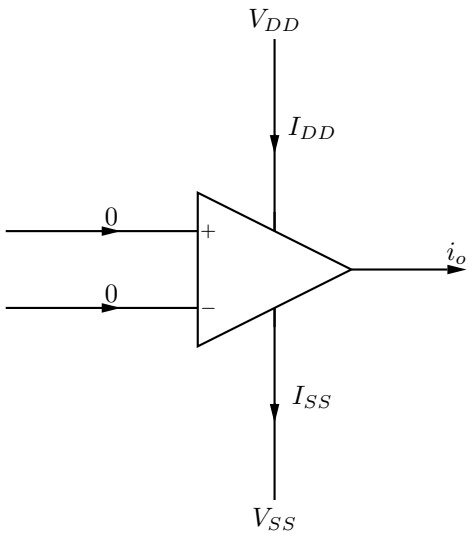

Figure 3: KCL for Op-Amp

and

$$i_o = i_L - i_x = -6mA$$

The currents into the "closed surface" are displayed in Figure 3.

Note that there are currents from the power supply connections, as shown. This is why KCL continues to hold.

$$0 + 0 + I_{DD} - I_{SS} - i_o = 0$$

In most of the examples we are considering, however, neither I_{DD} nor I_{SS} are known.

3. P14.23

   (a) First, check for negative feedback. This is subtle, because we have to check for the effects of perturbations in both op-amps outputs. The way to handle this is to observe first that any perturbation in the output of the bottom op-amp is stabilized by the negative feedback around it. Hence we can think of the $-$ input of the bottom op-amps as being tied to v_2 when considering perturbations of the output of the top op-amp and now conclude that such perturbations are also stabilized because of the negative feedback around the top op-amp.

   The summing point constraint at the op-amp A gives

   $$v_{2A} = v_{1A} = v_1$$

   Thus

   $$v_{oA} = i_o R_L + v_{2A} = i_o R_L + v_1$$

   The summing point constraint at the op-amp B gives

   $$v_{2B} = v_{1B} = v_2$$

   Since $i_o = i_1$, we have

   $$\begin{aligned} v_1 = v_{2A} &= v_{2B} + i_1 R \\ &= v_{2B} + i_o R \\ &= v_2 + i_o R \end{aligned}$$

   Hence, we have

   $$i_o = \frac{v_1 - v_2}{R}$$

   Finally

   $$v_{oB} = v_{2B} = v_2$$

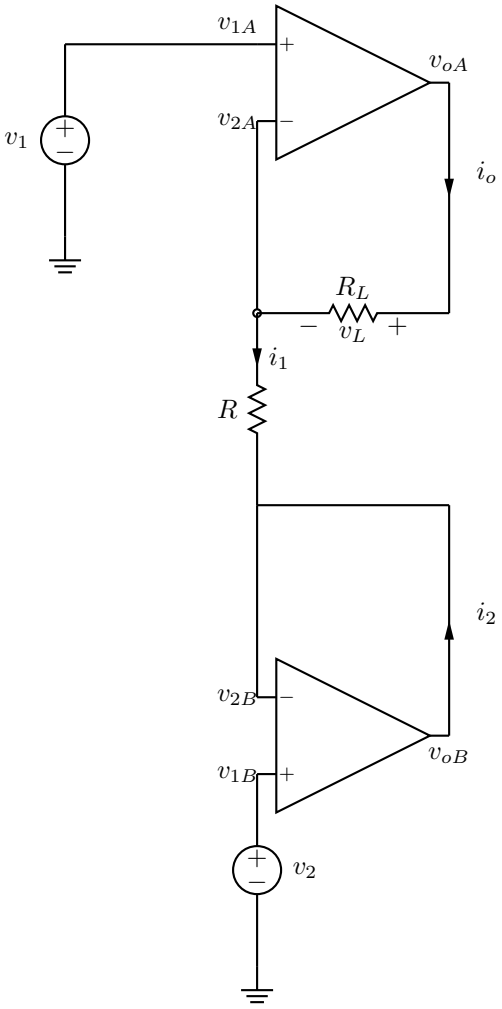

Figure 4: Circuit Analyzed in P14.23 (a)

and

$$i_2 = -i_1$$

Solving the circuit, we note that the current delivered to the load is

$$i_L = \frac{v_1 - v_2}{R}$$

irrespective of the value of the load, R_L. Thus, across its terminals, the load sees the circuit (i.e. the portion of the circuit ofther than the load) as an ideal current source delivering this current (see Figure 5).

For that reason, the output impedance is ∞.

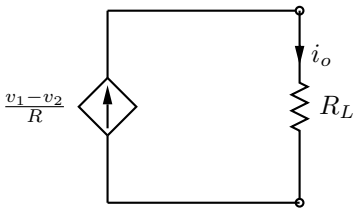

Figure 5: Ideal Current Source

In particular, there is no Thévenin equivalent circuit from the point of view of the load and the

circuit makes no sense when the load is replace by an open circuit. This is a constrast to several of the other circuits we studied, which make no sense when the load is replaced by a short circuit.

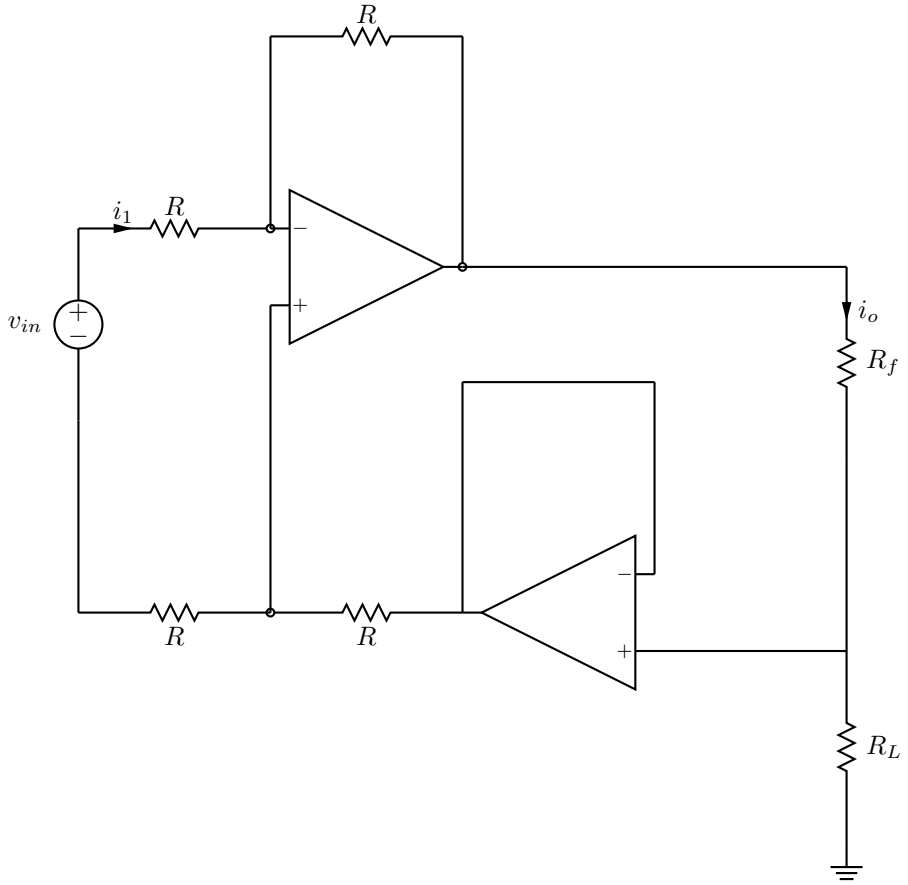

Figure 6: Circuit Analyzed in P14.23 (b)

(b) Upfront, we recognize that we have negative feedback at both op-amps. The op-amp on the bottom is a unity gain circuit and the upper op-amp is in a configuration where a perturbation of the output has a stronger impact on the negative input as on the positive input.
We first consider the loop containing the voltage source, the two adjacent resistors and the upper op-amp. As, by the summing point constraint, the voltage between the two input terminals of the op-amp is zero, we get for i_1

$$i_1 = \frac{v_{in}}{2R} \tag{1}$$

Secondly, we consider the loop containing the input terminals of the upper op-amp, the resistor between the input of the upper op-amp and its output, R_f, the unity gain buffer, and the resistor at its output. We obtain the KVL equation

$$2i_1R + i_oR_f = 0 \tag{2}$$

where we used that there are no currents flowing into the inputs of the op-amps and that the voltages of input and output of the unity gain buffer are equal.
We combine (1) and (2) to get the desired result for the output current.

$$i_o = -\frac{v_{in}}{R_f}$$

For the output resistance, we consider a circuit where the independent voltage source at the input is zeroed and R_L is replaced by a test voltage source with voltage v_t (not depicted).
By our analysis, we know that the test current drawn from the test voltage source is

$$i_t = -i_o = \frac{v_{in}}{R_f} = \frac{0}{R_f} = 0$$

We get R_{out} by the formula

$$R_{out} = \frac{v_t}{i_t} \to \infty$$

Therefore, as in (a), the output resistance is infinite.

4. P14.34

To check for negative feedback, we first observe that a perturbation at the output of the left op-amp is stabilized because it results in negative feedback through the path leading through the right op-amp (which dominates because of the gain of the right op-amp). Thus, we can thinkg of the '+' input of the right op-amp as being fixed. Now, perturbations of the output of the right op-amp are only fed back through the '-' input of the right op-amp (since the '+' input of that op-amp of that op-amp may be considered fixed) so they are also stabilized.

We proceed to solve the circuit in Figure 7. We have

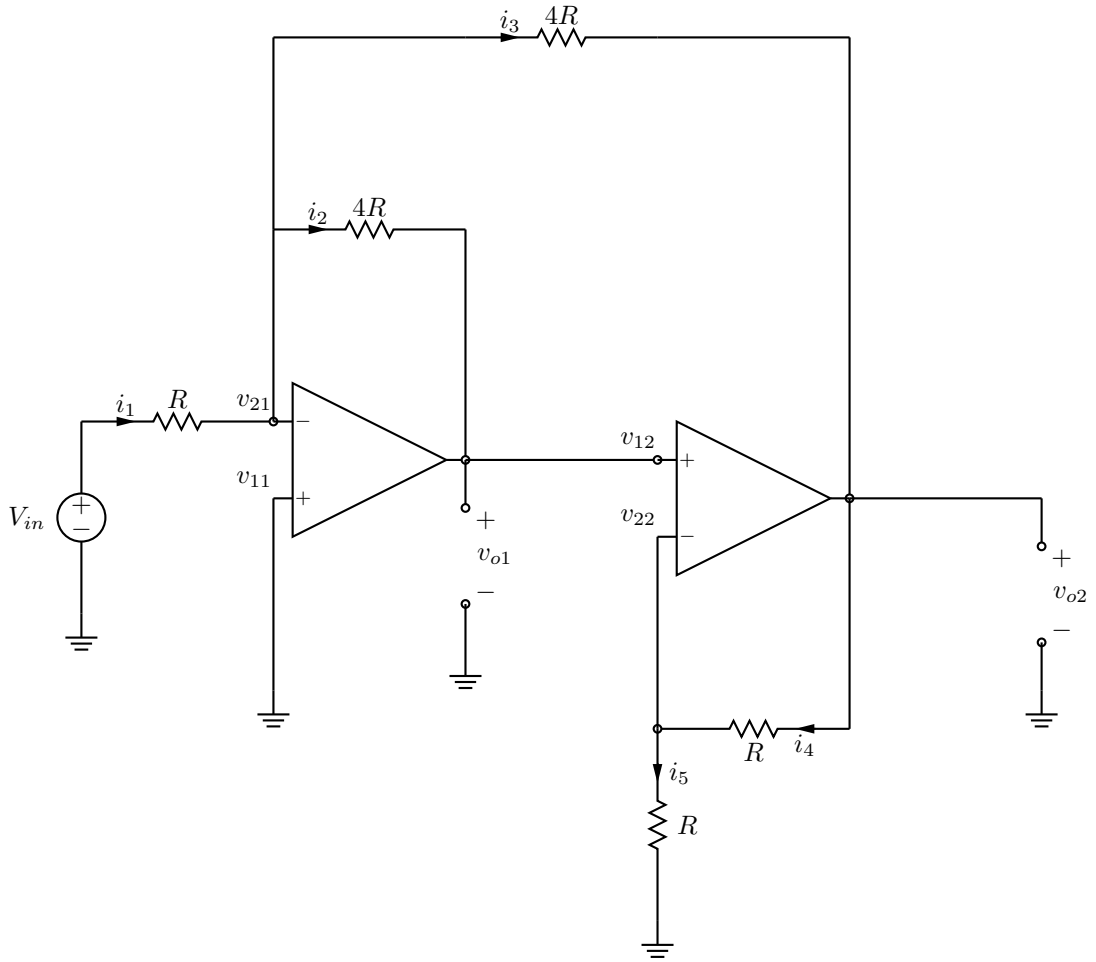

Figure 7: Circuit P14.34

$$v_{21} = v_{11} = 0$$

by the summing point constraint at op-amp 1. We also have

$$i_1 = \frac{v_{in}}{R}$$

For the other op-amp, we know that

$$v_{12} = v_{22}$$

and also

$$i_5 = i_4 = \frac{v_{22}}{R}$$

Hence

$$v_{o2} = 2v_{22}$$

and

$$i_3 = -\frac{v_{o2}}{4R} = -\frac{v_{22}}{2R}$$
$$i_2 = -\frac{v_{12}}{4R} = -\frac{v_{22}}{2R}$$

Using KCL, we have

$$i_1 = i_2 + i_3 = -\frac{3v_{22}}{4R}$$

Hence,

$$v_{in} = -\frac{3v_{22}}{4}$$

Hence,

$$v_{o1} = v_{12} = v_{22} = -\frac{4}{3}v_{in}$$
$$v_{o2} = v_{12} = 2v_{22} = -\frac{8}{3}v_{in}$$

Thus, $A_1 = -\frac{4}{3}$ and $A_2 = -\frac{8}{3}$.

5. P14.47

   (a) From KVL, we have

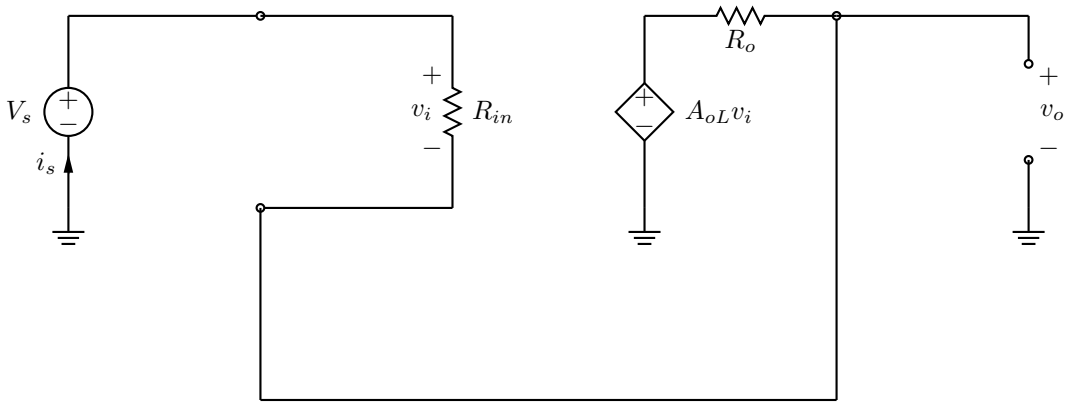

Figure 8: Circuit P14.47

$$v_s = i_s R_{in} + v_o$$

and

$$i_s R_o + A_{oL} v_{in} = v_o$$

Also,

$$v_i = i_s R_{in}$$

Substituting, we get

$$\begin{aligned} v_o &= i_s(R_o + A_{oL}R_{in}) \\ &= \frac{v_s - v_o}{R_{in}}(R_o + A_{oL}R_{in}) \end{aligned} \tag{3}$$

Hence,

$$\frac{v_o}{v_s} = \frac{R_o + A_{oL}R_{in}}{R_o + (A_{oL}+1)R_{in}}$$

For the given parameter values, we get

$$\frac{v_o}{v_s} = \frac{25 + 10^{11}}{25 + 10^6 + 10^{11}} = 0.99999$$

which is very close to 1 which is the result we get assuming an ideal op-amp.

(b) The input impedance is found by leaving the output terminals unloaded and considering the ratio of the input voltage to the input current. The circuit drawn is already unloaded at the output so the input impedance is

$$Z_{in} = \frac{v_s}{i_s} = R_o + (A_{OL} + 1)R_{in} = 25 + 10^6 + 10^1 1\Omega$$

The ideal op-amp has infinite input impedance.

(c) The output impedance is found by shorting the input terminals (setting the input voltage to zero) and applying a test circuit to the output terminals and determining the current drawn by the given circuit at the output. Redrawing the circuit for this scenario gives the circuit in Figure 9. Here, v_t is a test voltage and R_t a test resistance. We have

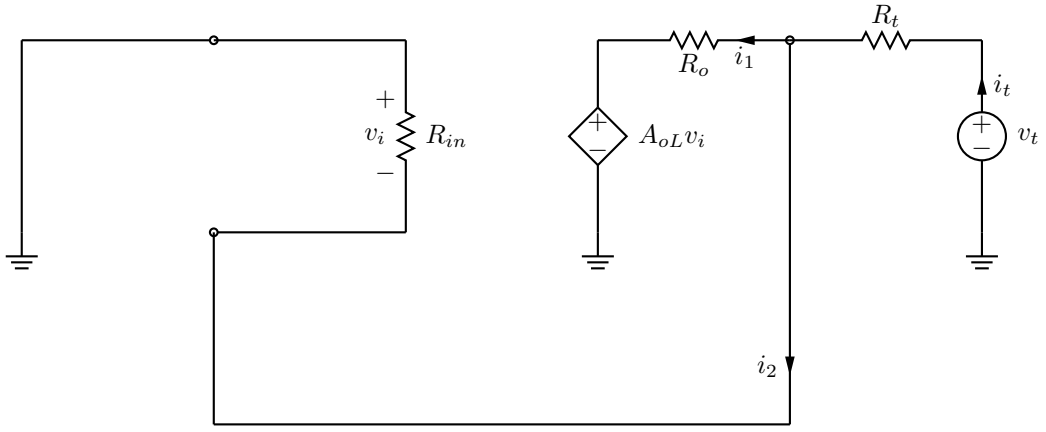

Figure 9: Calculating the Output Resistance

$$v_i = -i_2 R_i n$$

and

$$A_{OL}v_i + i_1 R_o = i_2 R_{in}$$

which gives

$$i_1 = \frac{R_{in}}{R_o}(1 + A_{OL})i_2$$

Hence,

$$i_t = i_1 + i_2 = \frac{R_{in}}{R_o}(1 + A_{OL}) + 1)i_2$$

Also

$$v_t = i_t R_t + i_2 R_{in} = i_t(R_t + \frac{R_{in}}{1 + \frac{R_{in}}{R_o}(1 + A_{OL})})$$

The output impedance is seen to equal

$$Z_o = \frac{R_o R_{in}}{R_o + R_{in}(1 + A_{OL})}$$

For an ideal op-amp, this would give zero as the open loop amplification is infinite.

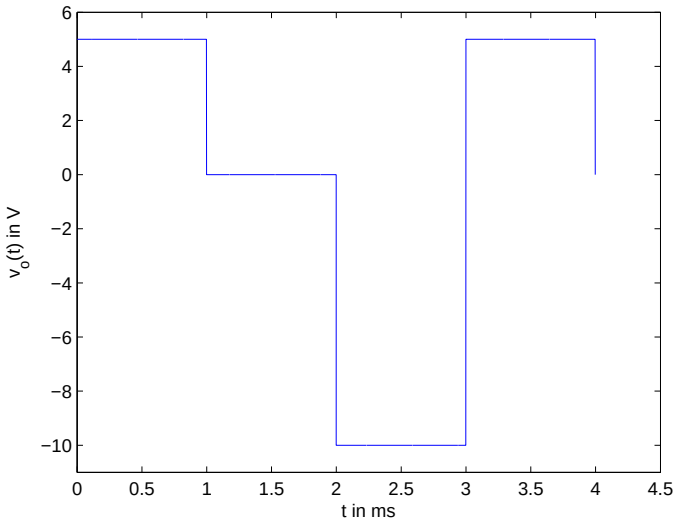

Figure 10: Output Voltage for Problem P14.75

6. P14.75 We know that this circuit functions as a differentiator and that

$$\begin{aligned} v_o(t) &= -RC\frac{dv_{in}}{dt}(t) \\ &= -10^{-3}\frac{dv_{in}}{dt}(t) \end{aligned}$$

For the given input voltage, we obtain the output signal as given in Figure 10

7. P14.78 part (b) only
We first observe that negative feedback is present in the circuit.
Next, we analyze the circuit using phasor analysis at frequency ω. Redrawing the circuit, we have the circuit in Figure 11.
We have $\mathbf{V}_1 = 0$ and, using the summing point constraint, we get

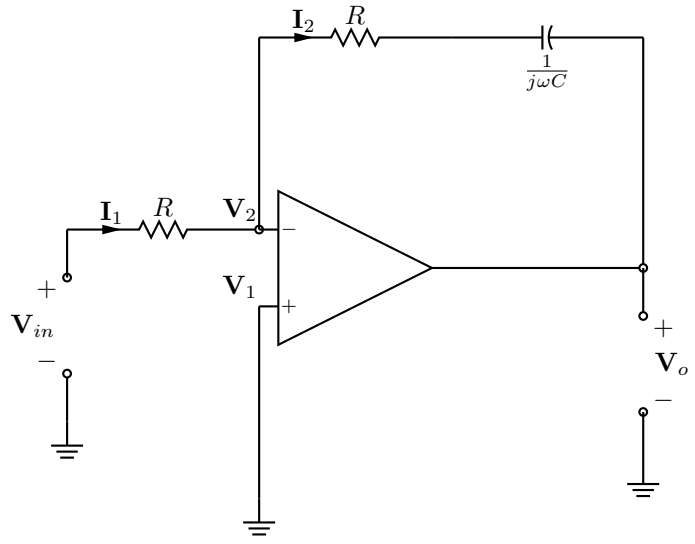

Figure 11: Circuit P14.78 (b)

$$\mathbf{V}_1 = \mathbf{V}_2 = 0$$

This gives

$$\mathbf{I}_1 = \frac{\mathbf{V}_{in} - \mathbf{V}_2}{R} = \frac{\mathbf{V}_{in}}{R}$$

and, since the inputs of the op-amp draw no current, we have

$$\mathbf{I}_1 = \mathbf{I}_2$$

from which we get

$$\begin{aligned} \mathbf{V}_o &= -\mathbf{I}\left(R + \frac{1}{j\omega C}\right) \\ &= -\mathbf{V}_{in}\left(1 + \frac{1}{j\omega RC}\right) \end{aligned} \tag{4}$$

The "voltage transfer ratio" (i.e. the transfer function) is

$$H(\omega) = -\frac{1 + j\omega RC}{j\omega RC}$$

The Body magnitude plot is the plot of $20\log_{10}|H(\omega)|$ against $\log_{10}\omega$. As $\omega \to 0$ we have $20\log_{10}|H(\omega)| \to 20\log_{10}\omega - 20\log_{10}RC$.
As $\omega \to \infty$ we have $|H(\omega)| \to 1$ and so $20\log_{10}|H(\omega)| \to 0$.
As $\omega \to 0$ we have $\angle H(\omega) \to 90\,\text{deg}$.
As we have $\omega \to \infty$ we have $\angle H(\omega) \to 0\,\text{deg}$.
The Bode plot is given in Figure 12. Not that the plot is normalized. $\omega_b = \frac{1}{RC}$.

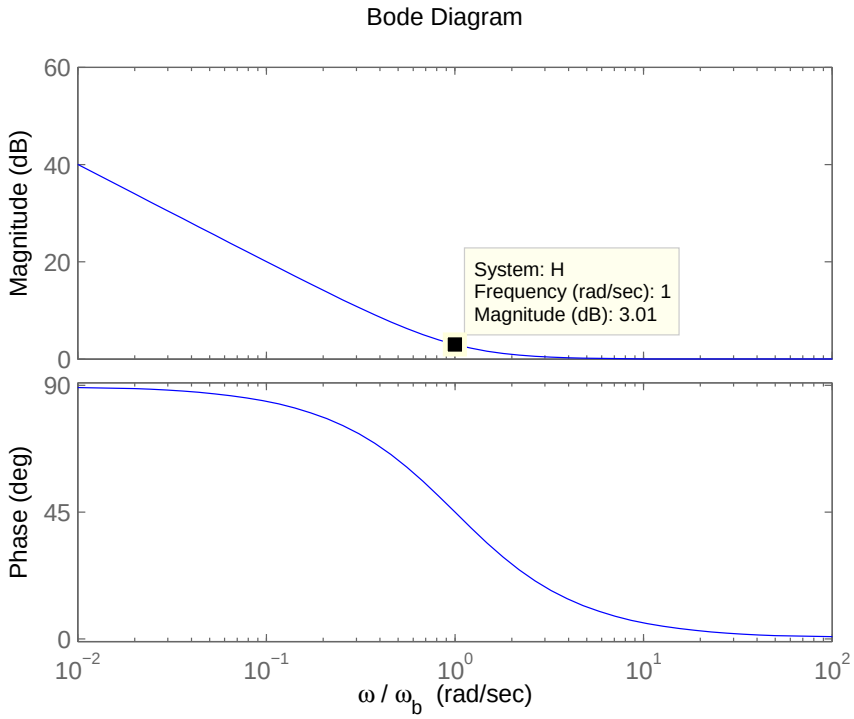

Figure 12: The Bode Plot of P14.78b

8. (a) P10.21 We have

$$10 = 2.5i + v$$

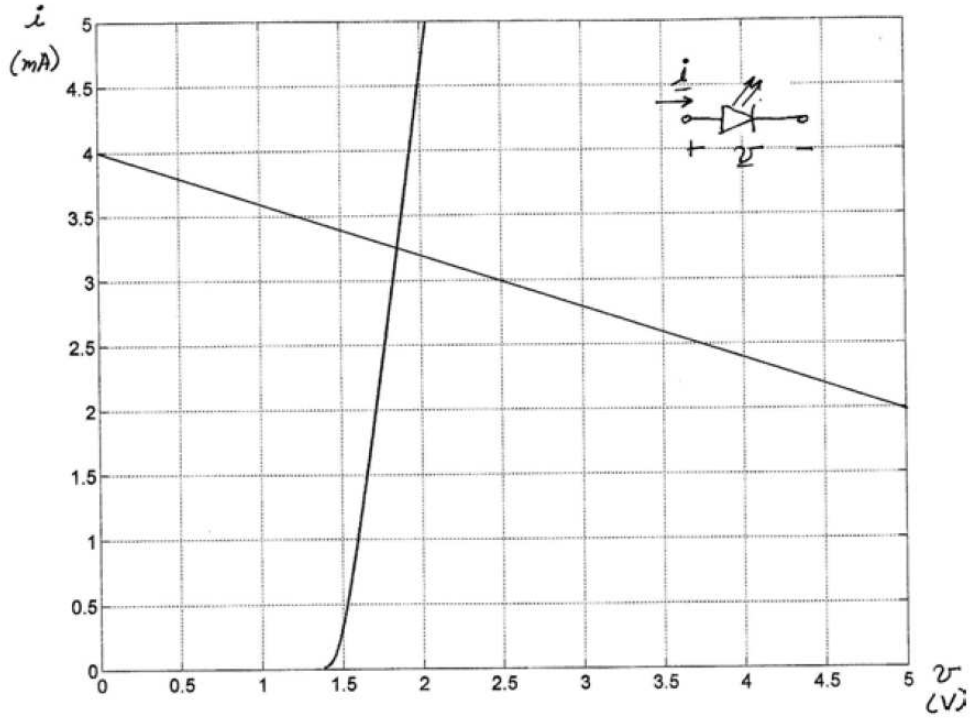

Figure 13: Load Line (a) in given I-V Characteristic

where v is measured in V and i is measured in mA. Drawing the load line on the indicated I-V characteristic of the diode gives the solution as given in Figure 13

The intersection of the two lines is the solution, we have approximately

$$v \approx 1.85V \qquad\qquad i \approx 3.25mA$$

(b) P10.23 We have

$$i = \frac{i_x}{2}$$

and

$$5 = i_x + v$$

So

$$5 = 2i + v$$

where v is measure in V and i is measured in mA. Drawing the load line on the given I-V characteristic of the diode (see Figure 14) gives the approximative solutions

$$v \approx 1.7V \qquad\qquad i \approx 1.7mA$$

9. P10.38 part (a) only

If $v_2 < 0$ then diode D_2 becomes on, shorting v_2 to ground, which forces $v_2 = 0$. Thus $v_2 \geq 0$. Similar logic tells us that $v_1 \leq 0$ and $v_3 \leq 0$.

If $v_2 > 0$ then diode D_2 is off. Further, since $v_1 \leq 0$ and $v_3 \leq 0$ this would mean that positive current flows from node 1 to node 2 and positive current flows from node 1 to node 3, which contradicts KCL. Hence $v_2 = 0$.

If $v_1 < 0$ then D_1 is off. Thus positive current flows from the $+15V$ end to node 1 and positive current flows from node 2 to node 1 (because $v_2 = 0$). This contradicts KCL at node 1. Hence $v_1 = 0$.

So we get the solution of the circuit as depicted in Figure 16. We have

$$v = 7.5V \qquad\qquad I = 0mA$$

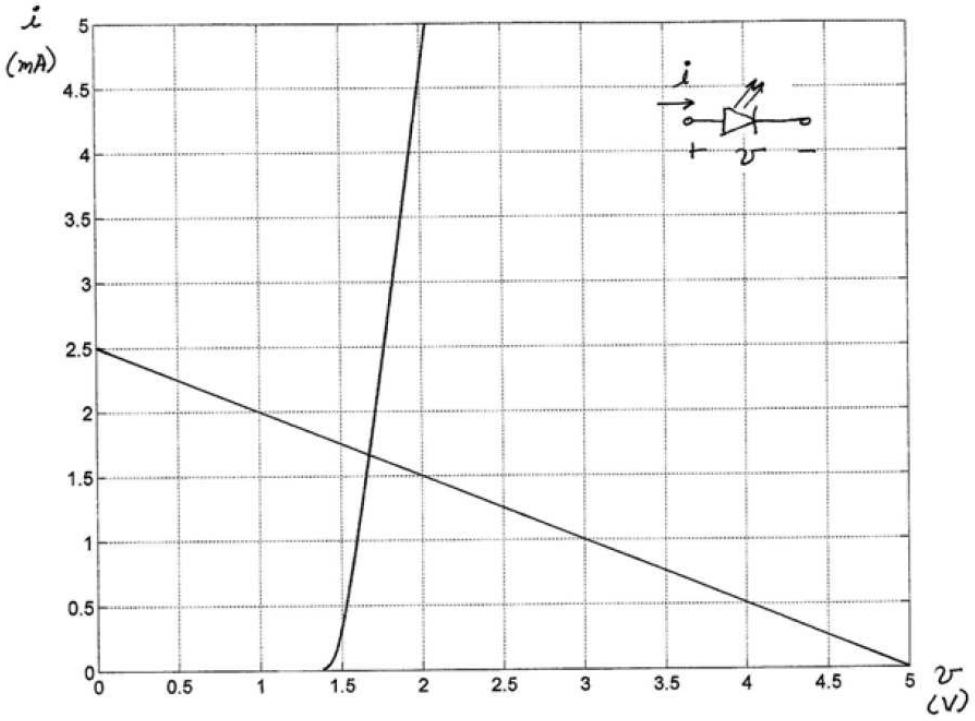

Figure 14: Load Line (b) in given I-V Characteristic

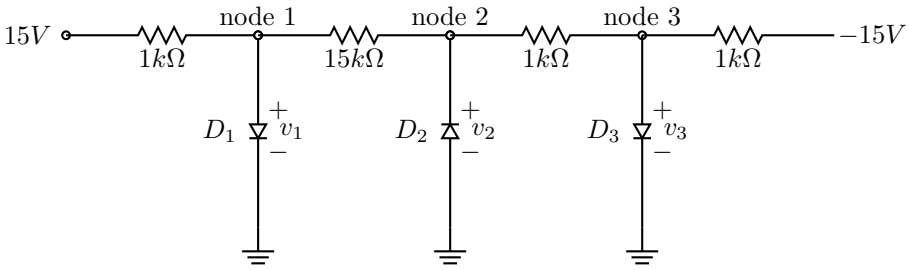

Figure 15: Circuit P10.38 (a)

10. P14.12 We can verify that negative feedback is present by noting that a positive perturbation in v_o causes a decrease in i_D and hence an increase at the $-$ input of the op-amp, which acts to restore the output from the perturbation.

We get the circuit in Figure 17. We have

$$v_1 = v_2 = 0$$

by the summing point constraint.
Hence,

$$i_1 = \frac{V_{in}}{R}$$

and so

$$i_D = i_1 = \frac{V_{in}}{R}$$

This gives

$$\begin{aligned} v_D &= nV_T \ln \frac{i_D}{I_S} \\ &= nV_T \ln \frac{V_{in}}{RI_S} \end{aligned}$$

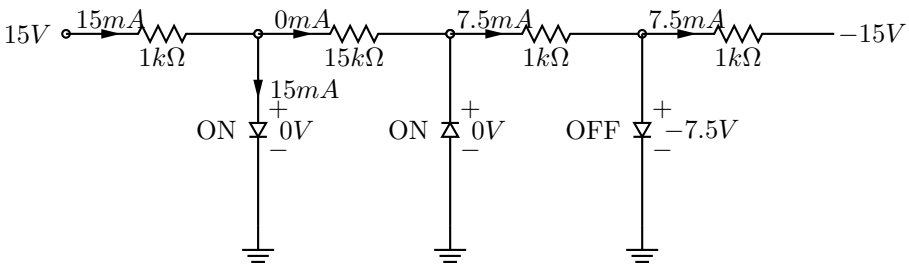

Figure 16: Solution Diode Circuit

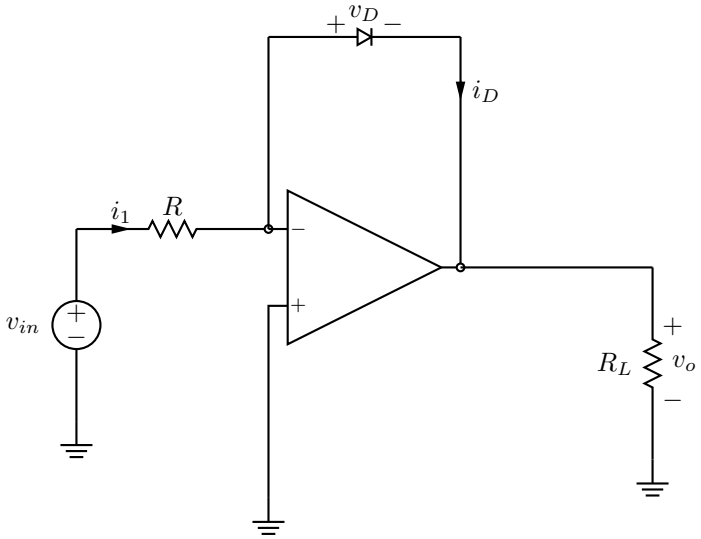

Figure 17: Diode Circuit with Op-Amp

Finally,

$$v_o = -v_D = nV_T \ln \frac{RI_S}{V_{in}}$$

Note that load line analysis was not needed. In general, it would be needed.