EE 40: Introduction to Microelectronic Circuits
Spring 2008: HW 8
Solution
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1. P10.7

![i-v characteristics for 10.7](image)

Figure 1: i-v characteristics for 10.7

2. P10.28

One way to keep the voltage \( v_L \) constant is for the Zener diode to be in the breakdown regime, with \( v_L = 5V \). We write a KVL equation to see that

\[
V_s - 5 = R_s(i_z + i_L).
\]

For consistency with the assumption that we are in breakdown region, we require that \( i_Z \geq 0 \) (with equality occurring at the boundary of the breakdown region). This translates to requiring that \( V_s - 5 - R_s i_L \geq 0 \), or, equivalently, that

\[
R_s \leq \frac{V_s - 5}{i_L}.
\]

Because this must be satisfied for *all* \( V_s \) and \( i_L \) given in the problem, \( R_s \) must be smaller than the constraint when it is tightest. This happens when \( V_s = 10 \) and \( i_L = 100mA \), so \( R_s \leq 50\Omega \) guarantees that \( i_z \geq 0 \) and our assumption of breakdown is consistent.
(For any value of \( R < 50\Omega \), the Zener diode will be in breakdown throughout the entire range \( 5 \leq V_s \leq 9 \) and \( 50 \leq i_L \leq 100\text{mA} \). The current \( i_Z \) through the Zener diode will adjust appropriately).

The power dissipated in the resistor is \((V_s - 5)^2/R_s\) when the source voltage is \( V_s \) and the resistor has value \( R_s \leq 50\Omega \). If we make the choice \( R_s = 50\Omega \), the resistor voltage range from 5 to 9V, and we’ll have a power dissipation ranging from \( 25/50 = 0.5\text{W} \) to \( 81/50 = 1.62\text{W} \). Hence the max power dissipated is 1.62W.

3. P10.36

(a) The diode is on
\[ V = 0, \quad I = \frac{10}{(2.7 \times 10^3)} = 3.7 \times 10^{-3}\text{amps}. \]

(b) The diode is off
\[ V = 10V, \quad I = 0. \]

(c) The diode is on. No current can flow through the bottom resistor because no voltage can drop across it.
\[ V = 0, \quad I = 0. \]

(d) The diode is on. Since no voltage can drop across it the current splits evenly between the two branches
\[ V = 5V, \quad I = 5\text{mA}. \]

4. P10.48

(a) If we assume the diode acts as an open circuit we get \( v_1 = 2V \) and \( v_2 = 1V \). This means 1V drops across the diode in the forward bias regime. But this would imply that the diode is on, contradicting the assumption that it acts as an open circuit.

(b) If we assume the diode is on, we can replace it by a voltage source of 0.7V. We can then use nodal analysis to solve the circuit, treating the two terminals of the diode as a floating voltage source. We get the KCL equations
\[
\frac{4 - (v_2 + 0.7)}{200} + \frac{4 - v_2}{300} = \frac{v_2 + 0.7}{200} + \frac{v_2}{100}
\]
where we have used \( v_1 = v_2 + 0.7 \).
This gives \( v_2 \simeq 1.13V \) and \( v_2 \simeq 1.83V \).
We need to check that \( i_D \geq 0 \) for consistency. We write a KCL equation to verify this:
\[
i_D = \frac{4 - v_1}{200} - \frac{v_1}{200} = 1.71\text{mA}
\]

5. P10.55

Since the average voltage is 9V and the average load current is \( I_L = 100\text{mA} \) the load (which we assume is resistive) is \( R_L = 90\Omega \). Since the peak-to-peak ripple is to be 2V, we take the voltage source to have \( V_m = 10V \).
Here \(10 = 9 + 2 \times 1/2\). The frequency of the source is 60Hz, so the period is \(T = 1/60\) seconds. We should therefore use a smoothing capacitor in parallel with the load with capacitance chosen according to the formula

\[
C = \frac{I_L T}{2 V_r} \text{ see equation 10.12}
\]

\[
= \frac{0.1 \times 1/60}{4} = 41.67 \mu F
\]

The circuit looks like (see Fig. 2)

6. P10.63

When \(V_s(t)\) is positive, diode \(D_3\) is off and the series connection of diode \(D_1\) with Zener diode \(D_2\) is also off till \(v_s(t)\) exceeds 10V, at which point the series connection becomes on. Subsequently the difference between \(v_s(t)\) and 10V drops entirely across the resistance of 2kΩ.

When \(v_s(t)\) is negative, diode \(D_3\) is on, the series combination of the diode \(D_1\) with the Zener diode \(D_2\) is off, and the entire source voltage drops across the resistance.

See Fig. 3 for the result.

7. P10.71

The diodes are assumed to be ideal.

Let the voltages across the capacitors \(C_1\) and \(C_2\) (assumed to be approximately DC because the capacitors are large) be denoted by \(V_1\) and \(V_2\) as indicated in Fig. 4. Then

\[
V_A = V_1 + V_m \sin(\omega t)
\]

\[
V_B = V_2
\]

The diode \(D_2\) must be forward biased at some point in the cycle to maintain the situation that the capacitor \(C_2\) is charged. Since no voltage can
drop across $D_2$ in forward bias this means, under our approximation that the capacitor voltages are DC, that we can write

$$V_1 + V_m = V_2,$$

i.e. the peak value of $V_A$ barely equals the value of $V_B$.

Diode $D_1$ cannot have any voltage drop across it in forward bias. Thus $V_1 + V_m \sin(\omega t) \geq 0$. In theory any value of $V_1$ consistent with this condition would be consistent with the mathematical assumption. However, physics tells us that any excess charge on capacitor $C_1$ would be drawn off through $D_2$ to dissipate in the resistance $R_L$, so the correct solution, under our approximations, is the one where this equation is barely true; i.e. we have

$$V_1 - V_m = 0.$$

(The maximum value of $V_1 + V_m \sin(\omega t)$ barely satisfied the requirement).

Putting the two equations together, we get

$$V_2 = 2V_m$$

This explains why the circuit is called a voltage doubler circuit.
8. P10.74

(a) There are many possible solutions. If one follows the idea suggested in Figure 10.31 on pg 494 of the textbook, one solution would be that of Fig. 5.

(b) It is unclear from the problem’s diagram what is supposed to happen for $V_{in} \leq 0$. We make it easiest by accepting any output for $V_{in} \leq 0$. See Fig. 6. The problem is trickier if you interpret it as asking that $v_0 = 0$ for $V_{in} \leq 0$. In this case we would like to add a parallel branch that becomes a short when $V_{in} \leq 0$. This could be accomplished by putting a diode (pointing up) in series with a 0.7 voltage source oriented the opposite way. How do we make such a voltage source, using, as the problem constrains us, only 15V sources, and diodes? We recall that we can build a voltage source of any value by using a diode with that breakdown or forward bias voltage, and applying a voltage to it that forces it into the desired regime. Hence, the new circuit will look like (see Fig. 7):
The op-amp is ideal, but its output is limited to the range \([-v, v]\) by the supply voltages.

\(v_B(t)\) will drop across the series combination of resistors, so \(v_1(t) = v_B(t)/2\).

When \(v_A(t) < v_1(t)\) we would have \(v_B(t) = V\) because of the infinite differential gain of the op-amp and because the output is limited by the supply voltages. This means the capacitor voltage \(v_A(t)\) (referred to ground) will begin to climb towards \(V\). At some point it will cross \(V/2\) which will make \(v_B(t)\) switch to \(-V\), taking \(v_1(t)\) to \(-V/2\). Now the voltage across the capacitor will discharge towards \(-V\). When it crosses \(-V/2\) we have \(v_B(t)\) switching again to \(V\) (and \(v_1(t)\) to \(V/2\)) so the cycle repeats.

If the circuit has been operating for a long time, the cycle structure can be understood by considering the following two circuits:

Circuit 1 (see fig. 9) with initial conditions \(v_A(0) = -V/2\)

\[
\begin{align*}
RC \frac{dv_A(t)}{dt} + v_A(t) = V, \quad \text{with initial condition } V_A(0) = -V/2
\end{align*}
\]

Figure 9: Circuit 1 for problem 9

and followed till \(V_A(t) = V/2\).

For Circuit 1 We have the equation

\[
RC \frac{dv_A(t)}{dt} + v_A(t) = V, \quad \text{with initial condition } V_A(0) = -V/2
\]

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with solution
\[ v_A(t) = -V/2 + \frac{3V}{2} \left(1 - e^{-t/RC}\right) \]
to be followed till \( V_A(t) = V/2 \), i.e. up to time \( RC \ln 3 \)
and we have Circuit 2 (see Fig. 10) with initial conditions \( v_A(0) = V/2 \)
and followed till \( V_A(t) = -V/2 \).

\[ v_A(t) = \frac{V}{2} - \frac{3V}{2} \left(1 - e^{-t/RC}\right) \]
to be followed till \( V_A(t) = -V/2 \), i.e. up to time \( RC \ln 3 \).

Putting the two together, we can solve the problem (see Fig. 11): where

we have arbitrarily chosen the situation at time \( t = 0 \) as the one where
\( v_B(t) \) switches from \(+V\) to \(-V\).
(a) The best way to do this would be following the book’s example, yielding the circuit shown in fig. 12. Then the current $i_1$ through the resistance $R_1$ equals $(V_{off}/10)$ mA (assuming $V_{off}$ is measured in Volts).

Since $i_2 = i_1$, we have

$$v_o = -V_{off} - 100i_1 = -11V_{off}$$

It is required that $|v_o| \leq 0.1$.

This would require $|V_{off}| \leq 100/11$ mV.

You could also have drawn the offset voltage at the other opamp terminal without any problem, if you did it as in figure 13. Then the answer does not change at all (assuming reference directions as in the figure).

During class there was a small mistake, and offset voltage was drawn as in figure 14. In this case, we have the familiar circuit which yields $v_o = -\frac{R_2}{R_1}V_{off}$, and enforcing the constraining that $|v_o| \leq .1V$, we get

$$\frac{.1V}{|V_o|} = \frac{R_2}{R_1}|v_{off}|,$$
so we require
\[ |v_{\text{off}}| \leq \frac{R_1}{R_2} \cdot 1V = 10mV \]

(b) Since both inputs of the opamp are at ground, the current \( i_1 \) equals 0. Hence \( i_2 = -I_B \). This implies that \( v_0 = 100I_B \) (where \( I_B \) is measured in mA and \( v_0 \) is measured in Volts).

It is required that \( |v_o| \leq 0.1 \).

This would require
\[ |I_B| \leq 1mA. \]

(c) The scheme described in Fig 14.31 on pg. 697 of the book can be used to cancel the effects of the bias current. The resulting circuit (viewed as a 2-port) would look like fig. 16

(d) Note that the book’s convention for offset current is correct in Fig.14.29 rather than 14.30d. However, the answer will only differ up to a sign. See Fig. 17

Since \( i_3 = I_{\text{off}}/2 \), the voltage at the + input of the opamp is \(-\frac{100}{1} \cdot \frac{I_{\text{off}}}{2}\) (where \( I_{\text{off}} \) is measured in mA and the voltage is mea-
sured in Volts). This equals the voltage at the − input of the opamp (by the summing point constraint) so we have

\[-10i_1 = -\frac{100}{11} I_{\text{off}}.\]

i.e. \[i_1 = \frac{10}{11} I_{\text{off}}.\]

This gives \[i_2 = \frac{I_{\text{off}}}{2} + \frac{10}{11} I_{\text{off}} = \frac{21}{11} I_{\text{off}}\]

so \[v_0 = -\frac{100}{11} \frac{I_{\text{off}}}{2} - 100 \frac{21}{11} I_{\text{off}} = -100 \frac{22}{11} I_{\text{off}} = -200 \frac{I_{\text{off}}}{2}.\]

The result

\[v_0 = -100I_{\text{off}}\]

is simply off by a sign if \(I_{\text{off}}\) is chosen to point in the opposite direction. It is required that \(|v_0| \leq 0.1\ V\). This would require \(|I_{\text{off}}| \leq (0.1/100)\ mA = 1 \mu A\) (because of the absolute value, the direction of \(I_{\text{off}}\) ends up not mattering.

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Figure 16: 2-port view of circuit, for P14.68c
Figure 17: Answer to P14.68d