Supplementary Reader

EECS 40
Introduction to Microelectronic Circuits

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Note: This set of notes is intended to supplement the text book and not to replace it.

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Acknowledgements

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Chapter 1. Bode Plots

1.1 Introduction

Bode plots are widely used in various fields of engineering because they characterize the magnitude and the phase response of a system. In this section, we will present step-by-step analysis to create the Bode plots of a given transfer function. We analyze the trend of the transfer function at different frequency regimes based on the value of the break or resonant frequency. This approach helps to understand the frequency behavior of the circuit, and also works for first order, second and higher order circuits.

1.2 First Order Circuits

1.2.1 General Construction and Break Frequency

A Bode plot illustrates the behavior of a circuit by generalizing its response into *trends* and graphing it against a log scale of frequency. Given a transfer function, $H(\omega)$, we may produce a magnitude and phase Bode plot. In each plot, we break down the analysis of the transfer function into 3 regimes, depending on the frequency in question:

1. At $\omega=\omega_B$,
2. when $\omega<<\omega_B$, or when ω is much less than the break frequency
3. when $\omega>>\omega_B$, or when ω is much greater than the break frequency

The break frequency, ω_B , is a property of the filter that can be found by examining the transfer function. It describes the frequency where the trends on the Bode plot are broken, where one trend (when $\omega<<\omega_B$) ends and the next (when $\omega>>\omega_B$) begins.

For first-order circuits, the break frequency can be found by looking solving for the frequency at which the real and complex components are equal.

Example 1 – Find the Break Frequency

Given the transfer function $H(\omega)=\frac{1}{1+j\omega RC}$. We find the break frequency by examining the denominator, because it consists of two terms, 1 and $j\omega RC$. The first term is real and has a ω^0 dependence. The second term $j\omega RC$ has a ω^1 dependence. The break frequency, ω_B, occurs when the MAGNITUDE two components are equal. Thus, the break frequency for a filter with this transfer function is at $\omega_B=\frac{1}{RC}$.

After finding the break frequency, we can examine the trends on either side of ω_B . When $\omega << \omega_B$, the real term (in the denominator of Exp. 1) dominates and we ignore the imaginary component. When $\omega >> \omega_B$, ω dominates real term, so we work with only the imaginary term, as will be shown next.

Note: We can only disregard terms that are added and subtracted and not those that are multiplied or divided when making approximations.

e.g For a<<b, a<c and c<<d, $a \times \frac{(c+d)}{b} \approx \frac{ad}{b}$

Try to plug in any number you like and see if it is true.

1.2.2 Bode Magnitude Plot

For the magnitude plot, we plot on the y-axis: the 'square' of the magnitude of the transfer function, $H(\omega)$ in decibels (unit dB). This is because the transfer function describes the output to input voltage ratio. Since power is proportional to V^2, we plot $|H(\omega)|^2$, which in dB is:

$$\begin{aligned} |H(\omega)|_{dB} &= 10\log|H(\omega)|^2 \\ &= 20\log|H(\omega)| \end{aligned} \qquad (1)$$

Both of these expressions can be useful, depending on the form of the transfer function. We plot $|H(\omega)|_{dB}$ on the y-axis, against a logarithmic scale of ω on the x-axis. One thing to keep in mind about logarithmic functions is the ability to pull multiplicative factors out, for instance:

$$20\log(A \times B) = 20\log A + 20\log B$$

$$10\log(\frac{C}{D}) = 10\log C - 10\log D$$

The key to our analysis is that we identify and examine the dominant terms of the transfer function in each of the 3 regimes in the following.

(1) At $\omega = \omega_B$, we simply plug ω_B in $|H(\omega)|_{dB}$ and get the actual value.

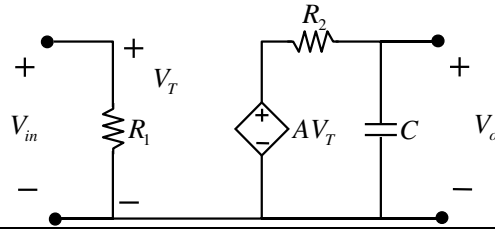
(2) When $\omega << \omega_B$. Examine SEPERATELY in the numerator and denominator all terms containing ω (e.g. ω^0 , ω^1). The one with the lowest power (e.g. ω^0) dominates in this frequency range. Hence we keep only the dominating term, one each for the numerator and denominator, respectively. The resulting formula will be used to determine the asymptotic behavior , or "trend".

(3) When $\omega >> \omega_B$. Again, we examine the numerator and denominator separately. Leave only the term with the highest power (ω^1 in the previous example), one each for numerator and dominator. The resulting formula will be used to determine the asymptotic behavior , or "trend".

By analyzing these three regimes, we can construct the magnitude Bode plot. We start at the break frequency, $\omega = \omega_B$, and then plot the trends for $\omega << \omega_B$ and $\omega >> \omega_B$.

Example 2 – Find the Transfer Function, $H(\omega)$, and plot the magnitude Bode Plot.

Given the following circuit, construct the magnitude Bode plot.



$A = 100$
$R_1 = 200\Omega$
$R_2 = 1k\Omega$
$C = 10 \ \ F$

We can see $V_T = V_{in}$ By voltage divider, we have: $V_{out} = \frac{Z_c}{Z_c + R_2} A V_{in}$

where $Z_c = \frac{1}{j\omega C}$

Thus, the transfer function is given by:

$$H(\omega) = \frac{V_{out}}{V_{in}} = \frac{Z_c}{Z_c + R_2} A$$
$$= \frac{1/\, j\omega C}{1/\, j\omega C + R_2} A = \frac{A}{1 + j\omega R_2 C}$$

The magnitude plot will be the transfer function in dB, or:

$$|H(\omega)|_{dB} = 20\log|H(\omega)|$$
$$= 20\log\left|\frac{A}{1 + j\omega R_2 C}\right|$$

Plotting this function would yield the exact behavior of our filter, but we only need the asymptotic behavior for the Bode plot. Now we begin a 3-part analysis.

Step 1: Break Frequency

Setting equal the real and imaginary components in the denominator, we find the break frequency:

$$\omega_B = \frac{1}{R_2 C} = \frac{1}{(1\,\text{k}\Omega)(10\,\mu\text{F})}$$
$$= \frac{1\,\text{rad}}{10^{-2}\,\text{s}} = 100\,\text{rad/s}$$

Step 2: Asymptotes

(1) At $\omega = \omega_B$,

$$|H(\omega_B)|_{dB} = 10\log\left|\frac{A}{1+j}\right|^2 = 10\log\left(\frac{A}{\sqrt{2}}\right)^2 = 10\log\left(\frac{A^2}{2}\right)$$
$$= 20\log A - 10\log 2 = 20\log A - 3dB$$

With A = 100, $|H(\omega_B)|_{dB} = 37$ dB. The first line of the above steps shows that at ω_B, the output is at half the maximum power (-3dB is half in linear scale); the transfer function (voltage) has a value of $A/\sqrt{2}$, and power is proportional to the square of voltage. The break frequency for a first-order circuit is also referred to as the half-power frequency, where the output is one-half the maximum power. The factor of 1/2 in the logarithm can be expanded out to -20 log 2:

$$10\log\left(\frac{1}{2}\right) = 10\log 1 - 10\log 2 = 0 - 10\log 2 \cong -3\,\text{dB}$$

The half-power frequency is -3dB below the maximum power, so we also call ω_B the -3dB frequency.

(2) For $\omega << \omega_B$, the constant 1 dominates in the denominator and is the only term to be kept.. The transfer function can be approximated as: $H(\omega) \cong \frac{A}{1+0} = A$

which is purely real, so $|H(\omega)|_{dB} = 20\log A$ and $|H(\omega)| = |A| = A$

Substituting the gain factor, A = 100, we obtain $|H(\omega)|_{dB} = 20\log 100 = 20\times 2 = 40\,\text{dB}$.

(3) Next, for $\omega >> \omega_B$, the ω term dominates in the denominator term, and the transfer function can be approximated as:

$$H(\omega) \cong \frac{A}{j\omega R_2 C}$$

$$|H(\omega)|_{dB} = 20\log\left|\frac{A}{j\omega R_2 C}\right| = 20\log\left|\frac{A}{R_2 C}\right| - 20\log|j\omega|$$

$$= 20\log\frac{A}{R_2 C} - 20\log\omega = C' - 20\log\omega$$

In the asymptote, the filter's magnitude decreases at a rate of 20 dB/decade (a 10x increase in ω). Here C' is a constant and we can simply connect the curve for $\omega >> \omega_B$ with the point $|H(\omega_B)|_{dB} = 37\,\text{dB}$. The magnitude $|H(\omega_B)|_{dB}$ decreases by 20 dB at $10\,\omega_B$, 40 dB at $100\,\omega_B$, and so on.

With these three regions analyzed, the magnitude Bode plot is complete and shown in Fig. 1.

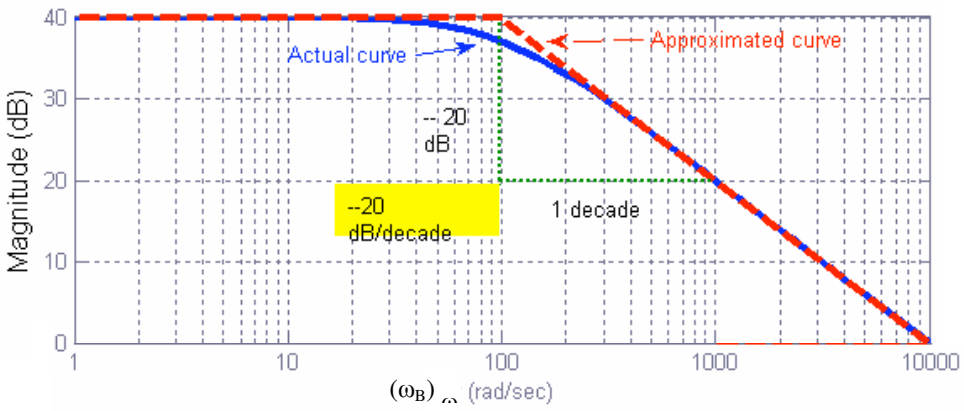


Fig. 1. Magnitude Bode Plot for H(ω) of Example 2, with the gain factor A = 100.

The dotted straight lines in Fig. 1. form the Bode plot. Note how it approximates the behavior of the actual function, shown in blue.

NOTE: This is an example of low-pass filter. The low frequencies are kept by the filter and the high frequencies are filtered out. First-order circuits are either high-pass or low-pass filters.

Exercise 1:

What if the voltage across the resistor R_2 (Example 2) is taken as the output? Is the total energy conserved in each frequency?

1.2.3 Bode Phase Plot

The Bode phase plot is constructed in a similar manner to the magnitude plot except we use limits (instead of trends). We first find the expression for phase, $\angle H(\omega)$, from the transfer function, $H(\omega)$. For $\omega << \omega_B$, we take the limit of $\angle H(\omega)$ as $\omega \to 0$. At $\omega = \omega_B$, we use the complete expression for $\angle H(\omega)$, as both the real and imaginary components have equal magnitude. For $\omega >> \omega_B$, we find the phase by taking the limit of $\angle H(\omega)$ as $\omega \to \infty$. We then construct the Bode phase plot by performing the following:

Plot lower-frequency limit value (from x $\omega << \omega_B$ to $\omega_B/10$),

Plot upper-frequency limit value (from x=10ω_B to $\omega \to \infty$)

Plot the value for $\omega = \omega_B$

Connect the extremes by curve (arctan) lines.

Example 3 – Find the Phase, $\angle$, of a Transfer Function, $H(\omega)$

Using the transfer function of Example 2,

$$H(\omega) = \frac{A}{1 + j\omega R_2 C}$$

We find the net phase, $\angle H(\omega)$, by subtracting the phase of the denominator from the phase of the numerator:

$$\angle H(\omega) = 0 - \tan^{-1}\left(\frac{\omega R_2 C}{1}\right)$$
$$= -\tan^{-1}(\omega R_2 C)$$

To plot the expression for phase in Exp. 3, we examine our 3 regions. Taking the limit of $\angle H(\omega)$ as $\omega \to 0$, we find the lower-frequency asymptote, $\omega << \omega_B$.

$$\lim_{\omega \to 0} \angle H(\omega) = -\tan^{-1}(0) = 0$$

The upper-frequency asymptote, $\omega >> \omega_B$ is found by taking the limit as $\omega \to \infty$:

$$\lim_{\omega \to \infty} \angle H(\omega) = -\tan^{-1}(\infty) = -90 \quad or -\frac{\pi}{2}$$

At the break frequency, $\omega_B = \frac{1}{R_2 C}$, we find the phase to be:

$$\angle H(\omega_B) = -\tan^{-1}(1) = -45 \quad or -\frac{\pi}{4}$$

This value is in agreement with a line drawn between the upper and lower asymptotes; ω_B is halfway between $\omega_B/10$ and $10\omega_B$, and -45° is halfway in between 0° and 90°. The phase Bode plot of Exp. 3 is shown in Fig. 2.

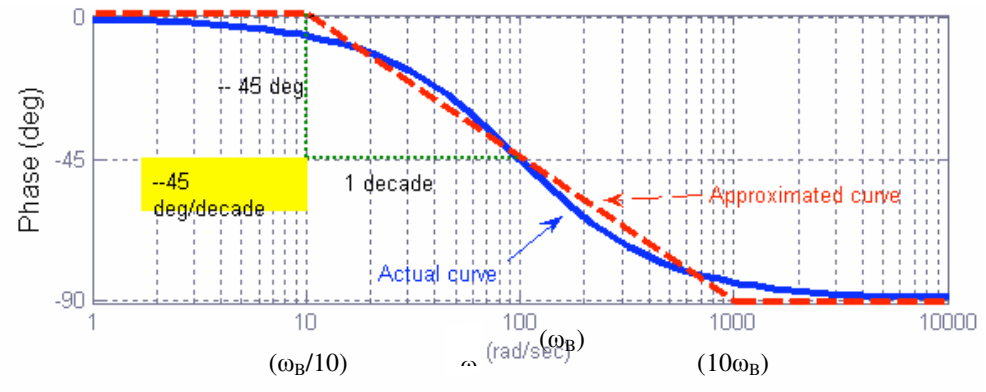
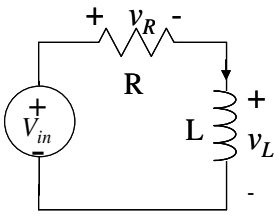


Fig. 2. Phase Bode Plot for H(ω) of Example 2.

As before, the dotted lines in Fig. 2 outline the phase Bode plot for our transfer function, but the actual values are shown by the solid line. Note that with our approximation, in the intermediate region between $\omega_B/10$ and $10\omega_B$, the phase decreases by 45 degrees per decade of angular frequency, and outside this region, the phase is constant (the asymptote).

Exercise 2: Find the Transfer Function, $H(\omega)$, and plot Bode magnitude and phase plots for (a) $V_{out}=V_L$ and (b) $V_{out}=V_R$. In both cases, do we have high-pass or low-pass filters?



1.3 Second Order Circuits

1.3.1 General Construction and Resonant Frequency

As with Bode Plots for first-order circuits, the transfer function for second-order circuits can be found by writing an equation relating V_{out} and V_{in}. Once this equation is written, an expression for $H(\omega)$ is easily obtained. You can use this transfer function to find its magnitude and phase.

Similar to first-order circuits, we depict the behavior of second-order circuits by plotting trends of the transfer function at three frequency regimes relative to a certain resonance frequency, ω_0:

1. At $\omega=\omega_o$
2. For $\omega<<\omega_o$, or in other words, the limit as $\omega\to 0$
3. For $\omega>>\omega_o$, or in the limit as $\omega\to\infty$

Around the resonant frequency, the magnitude of the transfer function $|H(\omega)|$ ***changes trend*** and ***often reaches the maximum or minimum value***. Though whether it reaches the maximum or minimum depends greatly on the Q value, which will be discussed next, the trend is always changed at the resonance frequency.

The resonant frequency, ω_0, can be found by setting the complex part of either numerator or denominator of the transfer function to zero. This is because the magnitude of $a+jb$ reaches minimum when b=0. If we have a complex term $a+jb$ on the numerator, by letting b=0, we reached minimum, whereas if this complex term is in the denominator, we reached maximum.

Example 4: Finding the resonant frequency

For a circuit with transfer function as $H(\omega)=\dfrac{R}{j\omega L+R-j\dfrac{1}{\omega C}}$

What is ω_o, the resonant frequency?

Solution:

The numerator is R, which has no frequency dependence term and hence irrelevant for this question. We look at the denominator. The resonant frequency is when

$j\omega L-j\dfrac{1}{\omega C}=0$ Hence, $\omega_o=\dfrac{1}{\sqrt{LC}}$

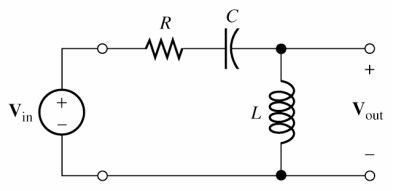
1.3.2 Bode Magnitude Plot

Constructing Bode Plots for second-order circuits is the same as for first-order circuits, so analyzing trends consists of the same process mentioned earlier – finding the dominant term amongst now typically three terms (ω^{-1} , ω^0 , ω^1) in both numerator and denominator ***separately***.

Example 5 below shows how to construct a Bode magnitude plot. Note, that in most Bode Plot problems, you will be asked the slope at which lines are ascending and descending. By using the techniques of Example 2, you will be able to answer such questions very easily.

Example 5: Constructing the transfer function and Bode magnitude Plot

Construct the magnitude Bode Plot for the circuit shown in the diagram below. Also, label the slopes of any lines in the plot.



First, write the output voltage in terms of the values given. Notice that all the electrical components of the circuit are in series, so applying the voltage-divider technique gives the following:

$$V_{out} = \frac{j\omega L}{R + j\omega L + \frac{1}{j\omega C}} V_{in} \qquad (1)$$

So, the transfer function becomes:

$$H(\omega) = \frac{j\omega L}{R + j\omega L + \frac{1}{j\omega C}} \qquad (2)$$

Step 1: Finding the Resonance Frequency

The magnitude for (2) is the magnitude of the numerator divided by the magnitude of the denominator. Remembering that the magnitude for a complex number, $a + bi$, is $\sqrt{a^2 + b^2}$, we obtain the following:

$$\left|H(\omega)\right| = \frac{\omega L}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}} \qquad (3)$$

This is an example that we cannot simply use the definition of $\left|H(\omega)\right|$ reaching maximum or minimum, because we have a ω dependence on the numerator. However, we can use the definition of breaking trends. The denominator has three terms, ω^{-1}, ω^0 and ω^1. The trend is either dominated by ω^{-1} or ω^1 at very low or high frequencies, respectively. At the resonant frequency, only the ω^0 term will dominate.

Hence, $\omega_0 L - \frac{1}{\omega_0 C} = 0$.

And $$\omega_0 = \sqrt{\frac{1}{LC}} \qquad (4)$$

Note: This resonant frequency is the same formula we got using second-order differential equation on slide 177 of EE40 Reader! (Surprise or not a surprise?)

Step 2: Asymptotes

Now, we must analyze this magnitude function in the three regimes mentioned above.

(1) For $\omega << \omega_o$, the numerator has only one term, so we leave it alone. For the denominator, we compare the three terms and keep only the dominant one. In this case, we will keep the $(\omega C)^{-1}$ term.

So, we obtain the following equation:

$$|H(\omega)| = \frac{\omega L}{(\frac{1}{\omega C})} = \omega^2 LC$$

$$Or \qquad (5)$$

$$|H(\omega)|_{dB} = 10\log(\omega^2 LC)^2 = 40\log(\omega) + 20\log(LC)$$

Note that as $\omega \to 0$, $|H(\omega)|$ goes to 0, which means that $|H(\omega)|_{dB}$ goes to $-\infty$. Note that the x-axis on a Bode Plot is $\log(\omega)$ and the y-axis is $|H(\omega)|_{dB}$, so equation 5 is of the form:

$y = 40x + B$ where B is a constant

This says that the slope of the Bode magnitude plot for $\omega << \omega_o$ is 40 *dB/decade*.

(2) For $\omega >> \omega_o$, we will keep only the ωL in the denominator of the transfer function. This gives the magnitude as:

$$|H(\omega)| = 1$$

$$OR \qquad (6)$$

$$|H(\omega)|_{dB} = 10\log(1) = 0dB$$

This means that the output remains unchanged for large values of ω and the slope is 0 *dB/decade*.

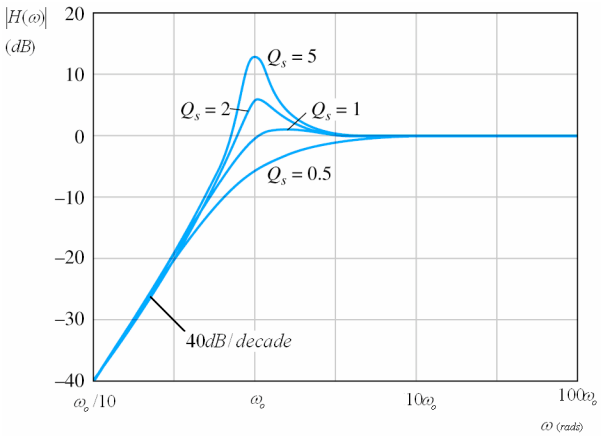
(3) At $\omega = \omega_o$,

$$|H(\omega)| = \frac{\sqrt{(\omega_o L)^2}}{\sqrt{R^2 + (\omega_o L - \frac{1}{\omega_o C})^2}} = \frac{\sqrt{(\omega_o L)^2}}{\sqrt{R^2}} = \frac{\omega_o L}{R} = \frac{1}{\omega_o RC} = Q_S$$

$$OR \qquad (7)$$

$$|H(\omega)|_{dB} = 20\log(Q_S)$$

The Bode magnitude Plot for this circuit is shown below.



This is a high-pass filter which rejects low frequencies while leaving the high frequency content unchanged. Note, this is better than the first-order high-pass filter because the slope of this filter in the low-frequency region is steeper, $40dB/decade$, rather than the $20dB/decade$ slope of the first-order filter. The increased slope provides stronger discrimination against the unwanted low frequencies.

Also note, a high value of Q_S means a large hump in the figure below. As Q_S increases, so does the value of $|H(\omega_o)|_{dB}$. At $Q_S = 0.5$, $|H(\omega_0)|_{dB} = 20\log(Q_S) = -3dB$; this curve resembles a first-order filter the most with only exception that the slope of filtered frequency is steeper.

Note:

$$Q_S = \frac{1}{2\zeta}$$

(Surprise or not a surprise?)

Hence when Q_s=0.5, ζ=1 , we have critically damped circuit.

When Q_s>0.5, ζ<1, we have under-damped circuit, whose signal, in the time domain, oscillates a great deal (slide 178, EE40 Reader). This can also be seen with the frequency response, we see $|H(\omega_o)| > 1$ or $|H(\omega_o)|_{dB} > 0dB$. Likewise, we have an over-damped circuit with Q_s<0.5.

Exercise 1 Find the Transfer Function, $H(\omega)$, and plot Bode magnitude plot for $V_{out}=V_C+V_R$ .in Example 5. Do we have high-pass or low-pass filter? Is the energy conserved at ω_0?

Exercise 2 Repeat the exercise for $V_{out}=V_C$ .in Example 5. What kind of filter is this?

Exercise 3 Repeat the exercise for $V_{out}=V_C+V_L$. in Example 5. What kind of filter is this?

1.3.3 Bode Phase Plot

Constructing the phase plot is done in a similar manner to the magnitude plot. After finding the transfer function, you can find its phase. Remember that the phase of a function is the phase of the numerator minus the phase of the denominator, and the phase of a complex number, $a+bi$, is $\arctan(b/a)$. After finding

the phase function, you must analyze the function in the same 3 regimes as was done for the magnitude plot. Follow the next example, which constructs a phase plot for the circuit in Example 2.

Example 6: Constructing the Phase Plot:

Construct the Phase Plot for the circuit shown in Example 5.

Solution:

The transfer function of example 2 is reproduced below:

$$H(\omega) = \frac{j\omega L}{R + j\omega L + \frac{1}{j\omega C}} \qquad (6\text{-}1)$$

The phase of the above transfer equation is:

$$\angle H(\omega) = 90^\circ - \arctan\left(\frac{\omega L - \frac{1}{\omega C}}{R}\right) \qquad (6\text{-}2)$$

Now, we must analyze this function in the same 3 regimes as before.

(1) For $\omega << \omega_o$ or as $\omega \to 0$, we can disregard the ωL term in the numerator of the second term since this value is approaching 0 and will not make a significant effect when added to other values. So, the above function reduces to:

$$\angle H(\omega) = 90^\circ - \arctan\left(\frac{-\frac{1}{\omega C}}{R}\right) = 90^\circ + \arctan\left(\frac{1}{\omega RC}\right) = 90^\circ + \arctan\left(\frac{\omega_0}{\omega}\frac{1}{Q_S}\right) \qquad (6\text{-}3)$$

Notice that as $\omega \to 0$, the argument to arctan in equation 3 becomes very large, so:

$$\angle H(\omega) = 90^\circ + 90^\circ = 180^\circ \qquad (6\text{-}4)$$

(2) For $\omega >> \omega_o$ or as $\omega \to \infty$, in equation 2, we can disregard the $(-1/\omega C)$ term in the numerator because it becomes very small and has a negligible effect when it is added to other values. So, equation 2 reduces to:

$$\angle H(\omega) = 90^\circ - \arctan\left(\frac{\omega L}{R}\right) = 90^\circ - \arctan\left(Q_S \frac{\omega}{\omega_0}\right) \qquad (6\text{-}5)$$

As $\omega \to \infty$, in equation 5, the argument to arctan becomes very large, so:

$$\angle H(\omega) = 90^\circ - 90^\circ = 0^\circ \qquad (6\text{-}6)$$

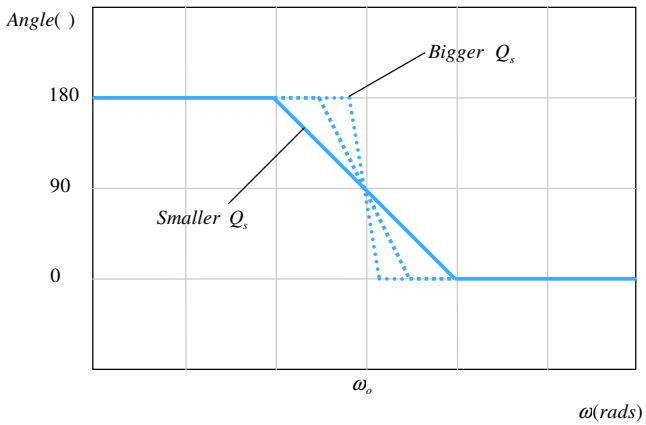
(3) At $\omega = \omega_o$, equation 2 becomes:

$$\angle H(\omega) = 90^\circ - \arctan\left(\frac{0}{R}\right) = 90^\circ \qquad (6\text{-}7)$$

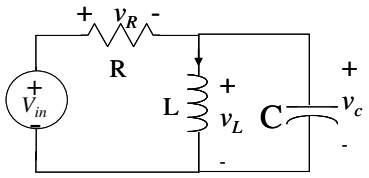
The figure below shows the phase plot for equation 2. As seen in the plot, for low frequencies, the phase completely changes, yet for high frequencies, it remains unchanged.

Note that as Q_S increases, the downward sloping line becomes steeper. This can be seen using either equation 6-3 for $\omega < \omega_0$ and 6-5 for $\omega > \omega_0$, respectively.

If Q_S could reach ∞, the downward sloping line would become vertical which approaches an ideal high-pass filter.



Exercise. Find the Transfer Function, $H(\omega)$, and plot Bode magnitude and phase plots for (a) $V_{out}=V_L$ and (b) $V_{out}=V_R$. In both cases, what filters do we have? Show the definition of Q is different for a parallel LC than a series LC circuit. Explain how is Q related to the damping ratio in this case.



1.3.4 Definitions

Table 1. Symbol Table for ω_o, Q_s and Q_p

Symbol	Definition
$\omega_o = 1/\sqrt{LC}$	The resonant frequency is defined to be the frequency at which the impedance is purely resistive.
$Q_s = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC}$	The quality factor for a series resonant circuit is defined to be the ratio of the reactance of the inductance at the resonant frequency (e.g. $\omega_o L$) to the resistance.
$Q_p = \frac{R}{\omega_0 L} = \omega_0 RC$	The quality factor for a parallel resonant circuit is defined to be the ratio of the resistance to the reactance of the inductance at the resonant frequency (e.g. $\omega_o L$).

Chapter 2. Diode Circuits

2.1 Physical Behavior of Diodes

A diode is a simple two terminal device. The two terminals are labeled anode (positive side) and cathode (negative side). The diode symbol used in a circuit is shown in Fig. 1a, with the definition of the plus and minus directions of voltage and current. A positive voltage applied to the diode is referred as a forward bias and negative, a reverse bias. In this part of the course, we will introduce three models to describe the current-voltage (I-V) characteristics of a diode: the ideal diode model, a simple piecewise model and the Shockley equation.

An ideal diode has only two modes of operation: off and on, as shown in Fig. 1b. When the diode is "off", it passes through no current but the voltage can be any value less than zero. It behaves like an open circuit. When the diode is "on", the voltage is clamped at zero while its current can be any positive value. Hence, it acts like a short circuit.

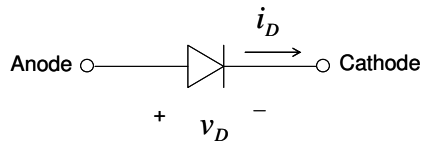


Fig. 1a circuit symbol of a diode (same as Hambley 10.1a)

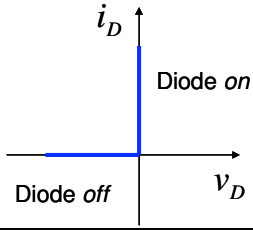


Fig. 1b Ideal diode current-voltage characteristics (on and off states are labeled)

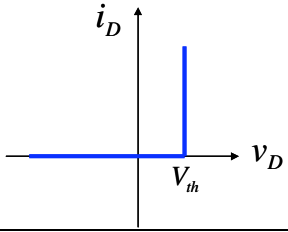


Fig. 1c Simple piecewise model (threshold voltage labeled)

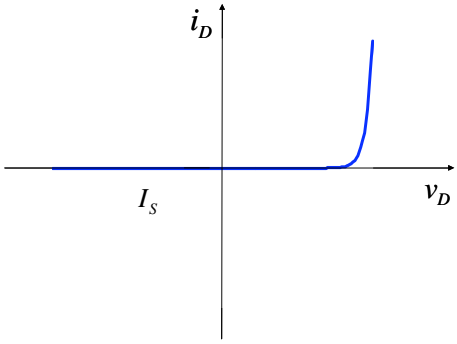


Fig. 1d Schockley equation

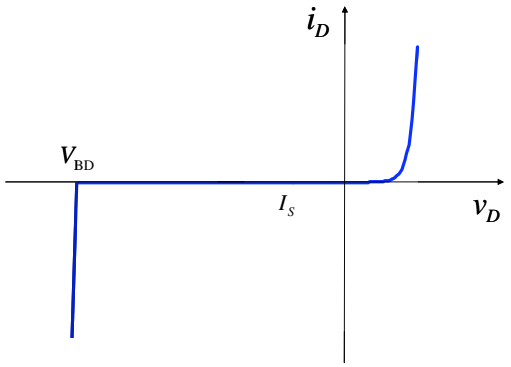


Fig. 1e real diode with breakdown voltage

The simple piecewise model is similar to the ideal diode model with "off" and "on" states being open and short circuit, respectively. The only difference is the inclusion of a threshold voltage. As shown in Fig. 1c, when the diode is biased below a certain threshold voltage, it is "off", i.e. the current passing through the diode is zero. When the diode is "on", voltage is clamped at this threshold voltage while current can be any positive value depending on the rest of the circuit. In EE 40, this threshold voltage is set to be 0.7 V. Note, this number is just a matter of convention and not based on fundamental physical laws. In this set of notes, this simple piecewise model is slightly different from the model used in section 10.5 of Hambley. This model is a simpler version of the piecewise-linear model described in 10.5, hence the name "simple piecewise model."

Shockley Equation model, shown by Fig. 1d, is more accurate than the first two. With forward bias, the current increases exponentially with voltage. For reverse bias, the current is negative and saturates at a saturation current. Since it is difficult to use this model to reach analytical solutions, for the circuits in this chapter, we use the ideal and simple piecewise model.

None of the models describe what happens when the voltage bias becomes a large but negative value, which is known as reserve bias breakdown voltage, for example, as in Zener diodes (Hambley 10.3). In the circuit analysis part of this course, we will simply add a reverse voltage as in 10.3. The physics behind the reverse breakdown phenomenon and the Shockley equation will be briefly discussed in the next Chapter. However, you will not see more detailed discussion until EE 105 and EE130, which I hope you will take next year.

Note, no matter which model you use, a diode has its I-V curve passes through the origin, i.e. with zero voltage there should be no current flow. The only exception is when unless there is an external source to generate electrons, e.g. in the case of sun light or laser beam shinning on a photodiode. In general, if we did not specifically mention photo-generation of electrons, zero voltage bias across a diode leads to zero current. Do not lose this "common sense" when dealing with diode problems.

$$I = 0 \longleftrightarrow V = 0$$

2.2 Solving Diode Circuits

2.2.1 Proof by Contradiction Approach

The proof by contradiction method uses guess-and-check, also discussed in the text book.

- For each diode in the circuit, "guess" an "on" or "off" state and replace it with the corresponding model (open circuit for "off", and 0.7 volt source for "on")
- If diode is assumed on, the current should flow into the positive terminal of the diode. If diode is assumed off, the voltage should be negative across the diode, i.e. reverse biased.

We apply the contra-positive of the second bullet above to contradict our guess. (If A→B, then Not B→Not A) In other words, if we solve the circuit and find a negative current through an "on" diode or a voltage greater than 0.7V across an "off" diode, we guessed the wrong states.

2.3 Load Line Analysis

Load line analysis is simply about finding the intersection point based on the physical characteristics of a device (the load), the physical characteristics of a driving circuit, based on fundamental laws such as KCL and KVL. For our present discussion, the diode is our load, but this powerful technique can be applied to other loads as well.

From the physical behavior of a diode, we know that a diode behaves in a certain way. This presents an I-V characteristic based on the model we choose. When this diode is placed in a simple circuit, the circuit will also want to dictate the way it behaves. In particular, by KVL, the driving circuit and the load must see the same voltage at their interface. In addition, the current out of the driving circuit must match the current into the load.. For the circuit to be consistent, both of these constraints must be satisfied. Therefore, we find the intersection of the curves representing the physical characteristic of a diode and the curve representing the manner in which the diode will behave when placed in a circuit (the load's IV curve, or "load line"). We call this intersection point, the "operating point", because it is the point at which the device will operate.

The physical characteristic of a diode (or other device) is sometimes represented by a set of family curves at different operating conditions. For example, in photodiode, two curves typically exhibit for the conditions with and without light illumination. In the case of MOSFET, characteristics are represented by I_{ds}-V_{ds} at different gate voltage (V_g) levels. But no matter how many curves are used to represent the physical characteristic of the diode, you are simply intersecting this characteristic with the behavior you obtain from analyzing the load in a circuit. Each intersection point of the characteristic and the load line indicates the Q-point in that particular condition.

The circuit may become more complicated than a simple source, diode, and resister in series. But even in a more complicated circuit, we can simplify the problem by first finding the Thevenin equivalent circuit of the linear portion of the circuit. Then, we can resort to the fundamental KVL principle to obtain the equation for the load line.

Once we find the load line equation using KVL, we can graph its I-V characteristic and find the solution from the intersection point. As shown in Fig. 2, as the source voltage is increased while keeping the

resistance constant, the load line is moved upwards in parallel to the original curve. The intersection point is changed accordingly. If, however, the value of the resistance is changed, the y-intercept of the load line is changed accordingly. When the resistance is decreased, the y-intercept increases, and the curve is pulled up with the same x-intercept. The official terminology for this upward shift due to a decrease in resistance is "resistor pull-up." Fig. 3 shows how the curve shifts downward as we increase the resistance. Because the x-intercept remains the same, the curve does not shift in parallel.

It is important to familiarize yourself with the various graphical representations of the load line because we sometimes may simply read off the values by examining the x and the y intercepts. For example, in Fig. 2, if we assume V_a is zero, then we instantly find the value of V_{cc} and R numerically by examining the x-intercept and the y-intercept, respectively.

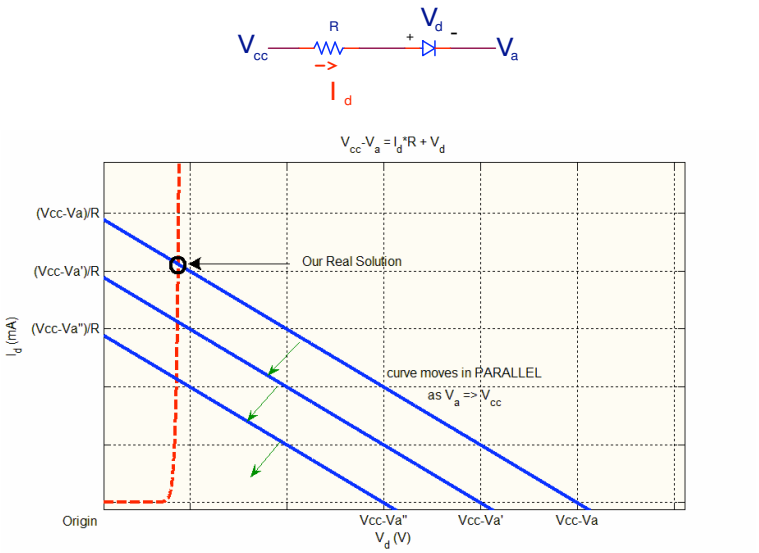


Fig. 2. The load line is shifted in parallel, indicated by the arrow, when the parameter V_a approaches V_{cc}, assuming that the resistance is kept at a constant value. The circuit for the particular load line is shown above.

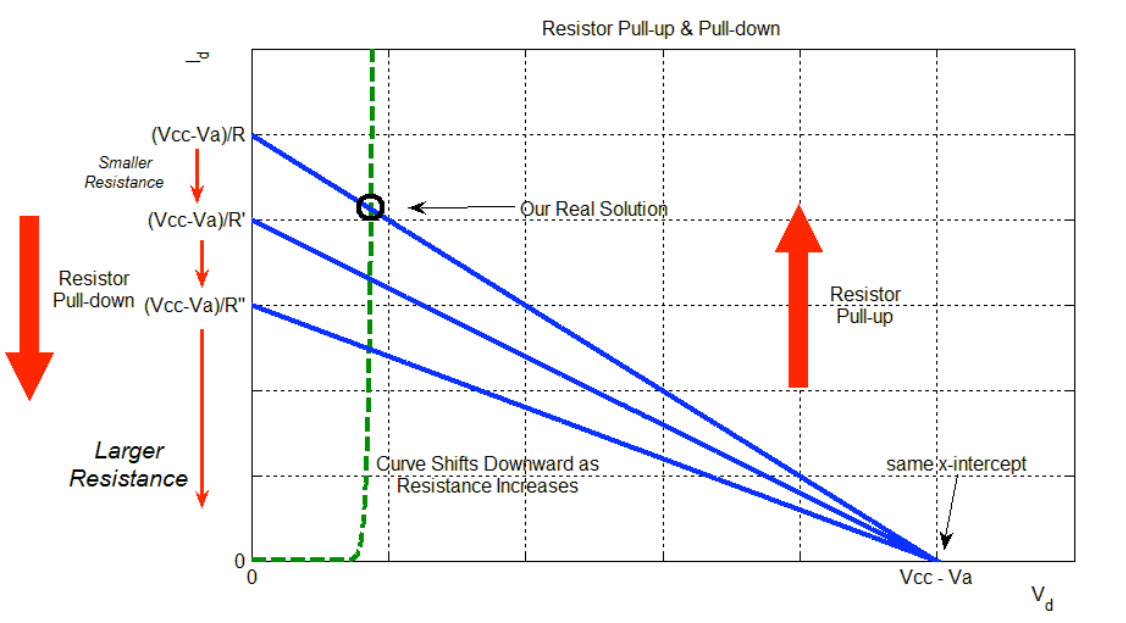


Fig. 3. The load line shifts as we vary the resistance, assuming Vcc and Va as constant. The curve does not shift in parallel because the x-intercept remains the same.

2.4 Zener Diodes

In a normal diode, the "activities" occurs in the first quadrant of the I-V characteristic. In Zener diode, the "activities" occurs in the third quadrant. In Zener diode, we assume that upon a certain negative voltage, named the breakdown voltage, the magnitude of the current increases dramatically. We are not so much interested in the positive voltage regime, but rather more in how the diode will behave in the realm of negative voltage. We still apply the same technique to obtain the load line equation from the circuit.

Example 10.3 in Hambley shows the graph of a Zener diode characteristic and its load line for two different supply voltages. The motivation for using a Zener diode rather than a regular diode is the high voltage switching applications. While a regular diode provides switching behavior, the voltage involved is fairly small. With Zerner diode, voltage switching occurs on the order of magnitude of 100 V. Moreover, a very small change in the voltage induces a large change in current; therefore, the resistance is very small by Ohm's Law, as the slope of the Zener diode characteristic is fairly large.

2.5 Applications for Diodes

The widespread applications for diode include, but are not limited, to the following:

- AND/OR gate
- Half & full wave rectifier
- Clamping circuit
- Clipper circuit
- Peak detector
- Level shift
- Voltage doubler

In the following section, I will discuss each application separately and briefly.

2.5.1 Clipper Circuit (a.k.a. Limiter Circuit)

To begin the analysis of clipper circuit, we present two basic forms. In each of the two forms, we will examine the transfer characteristic, namely the output voltage as a function of input voltage, and the output voltage as a function of time.

The first basic form is shown in Fig. 4. We will use the simple piecewise 0.7 model in our analysis.

If the input is less than 0.7 V, the diode is off, the output voltage will be equal to the input voltage because the diode is an open circuit. The slope of the transfer characteristic curve for input less or equal to 0.7 V will have a slope of 1. If the input is greater than 0.7V, the diode is on, the output will be clamped at 0.7 V. The difference voltage between the input and 0.7V will be "carried" by the series resistor, as there is now current flow in this case. Assuming the input is a sine wave with a magnitude of 1, the output waveform as a function of time is shown in Fig. 4(b). When the voltage exceeds 0.7 V, the output voltage is clipped off and remains at 0.7 V.

Exercise: Draw the transfer characteristics of the output vs. input voltage.

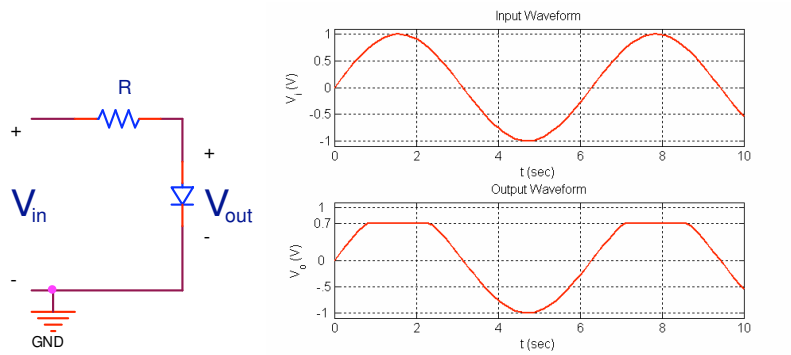


Fig. 4. 1st Clipper circuit using the simple piecewise 0.7 model. (a) The diode circuit representing a single limiter. (b) The plot of the input voltage and the resulting output voltage as a function of time.

If the orientation of the diode is switched, as shown in Fig. 5(a), the same analysis follows. If the input voltage is greater than -0.7V, the diode is an open circuit, and the output voltage is equivalent to the input voltage. On the other hand, if the input is less than -0.7 V, the diode is on and is a short circuit, thus output voltage is limited to be -0.7 V. Fig. 5(b) shows the output voltage as a function of time when input is a sine wave with 1V magnitude. When the input voltage falls below -0.7 V, the output voltage is clipped off and remains at -0.7 V.

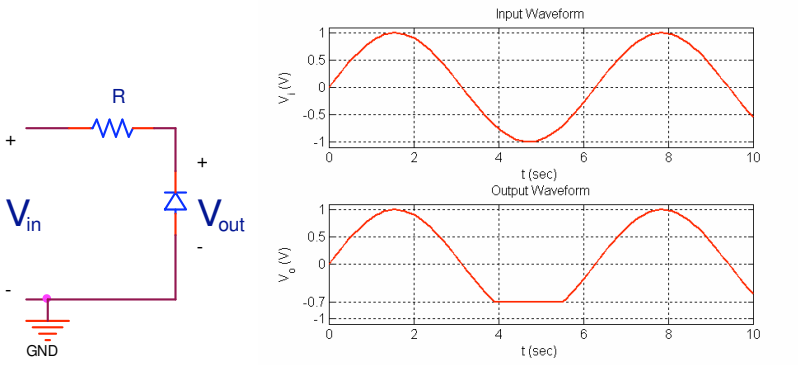


Fig. 5. Examination of behavior with diode orientation reversed, assuming the simple piecewise 0.7 model. (a) The diode circuit representing a single limiter. (b) The plot of the input voltage and the resulting output voltage as a function of time.

With the first canonical form, we have a limitation on the value the output becomes bounded, i.e., it is bounded by either 0.7 V or -0.7 V. We can change this value by adding a battery in series with the diode. We obtain our second canonical form by augmenting this battery, as in Fig. 6. The input needs to become (0.7 + battery voltage) Volts before the output voltage in the transfer characteristic flattens out. Furthermore, if the orientation of the battery is switched, the clipping will occur in the negative region.

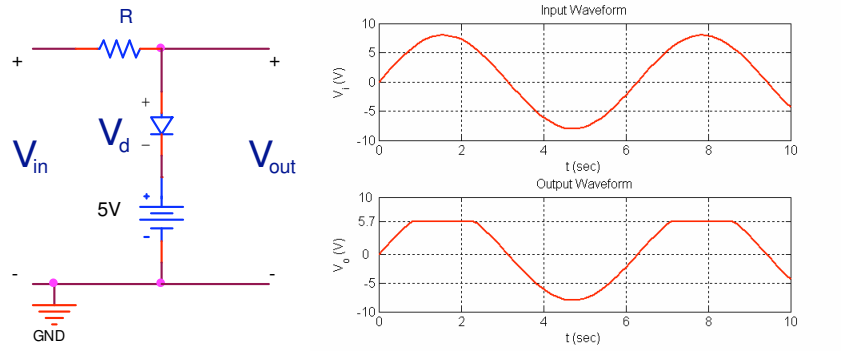


Fig. 6. The 2nd canonical form for analyzing clipper circuit, assuming the simple piecewise 0.7 model. (a) The new circuit with battery added in series with the diode. (b) The plot of the input voltage and the resulting output voltage as a function of time.

What we have examined is known formally as a single limiter, since the circuit will limit the output voltage on one side. By placing the two diodes with different orientation together in parallel, we obtain a circuit that bounds the output voltage on both sides. This double clipping action is more formally known as a double limiter. An example is shown in Fig. 7. The output voltage is both bounded below and above by 0.7 V and -0.7 V, respectively.

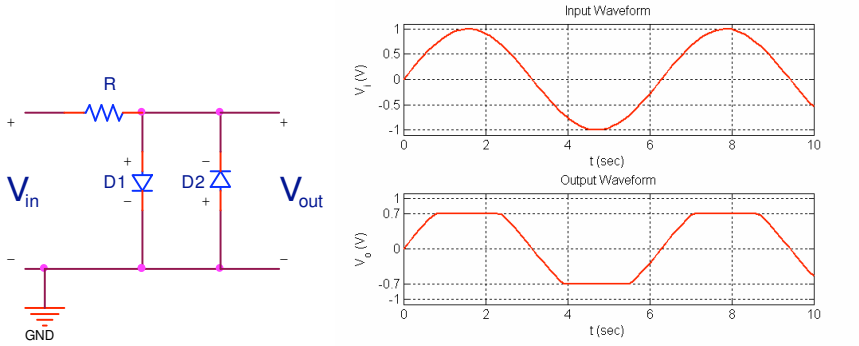


Fig. 7. A combination of two canonical forms in parallel, again assuming simple piecewise 0.7 model. (a) The double limiter circuit. (b) Plot of input voltage waveform and the resulting output voltage waveform.

Using the second canonical form, we can achieve a clipping at different voltages by placing different battery voltages. A classical example, used both in lecture and the textbook, is shown in Fig. 8. Knowing the canonical forms, we easily simplify the problem by examining each of the two parallel branches separately and superposing the two results.

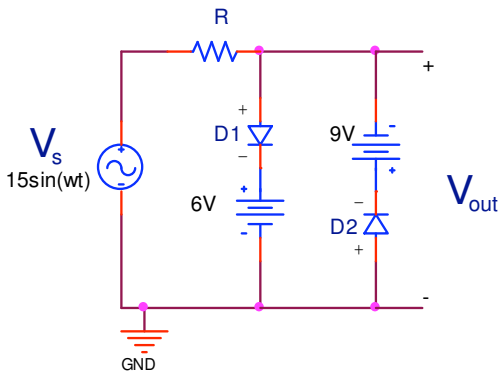


Fig. 8. Clipper circuit diagram.

2.5.2 Level Shift Circuit

A level shift circuit is composed of a capacitor in series with a diode. Note the orientation of the diode in relation to the output voltage and also note the polarity of the capacitor, as shown in Fig. 9. The intuition behind a level shift circuit is gained by considering the two cases with the diode on and off separately. We will use the ideal diode model. When the diode is turned on, we have a short circuit; hence the output voltage is zero. At this stage, the capacitor will get charged to an equal and opposite value as the input voltage. On the other hand, when the diode is turned off, the output voltage is given by KVL, $V_{out} = V_{cl} + V_{in}$.

Let's look at an example now. Consider a square wave as an input passed into the level shift circuit shown in Fig.10, with the positive peak at 4 V and negative peak at -6 V. Initially, when the square wave takes a negative value, the diode becomes a short circuit; hence the output voltage becomes zero. At this stage, the capacitor will get charged to become the negative of the input voltage; KVL shows us that $V_{in} = -V_{cl}$. Thus V_{cl}=6V here. When the input jumps to a positive value, the diode will be turned off, and $V_{out} = V_{cl} + V_{in} = 4 + 6 = 10$ V. When the input returns to -6V again, the diode is again a short circuit and $V_{out} = 0$. But in this case, the capacitor is already fully charged to 6V, there will be no longer current flow. The resulting waveform is shown in Fig. 10.

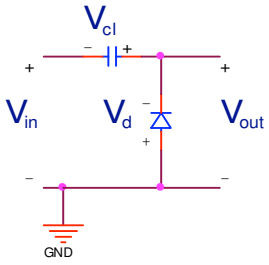


Fig. 9. The prototypical level shift circuit. Note the orientation of the diode and capacitor in relation to the input voltage.

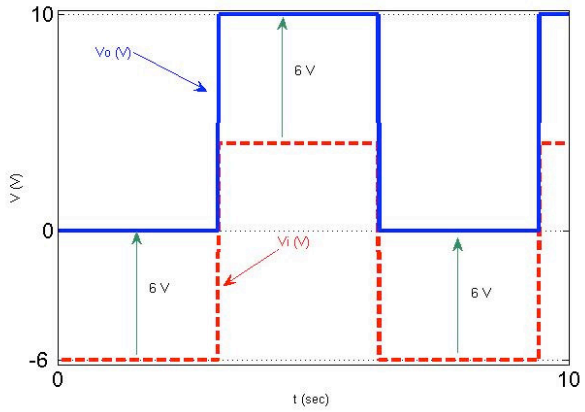


Fig. 10. The output voltage waveform, V_{out}, shown in solid lines, is obtained when the input voltage waveform, V_{in}, shown in dashed lines, is passed into the level shift circuit in Fig. 9. The resulting output waveform is shifted upward by 6 V.

If we switch the orientation of the diode (but still define all the polarities in the same way), the square wave will be shifted downward instead of being shifted upward. This new orientation is shown in Fig. 11. The polarity of the capacitor and output voltage remained the same. The only change is that the direction of the diode is reversed. The resulting waveform will then take the form as shown in Fig. 12.

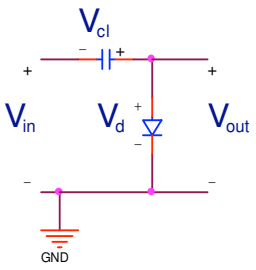


Fig. 11. Reversing the orientation of the diode while keeping the polarity the same.

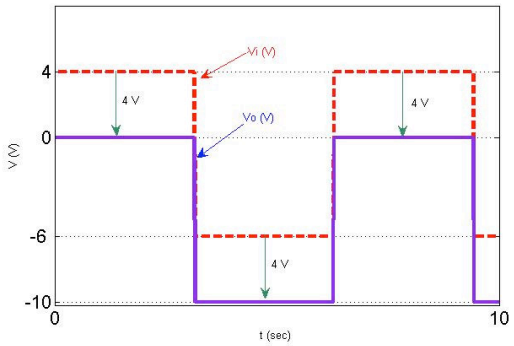


Fig 12. The output voltage waveform, V_{out}, shown in solid lines, is obtained when the input voltage waveform, V_{in}, shown in dashed lines, is passed into the level shift circuit in Fig. 10. The resulting output waveform is shifted downward by 4 V.

Exercise: Draw the diode current as a function of time.

2.5.3 Clamping Circuit (a.k.a. DC Restorer)

The level shift circuit shows that the square wave can be shifted upward and downward, depending on the orientation of the diode. In either case, the wave is bounded above or below by the threshold value of the diode. In other words, the peak or trough of the waveform is "clamped" at this particular threshold value of the diode. Because we assume the ideal diode model, the output waveform becomes bounded by 0 V. If we had assumed the simple piecewise 0.7 model, the output waveform would become bounded either below or above by 0.7 V. We can clamp the waveform by utilizing different diodes with different threshold value. However, we sometimes wish to clamp the waveform with a large range of possible voltage values. To accomplish this greater freedom, we add a battery in conjunction with the diode. Thus, it can be seen that clamping circuit is a more generalized class of a level shift circuit.

2.5.4 Rectifier Circuit

Rectifier circuits are divided into two classes – half-wave and full-wave rectifier. Consider a sinusoidal input signal $x(t)$ as given. Mathematically, a half-wave rectifier produces an output $y_1(t) = \frac{|x(t)| + x(t)}{2}$, while a full-wave rectifier produces an output $y_2(t) = |x(t)|$. These outputs, $y_1(t)$ and $y_2(t)$, represent a half wave and a full-wave rectified output, respectively, assuming the ideal diode model. An example showing the input and output waveform for a half-wave and a full-wave circuit is shown in Fig. 13. If we were mathematicians, our discussion of rectifier circuits would terminate here; however, as an engineer, we want to know how to construct circuits to produce the output signals $y_1(t)$ and $y_2(t)$ given an input signal $x(t)$.

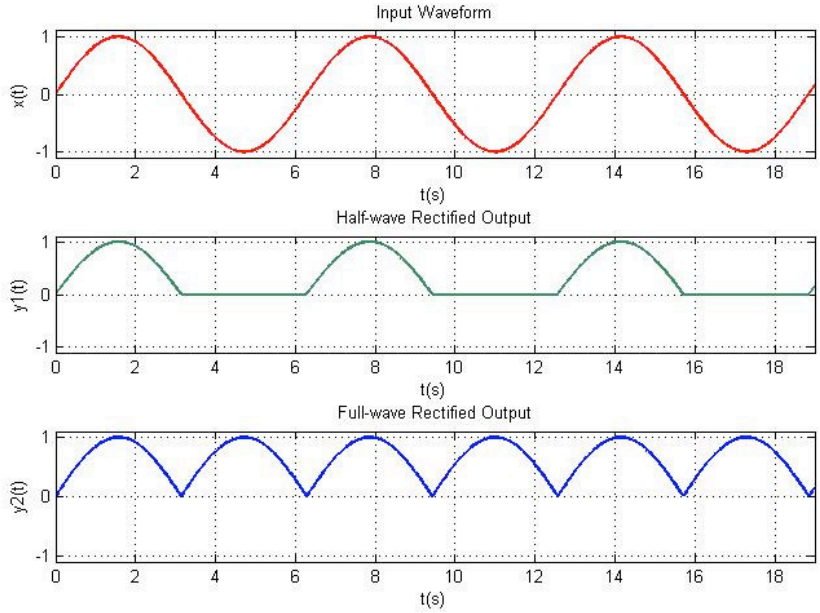
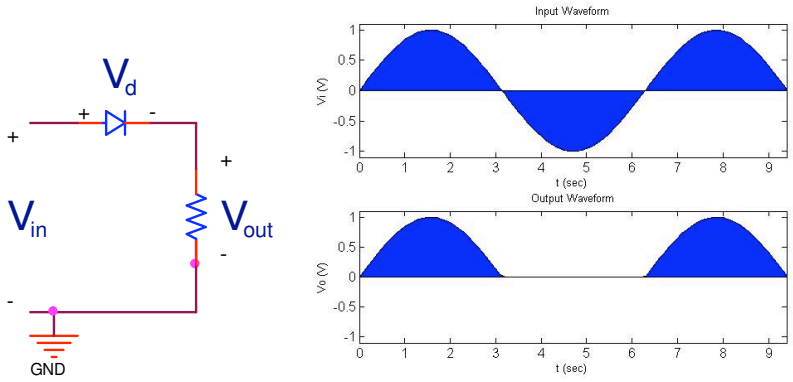


Fig. 13 Half-wave rectified and full-wave rectified signals. The topmost signal is the input signal which is fed into a half-wave rectifier to produce the middle output signal, and fed into a full wave rectifier to produce the bottom signal.

Half-Wave Rectifier

Fig. 14 shows the classical half-wave rectifier circuits. To analyze the output, we follow the input voltage and apply fundamental diode principles and KVL. When the input is positive, the diode behaves as a short circuit, thus the output voltage is given by $V_{out} = V_{in} - V_d$ (KVL). Assuming an ideal diode model, $V_{out} = V_{in}$. Assuming a simple piecewise 0.7 model, $V_{out} = V_{in} - 0.7$. When the input is negative, the diode is reverse biased and behaves as an open circuit. Thus, the output voltage is zero since no current flows in the closed loop.



(a) (b)

Fig. 14. (a) Half-wave rectifier circuit. (b) A sinusoidal input and the resulting output.

Now consider adding a 0.6 V battery to produce the circuit shown in Fig. 15. The ideal diode model is still assumed. The diode will be on only when the input is greater than the voltage across the battery, 0.6 V, since only then will the voltage across the diode be positive. ($V_d = V_{in} - 0.6$ V) The output voltage will be V_{in} - 0.6 (KVL). Whenever the input voltage falls below 0.6 V, the diode will be reverse biased. Thus, a zero current implies zero voltage.

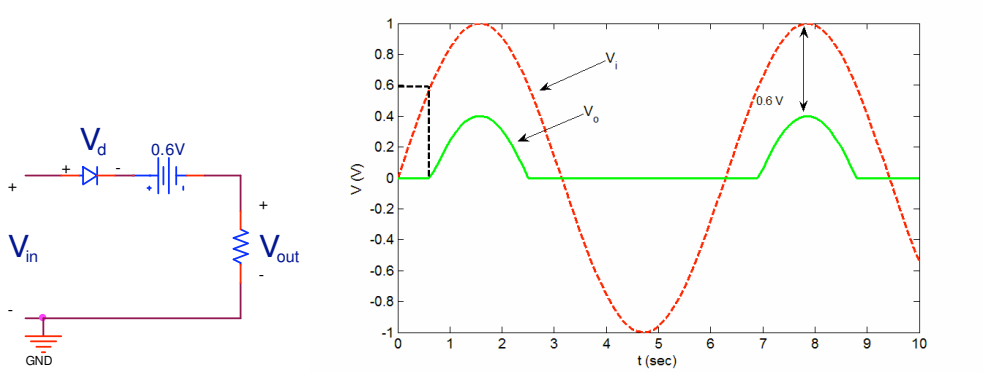


Fig. 15. Adding a 0.6 V battery to the circuit produces the corresponding output signal, shown in green from the input signal, shown in red. Ideal diode model is assumed here.

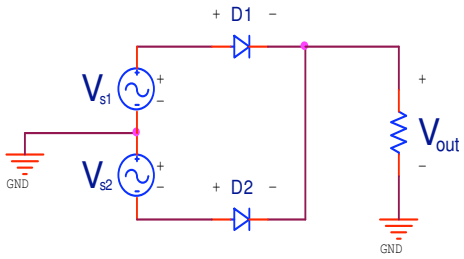
Full-Wave Rectifier

A full-wave rectifier can be constructed in two ways:

1. Using two AC sources and two diodes

2. Using a diode bridge

The first method composes of two sources which have π phase difference along with two diodes, as in Fig. 16. When V_{s1} is positive, V_{s2} is negative. Hence the top diode will be a short and the bottom diode will be an open. On the other hand, when V_{s1} is negative, V_{s2} is positive. Hence the bottom diode will be on and the top diode will be an open circuit. Therefore, we obtain the resulting waveform as shown in Fig. 13. In practice, a transformer can be used to provide the two out-of-phase voltage sources.



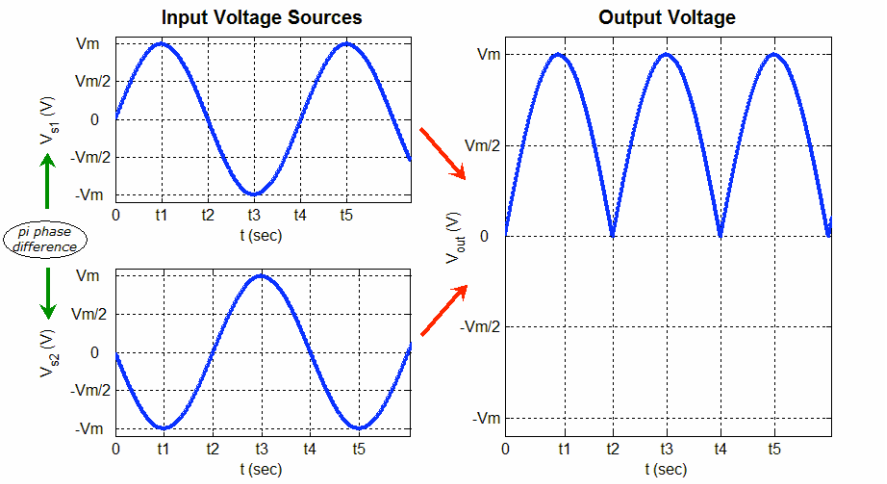


Fig. 16. A full-wave rectifier implemented using two AC sources and two diodes model. The two voltage sources are out of phase, as seen from the left plot.

A second way to construct a full-wave rectifier is to use a diode bridge. This configuration is used because sometimes it may be impractical to obtain two voltage sources. Fig 17 shows a diode bridge. The four diodes are aligned such that diode A and C orient in the same direction and diode B and D orient in the same direction. The output is taken across the load resistor. The negative lead of the resistor is essentially the ground that connects to the junction between B and C.

In the positive portion of the cycle, both diode A and C will be on and both diode B and D will be under reversed bias. The current will flow through diode A, the load resistor, the ground, and return through diode C. The direction of the current is shown by arrows in Fig. 18. Diode B and D is shaded to indicate that they are both under reverse bias and off.

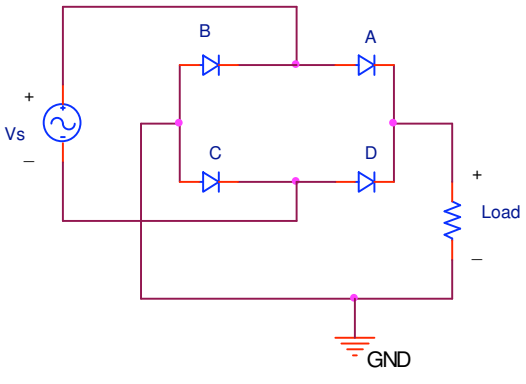


Fig. 17. A full-wave rectifier implemented using a diode bridge model.

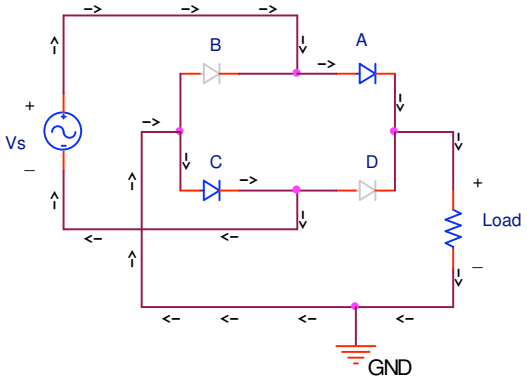


Fig. 18. The input is in the positive cycle. The arrows show the path of the current. Diode B and D, shown in gray, are both under reverse bias and therefore off.

In the negative portion of the cycle, the opposite occurs. Diode B and D will be on and diode A and C will be under reverse bias. The current flows through diode D, the load resistor, and returns through diode B. This scenario is shown in Fig. 19. Again, the shading of diode A and C indicate their reverse bias condition, and the arrows show the path of the current.

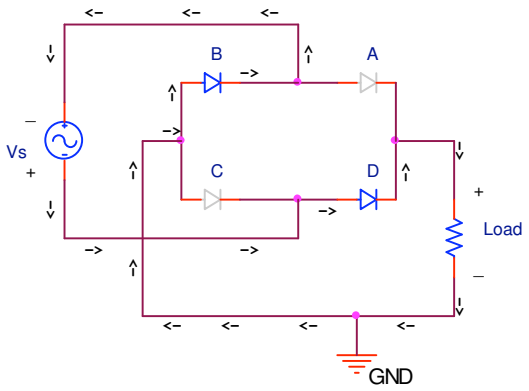


Fig. 19. The input is in the positive cycle. The arrows show the path of the current. Diode A and C, shown in gray, are both under reverse bias and therefore off.

In either case, current will flow through the load resistor from the marked positive lead toward negative. Therefore, the voltage measured across the load will always be positive, so we obtain a full-wave rectified version of the original sinusoid.

2.5.5 Peak Detector

Peak detectors have useful applications in converting an AC signals into DC signals. They also have extremely important applications in envelope detection.

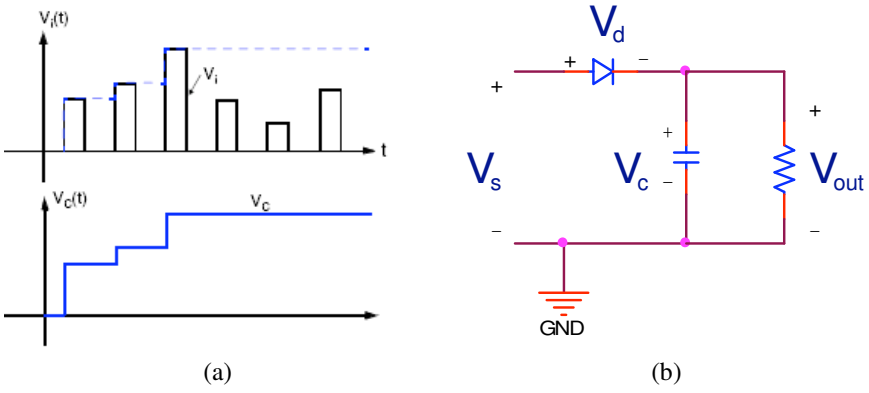


Fig. 20. Peak detection. (a) The top waveform is fed into a peak detector circuit to produce the bottom curve, assuming the capacitance is nearly infinite. (b) Peak detection circuit.

To construct a peak detector, we add a capacitor in parallel with the resistor in the existing configuration of a standard half wave rectifier. Assume the capacitor is initially uncharged. $V_d = V_s - V_c$. Initially, in the first quarter of a full period of a sine wave input, the diode will be a short circuit because the voltage across it will be positive, since $V_s > V_c$. The capacitor will get charged, thus the voltage across the capacitor will follow the input voltage.

When the input voltage reaches the peak of the sinusoidal curve, the input voltage will start to drop faster than the capacitor voltage, since we assume that the capacitor is fairly large (thus large time constant). When the input voltage drops faster than the capacitor voltage, $V_s < V_c$, $V_d < 0$, and diode is turned off. The output voltage follows the capacitor discharge (as Vout = Vc). The shape of this curve will depend on how large the capacitance is. If the capacitance is assumed infinity, the curve will be a flat line. As the capacitor continues to discharge, there will be a point in which it intersects the input curve. After this intersection, $V_s > V_c$, $V_d > 0$, diode will turn on again, and the capacitor follows the input curve as it gets charged up again.

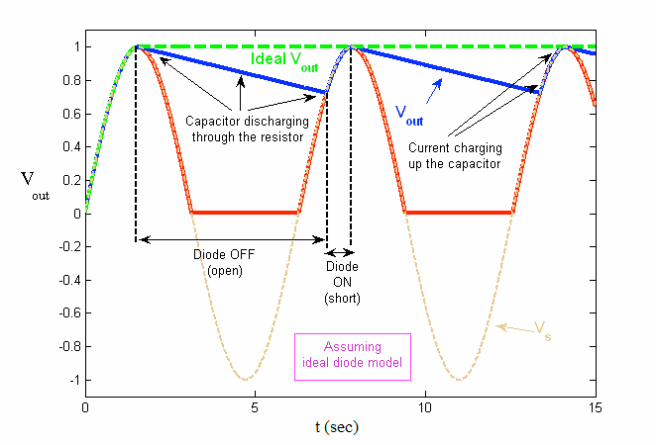


Fig. 21. The plot of the output voltage V_{out} versus the input voltage V_s, given the peak detector circuit in Fig. 19 and assuming the ideal diode model. The ideal voltage output is shown in thick dashed lines, when the capacitor is assumed to be nearly infinite.

How does adding a battery in series with the diode affect the behavior of the output? We can gain an intuitive understanding of a peak detector by considering the circuit first without the capacitor. In another word, the capacitor is nonexistent, and it is simply a short where the capacitor should be. In this case, the output with a battery will be a half wave rectified shifted downward by the voltage across the battery. Adding the capacitor will add a curve connecting from the peaks to a point on the rising portion of the peak.

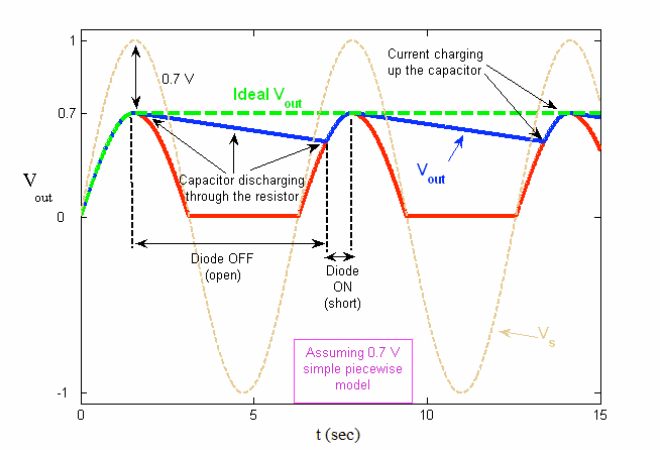


Fig. 22. The plot of the output voltage V_{out} versus the input voltage V_s, given the peak detector circuit in Fig. 19 and assuming the 0.7 simple piecewise model. The ideal voltage output is shown in thick dashed lines, when the capacitor is assumed to be nearly infinite.

2.5.6 Voltage Doubler Circuit

A voltage doubler is composed of a level shift circuit and a peak detector circuit in a cascade composition. In a sense, the level shift circuits will already double the input voltage. However, we use a peak detector to convert this AC signal into a DC signal. Fig. 23 shows such cascade composition. The output of the level shift circuit on the left is passed as an input to the peak detector circuit on the right.

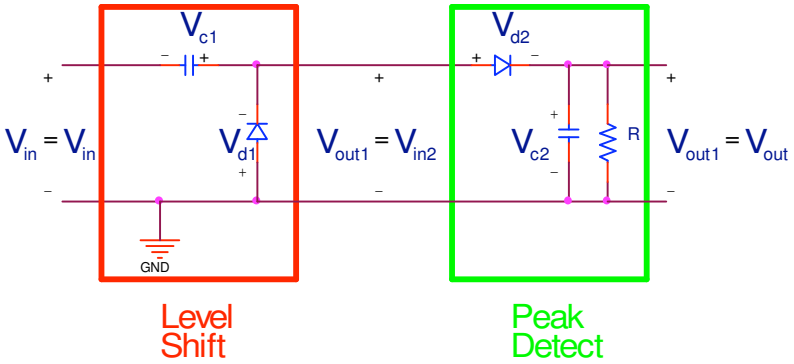


Fig. 23. Voltage doubler circuit. A cascade composition of the level shift circuit with the peak detector. The output of the level shift circuit on the left is passed in as the input to the peak detector circuit on the right.

An example is shown below in Fig. 24. The input voltage waveform, indicated by dash lines, is passed into the circuit. After passing through the level shift circuit, a shifted version of the original waveform is formed. This new waveform is passed as an input to the peak detector circuit. The peak detector detects the peak of the new waveform, resulting in the final line indicated by 'peak detect.'

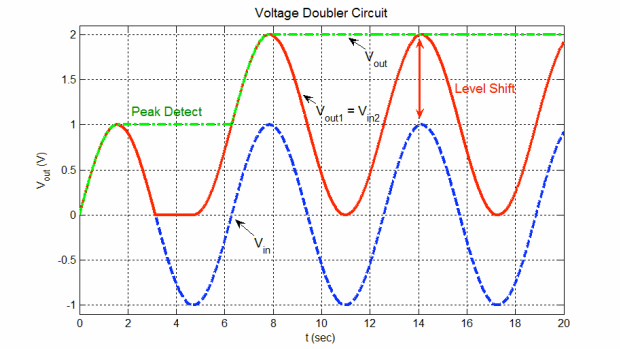


Fig. 24 A plot of the input voltage V_{in}, the intermediate voltage V_{out1} or V_{in2}, and the final voltage output V_{out}. After the initial waveform, indicated in dash, is shifted upward, the peak detector detects the peak to obtain the final output voltage.

2.5.7 Diode Logic Gates

The two fundamental logic gates, AND and OR, can be implemented using diodes, as shown in Fig. 25. In an AND gate (Fig. 25(a)), the cathodes of the diodes are connected to a resistor that connects to a positive voltage source. The output is measured at point Z, the cathode of two diodes. In an OR gate (Fig. 25(b)), the anodes of the diodes are connected to a resistor that connects to ground, and the output is taken at point Z, the anode the two diodes.

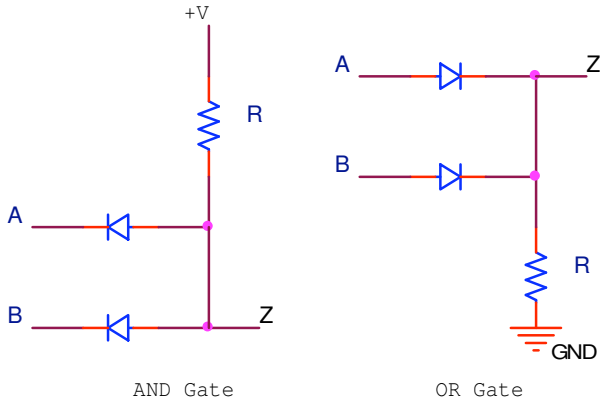


Fig. 25. Diode logic gates. Z represents the output, given A and B as inputs. (a) AND gate. (b) OR gate.

AND Gate

AND gate is shown in Fig. 25(a). If either input A or B is low, the diode will conduct, resulting in a short circuit thus a low output Z. Only when both the inputs to A and B are high will neither of the diode conduct. The diode will behave as open circuits resulting in a high output Z. These conditions are shown in Table 1, which presents the truth table for the AND gate.

Table 1. The truth table for the AND gate shown in Fig. 24(a).

A	**B**	**Z**
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

OR gate is shown in Fig. 25(b). If both of the input to A and B is low, the diode will be off because the voltage across the diode is zero, hence no current flows. The output will therefore be pulled down to zero. If either of the input is high, the diode will conduct, as current flows from the higher potential to a lower potential. The output voltage at point Z will hence be a positive, high voltage, which is equal to the voltage across the resistor. Table 2 below presents the truth table for the OR gate. We can see from the table that the output is high when either one of the inputs A or B is high.

Table 2. The truth table for the OR gate shown in Fig. 24(b).

A	**B**	**Z**
0	0	0
0	1	1

1	0	1
1	1	1

Chapter 3. Semiconductor Physics

3.1 Introduction to Silicon

Almost all semiconductors used in integrated circuit (IC) technology are single crystalline Silicon (Si) material. Si is element 14, in Group IV, with an electronic configuration of $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$. From this electronic configuration, we can see that Si has 4 valence electrons in the n = 3 energy level. A silicon crystal is tetrahedrally arranged in a diamond cubic unit cell, in which the valence orbital are sp^3 hybridized.

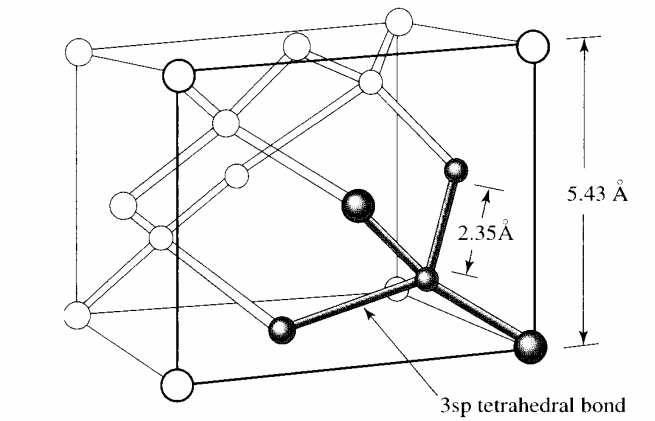


Fig. 1. Unit cell of crystalline silicon.

The atomic density of crystalline silicon can be calculated from its unit cell, shown in Fig. 1, by observing that there are 8 atoms in corners, each having 1/8 of the atom lie within the unit cell. There are 6 atoms on the faces of the cube, with 1/2 the atom inside the unit cell, and 4 more atoms completely inside the unit cell. Thus, the atomic density of silicon can be calculated, given the size of the unit cell, with length a_0 on each side:

$$\frac{\#\ Atoms}{Volume} = \frac{8\times 1/8 + 6\times 1/2 + 4}{a_0^3} = \frac{8}{(5.43\times 10^{-8}\,cm)^3} = 5.00\times 10^{22}\,cm^{-3}$$

A common representation of the silicon crystal structure is given in Fig. 2. Each black line denotes a single bond, involving 2 electrons. Note that this does not represent a planar description of the crystalline structure of Si. Rather, this diagram demonstrates the bonding between each silicon atom and its 4 closest neighbors.

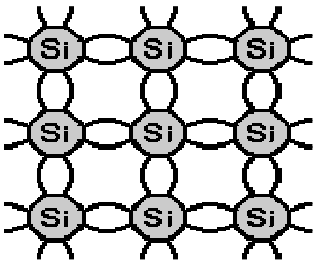


Fig. 2. Silicon bonding model.

3.1.1 Bandgap Energy

Conduction occurs in a substance through the flow of electrons (negative charge) and holes, or the lack of an electron (positive charge). The arrangement of atoms bonded together produces for its electrons many energy levels that are so close to each other that we may regard them as energy bands. Electrons are mobile in the high energy conduction band, while holes are mobile in the lower energy valence band. To form electron-hole pairs, electrons must have sufficient energy to overcome the bandgap energy, which is a region with no allowed energy levels. The excited electrons move from the valence band into the conduction band, leaving holes in the valence band. (See Fig. 3). Situations like this may occur when the crystal is illuminated with light or photons whose energy is larger than the bandgap energy, or when the crystal is sufficiently heated.

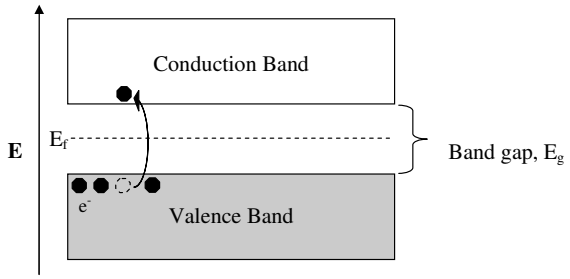


Fig. 3. Energy band diagram of semiconductors.

Insulators have a large band gap, usually 3.5 electron-volts (eV) or greater, preventing substantial amounts of charge carriers from flowing. Metals are good conductors, with electrons filling up into the conduction band. This means electrons are inherently mobile through a crystal, with thermal excitation producing even more electron-hole pairs. Semiconductors are in between, with band gaps ranging from 0.5 - 3.0 eV, allowing the easy excitation of electrons into the conduction band. However, it is the intermediate conductivity of semiconductors that is important for the electronics industry, along with their great flexibility in conductivity through doping.

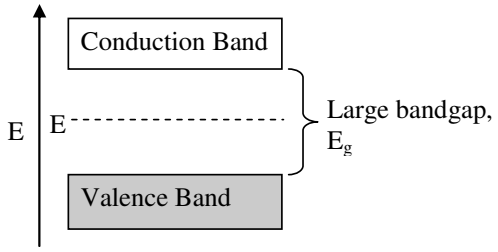


Fig. 4(a). Band diagram of an insulator.

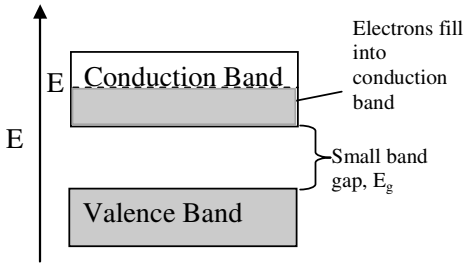


Fig. 4(b). Band diagram of a metal.

3.1.2 Fermi Energy

The Fermi-Dirac function provides the probability that an energy level is occupied by a fermion which is under thermal equilibrium. Electrons as well as holes are Fermions and hence obey Fermi-Dirac statistics. (A hole is simply "the lack" of an electron.) As electrons are added to an energy band, they will fill the available states in an energy band just like water fills a bucket. The states with the lowest energy are filled first, followed by the next higher ones. At the Fermi level, the probability of filling the state is exact 50%. The transition between completely filled states and completely empty states is gradual rather than abrupt, and the transition depends on temperature. The Fermi function which describes this behavior, which is given by:

$$f(E,T) = \frac{1}{1+e^{(E-E_f)/kT}} \tag{1}$$

where k is the Boltzmann constant, E_f is the Fermi energy, E is the energy of concern and T is the temperature at which the material is kept.

Figs. 4(a) and (b) show the position of the Fermi level in an insulator and a metal, respectively. Fig. 5 shows the Fermi function plotted with the energy bands at different temperatures. The x-axis, $f(E)$, is the probability that an energy level is occupied. The lowest energy levels are almost always occupied, with a probability of 1, and the highest levels have a probability of nearly 0, but this probability increases with higher temperature. To be more precise, the sharp edge of Fermi function is smeared out due to the increase in temperature.

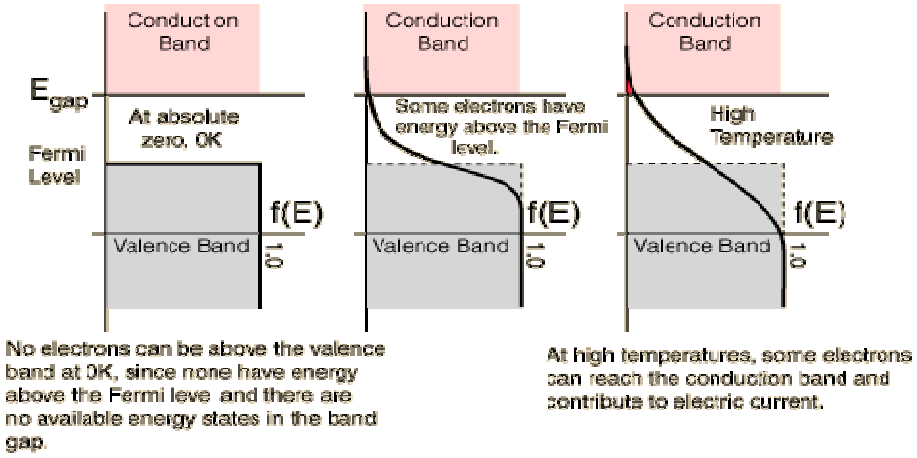


Fig. 5. Fermi function plots at absolute zero, mid-range, and high temperature.

For a given piece of semiconductor at a particular location (space coordinate) under thermal equilibrium, there is *only one Fermi level* for both the conduction and valence band, as it describes one equilibrium system.

For a semiconductor where $E_v < E_f < E_c$, we can derive the electron density, n and hole density, p, which are the density of states multiplied with Fermi probability function.

$$n = N_c \frac{1}{1+e^{(E_c-E_f)/kT}} \sim N_c e^{(E_f-E_c)/kT}$$

$$p = N_v \left[1 - \frac{1}{1+e^{(E_v-E_f)/kT}}\right] \sim N_v e^{(E_v-E_f)/kT}$$

$$np = N_c e^{(E_{f,i}-E_c)/kT} N_v e^{(E_v-E_{f,i})/kT} = N_c N_v e^{(E_v-E_c)/kT} = N_c N_v e^{-E_g/kT}$$

Here, N_c and N_v *are* the effective density of states in the *conduction* and valence band, respectively, and E_g is the bandgap energy. All three are constants for Si at a given temperature. This property is referred to as the *mass action law*

For an intrinsic (undoped) Si, the electron density n_i equals to the hole density, p, which is thus:

$$n_i = p_i$$

$$n_i p_i = n_i^2$$

$$n_i = \sqrt{N_c N_v} e^{-E_g/kT}$$

3.1.3 Doping

Doping a semiconductor refers to the careful addition of impurity atoms into the semiconductor. A doped semiconductor is considered extrinsic, and has enhanced conductivity due to additional charge carriers from the dopant atoms. The two categories of dopants are n-type, with excess electrons producing donor energy levels near the conduction band, and p-type, with holes (lack of electrons) producing acceptor energy levels just above the valence band. The two types of doped semiconductors are named for their majority charge carriers (the leading contributors to conduction in a material): n-type's majority charge carrier is electron (negative charge), while p-type's is hole (positive charge).

N-type dopants are typically group V elements, such as Phosphorus (P) and Arsenic (As), with five valence electrons. When a group V element is incorporated into Si and, in fact, replaces a Si atom in a lattice, it provides four of its outermost electrons to form covalent bonds with the surrounding Si atoms. However, there is an extra electron remaining, loosely orbiting the dopant atom, at a large radius, or high energy, as shown in Fig. 6(a). Thus, the extra electron form the donor electron that are close and easily excitable to the conduction band.

Typically, we may consider the electron density $n = N_d$, where N_d is the n-doping density, which can be seen as an increased Fermi energy level, shifting it closer to the conduction band compared to an undoped semiconductor at the same temperature. (See Fig. 6(b).) We can calculate the Fermi level relative to the conduction band edge and the hole density using the following equations.

$$\boxed{\begin{aligned} n &= N_d = N_c e^{(E_f - E_c)/kT} \\ p &= n_i^2 / N_d \end{aligned}}$$

P-type dopants are typically Group III elements, such as Boron (B) and Gallium (Ga), with three valence electrons. Of the four covalent bonds with surrounding Si atoms in the crystal lattice, only three are filled with an electron from the dopant atom. This vacancy creates an acceptor energy level just above the top of the valence band, for surrounding electrons to fill with ease. An electron that fills this hole propagates the vacancy to a Si atom, which is now missing an electron and positively charged. In this manner, the hole represents a region of positive charge, and is mobile just as an electron is, as shown in Fig. 7(a).

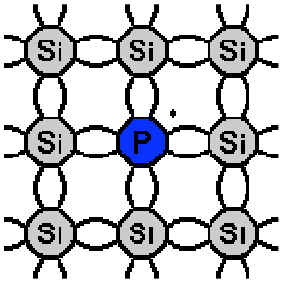


Fig. 6(a). Bonding model of n-type dopant (donor).

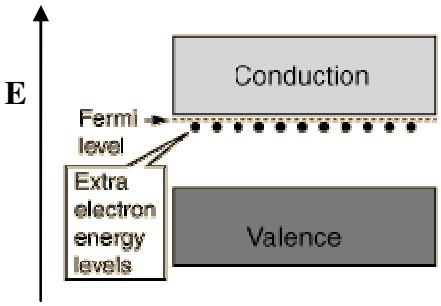


Fig. 6(b). Band diagram of n-doped semiconductor.

The presence of holes shifts the effective Fermi level downwards. This means less electrons will be found in the conduction band (while more holes can be found in the valence band) than in an intrinsic semiconductor, and the positively charged holes serve as the majority charge carrier. Fig. 7(b) shows the energy band diagram, where electrons can easily occupy the low energy acceptor levels provided by the p-dopants. In this case, we will have:

$$p = N_A = N_v e^{(E_v - E_f)/kT}$$
$$n = n_i^2 / N_A$$

It is amazing to see that a tiny amount of dopant is enough to achieve a great effect. For instance, typical doping concentrations are 10^{16} – 10^{19} cm^{-3}, but compared to the 5.0×10^{22} cm^{-3} density of Si atoms, a 10^{18} doping concentration means a 1:50,000 ratio of dopant atoms to Si atoms.

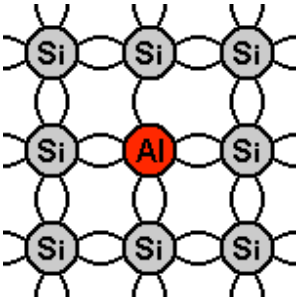


Figure 7(a). Bonding model of p-type dopant (acceptor).

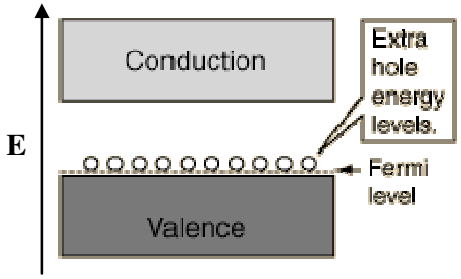


Figure 7(b). Band diagram of p-doped semiconductor.

3.1.4 Doping Methods

A common method of doping is diffusion. When a silicon crystal is exposed to high temperature dopants (gas phase), dopant atoms will diffuse against a concentration gradient into the silicon, where its concentration is much lower. Fig. 8(a) illustrates the process, where an oxide (SiO_2) shields the silicon from the dopant. Fig. 8(b) plots the doping concentrations along the material, as a cutout from Fig. 8(a).

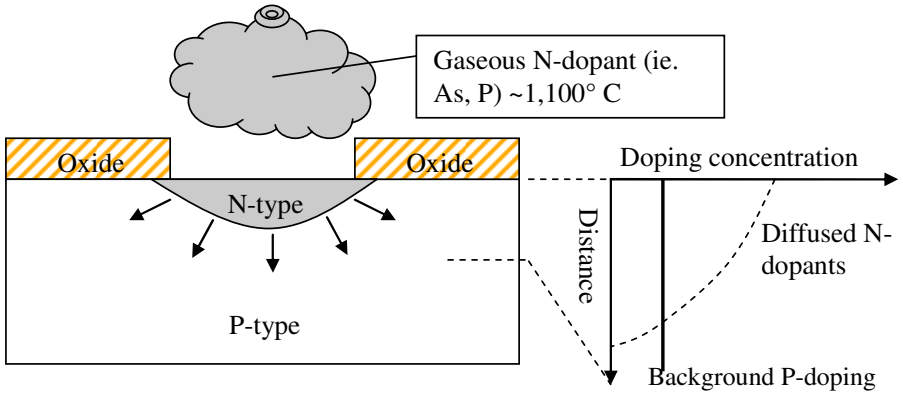


Fig. 8(a). Doping through diffusion of n-dopants into p-type silicon.

Fig. 8(b). Doping profile of the upper region of silicon in Fig. 8(a).

An alternative method to the high-temperature diffusion is ion implantation. Dopant ions are accelerated to high speed, and directed in a beam towards the silicon. This process allows more control of doping distribution than diffusion, because the penetration depth of the ions is directly correlated to their kinetic energy. Fig. 9(a) illustrates ion implantation, again in which an oxide shields areas to remain undoped. Fig. 9(b) shows the doping profile of the sample in Fig. 9 (a) after ion implantation.

Ion implantation allows silicon to be doped at lower temperatures than diffusion. However, the silicon crystal is damaged by the penetrating dopant atoms. Fortunately, a thermal treatment, annealing, of the silicon can remove most of the damage.

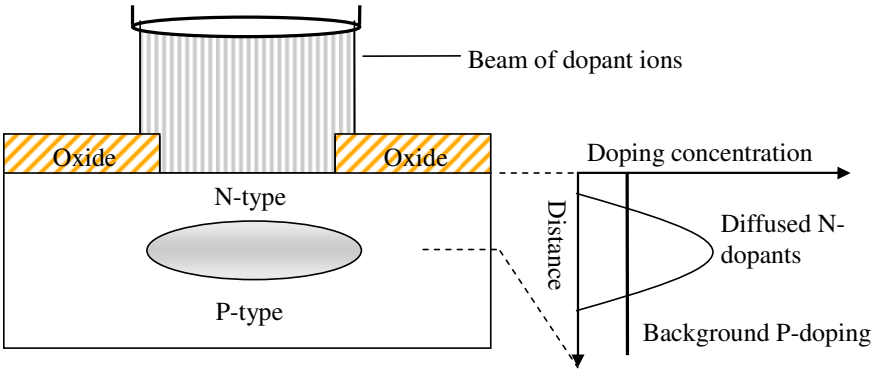


Fig. 9(a). Doping through ion implantation of N-dopants into P-type silicon.

Fig. 9(b). Doping profile of the upper region of silicon in Fig. 9(a).

3.2 Quantitative Analysis

3.2.1 Electric Fields

Gauss's law relates the electric field, $\vec{E}$, and charge. In differential form, Gauss's law is:

$$\nabla \cdot \vec{E} = \frac{\rho}{\varepsilon} \qquad (1)$$

The divergence of the electric field from a point is equal to the volume charge density, ρ (units of Coulombs / cm^3), divided by the electric permittivity, ε (units of Farads / cm). Thus, the units of electric field, $\vec{E}$, are Volts / cm. The permittivity measures a material's ability to polarize in response to an electric field, and consequently cancel out the field. The permittivity of free space, ε_0, is about 8.85×10^{-14} F/cm, while the permittivity of silicon is around $11.7\,\varepsilon_0$.

In integral form, Gauss's law is:

$$\oint_S \vec{E} \cdot d\vec{A} = \frac{1}{\varepsilon} \oint_V \rho \cdot dV = \frac{Q_{encl}}{\varepsilon}$$

The surface integral of electric flux is equal to the charge, Q (Coulombs), enclosed by the surface, divided by the electric permittivity.

In our study of semiconductors, we usually need only the 1-dimensional version of Gauss's law:

Differential form:

$$\boxed{\frac{dE}{dx} = \frac{\rho}{\varepsilon}} \qquad (2)$$

Integral form:

$$\int_{x_a}^{x_b} d[\varepsilon E(x)] = \varepsilon_b E(x_b) - \varepsilon_a E(x_a)$$

$$= \int_{x_a}^{x_b} \rho(x)\,dx = Q_{encl}\Big|_{x_a}^{x_b} \qquad (3)$$

where Q_{encl} is the charge enclosed between x_a and x_b. The permittivity, ε, may differ throughout a material, so it is included inside the differential, along with the electric field, $E(x)$. ε_a is the permittivity at x_a, and likewise for ε_b. We can find the electric field at a point b, by selecting a boundary point a that contains zero charge density. The electric field at the boundary location, $E(x_a)$ would then be 0.

3.2.2 Electrostatic Potential

Poisson's Equation relates electrostatic potential, ϕ, to the electric field, $\vec{E}$, and to charge density, ρ. The units of potential are Joules / Coulomb, or Volts.

In differential form, it is:

$$\nabla^2\phi = -\nabla \cdot \vec{E} = -\frac{\rho}{\varepsilon}$$

As before, we only need the one dimensional version in our analysis of semiconductors:

$$\boxed{\frac{d^2\phi(x)}{dx^2} = -\frac{dE(x)}{dx} = -\frac{\rho(x)}{\varepsilon}} \qquad (4)$$

By definition, the electrostatic potential $\phi(x)$ is found with respect to an arbitrary value at a reference point x_0 as the integral of the negative of the electric field E from x_0 to x:

$$\boxed{\phi(x) - \phi(x_0) = \int_{x_0}^{x} -E(x)dx} \qquad (5)$$

Like any potential function, only the potential difference (voltage) between two points is physically meaningful, since any constant can be added to ϕ without affecting $\vec{E}$. Thus, the usual value chosen for the potential at the reference point, x_0, is $\phi(x_0) = 0$.

3.3 PN Junction

A PN junction is formed when p-type material is in contact with an n-type material. This device allows considerable current to flow in only one direction (forward bias), while basically preventing current from flowing in the opposite direction (reverse bias) as shown in Fig. 14. Note that this semiconductor is a single crystal, in which one region is doped with acceptor impurity atoms (P-region), and the adjacent region is doped with donor atoms (N-region). For simplicity, we will consider a step junction where the doping concentration is uniform in each region, and there is an abrupt change in doping at the junction (see Fig. 15). Doping concentrations N_a in the P-region and N_d in the N-region are in units of cm^{-3}, denoting 1 impurity atom / cm^3.

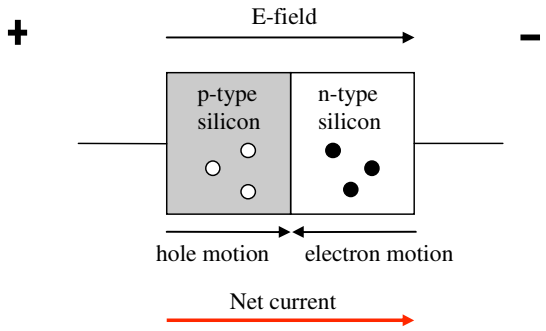


Fig. 14. PN junction with applied electric potential (forward bias).

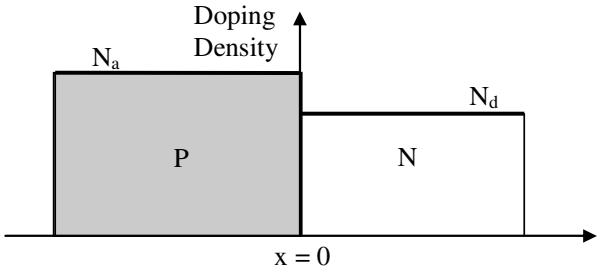


Fig. 15. Doping profile of a PN junction.

3.3.1 Depletion Approximation

The behavior of the PN junction can be understood by analyzing the physics of the diode as modeled in Fig. 16. Initially at the junction, there is a very large concentration gradient in the electron and hole concentrations. Majority carrier electrons in the N-region will begin diffusing into the p-region and majority carrier holes in the P-region will begin diffusing into the N-region. **Even though a doped semiconductor has excess electrons and holes, it is electrically neutral.** However, as electrons diffuse from the N-region, positively charged donor atoms are left behind (see Fig. 16). Likewise, holes diffusing from the P-region will leave negatively charged acceptor atoms.

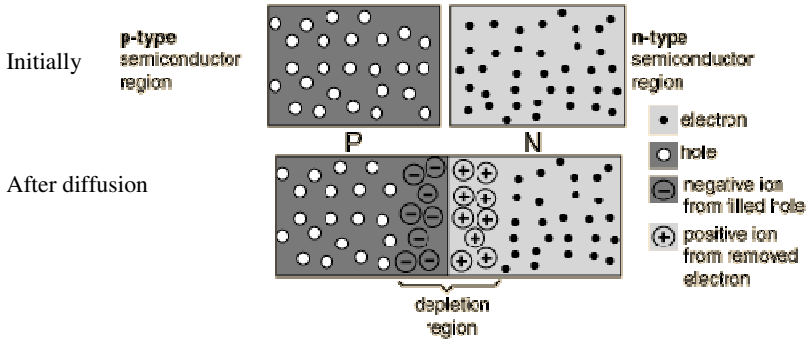


Fig. 16. Formation of the depletion region due to mobile charge carrier diffusion in a PN junction.

The dopant atoms, now ionized, are immobile because they are fixed in the crystal by their covalent bonds with surrounding silicon atoms. The regions on both sides of the junction are now depleted of mobile charge carriers, because the mobile carriers (electrons and holes) have diffused to the other side. The N-side is now positively charged with ionized donors near the junction, and the P-side is negatively charged with ionized acceptors, due to the ionized dopants. We call this the depletion region, which on either side, is depleted of mobile charge carriers and has a constant charge density due to the constant doping

concentration. The presence of immobile ions, as illustrated in Fig. 16, generates a built-in electric field pointing from N-side to the P-side within the depletion region. This built-in field will prevent mobile charge diffusion across the junction and balance the carrier motion in a PN junction under thermal equilibrium.

The portions of the semiconductor outside the depletion region are electrically neutral, due to the balance of charge carriers and dopant atoms. Reference 1 present a good quantitative treatment of the depletion approximation, in which we assume:

$$\rho_0(x) \approx \begin{cases} -qN_a & (-x_{p0} \le x \le 0) \\ qN_d & (0 \le x \le x_{n0}) \end{cases} \quad \text{and} \quad \rho_0(x) = 0 \quad (x < -x_{p0},\ x > x_{n0}) \qquad (10)$$

The charge distribution above in equation (10) describes the depletion region of a PN junction with the P-side between $x = -x_{po}$ and $x = 0$, while the N-side is between $x = 0$ and $x = x_{no}$. The P-side has a doping concentration of N_a, and its acceptor dopants ionize to negatively charged atoms, so the charge density, ρ_o, of this side is $-qN_a$. Likewise, the N-side has a doping concentration of N_d, with positively charged donor ions, giving a charge density, ρ_o, of qN_d. Keep in mind that the PN junction actually extends past $-x_{po}$ and x_{no}, but this bulk silicon outside the depletion region is neutrally charged, so $\rho_o = 0$ in the regions where $x<-x_{po}$ and $x>x_{no}$.

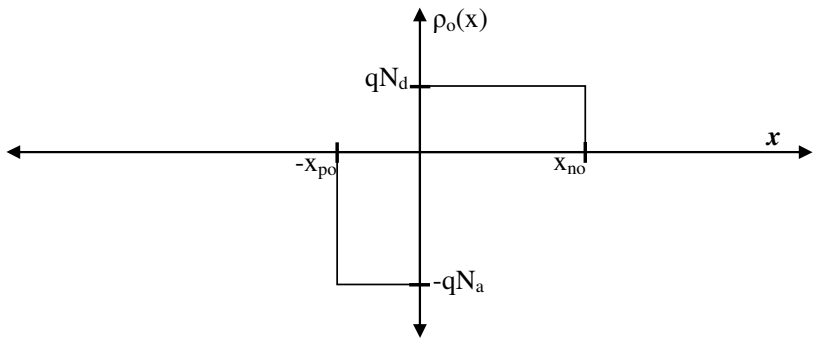


Fig. 17. Charge distribution, $\boldsymbol{\rho_o(x)}$, of the PN junction, with depletion region as approximated in Equation (10).

3.3.1.1 Finding the electric field

The subscript 0 for the charge density $\rho_o(x)$ indicates that our PN junction is in thermal equilibrium. We now integrate the charge density to find the electric field $E_o(x)$ and then integrate again to find the electrostatic potential $\phi_o(x)$. Gauss's Law relates the charge density to the derivative of the electric field:

$$\frac{dE_0}{dx} = \frac{\rho_0(x)}{\varepsilon_s} \qquad (11)$$

where $\varepsilon_s = 11.7\,\varepsilon_0$ is the electric permittivity of silicon.

The PN junction in thermal equilibrium has no net current flow. In the formation of the depletion region, the total negative charge on the P-side is equal and opposite to the positive charge on the N-side, because an equal number of holes from the p-side and electrons from the n-side diffused and recombined at the interface. Thus, differing doping concentrations N_a and N_d will result in regions of different width, but the net charge on either side is the same:

$$qN_a x_{po} = qN_d x_{no} \qquad (12)$$

This fact means that the electric field at the boundaries $-x_{po}$ and x_{no} is 0, because the net enclosed charge in the depletion region is 0 (Gauss's Law states that if a surface encloses no net charge, there is no electric

flux through the surface). Also important, the adjacent bulk silicon outside the depletion region is neutrally charged.

On the P-side of the depletion region $-x_{po}<x<0$, we integrate the charge distribution of equation (10) to obtain the electric field:

$$E_0(x) = \int_{-x_{po}}^{x} \frac{\rho_0(x)}{\varepsilon_s} dx + E_0(-x_{po}) = \frac{-qN_a}{\varepsilon_s}(x-(-x_{po})) + 0$$

where our constant of integration, $E_o(-x_{po})$, is 0, because at the edge of the depletion region, the electric field is 0. This is because there is no charge density on the left side (bulk p-silicon). Therefore,

$$E_0(x) = \frac{-qN_a}{\varepsilon_s}(x + x_{po}) \qquad (-x_{po} < x < 0) \tag{13}$$

In the N-region, the electric field can be found by noting that at the boundary of the depletion region with the bulk n-silicon, x_{no}, the electric field, $E_o(x_{no})$, is the sum of the electric field, $E_o(x)$, at the point x, and the contribution due to the charge between x and x_{no}, found by Gauss's law:

$$E_0(x_{no}) = E_0(x) + \int_{x}^{x_{no}} \frac{\rho_0(x)}{\varepsilon_s} dx = 0$$

$E_o(x_{no})$ is also 0, because by Gauss's law, the entire depletion region has 0 net charge, so the electric flux must be 0 at its boundaries. Rearranging the above expression, we can find the electric field in the N-side of the depletion region:

$$E_0(x) = \int_{x}^{x_{no}} \frac{\rho_0(x)}{\varepsilon_s} dx \; - E_0(x_{no}) \; = \; \frac{-qN_d}{\varepsilon_s}(x_{no} - x) - 0 =$$

$$E_0(x) \; = \; \frac{qN_d}{\varepsilon_s}(x - x_{no}) \qquad (0 < x < x_{no}) \tag{14}$$

The electric field of our PN junction in thermal equilibrium, as described by Eqns. (13) and (14) is shown in Fig. 18.

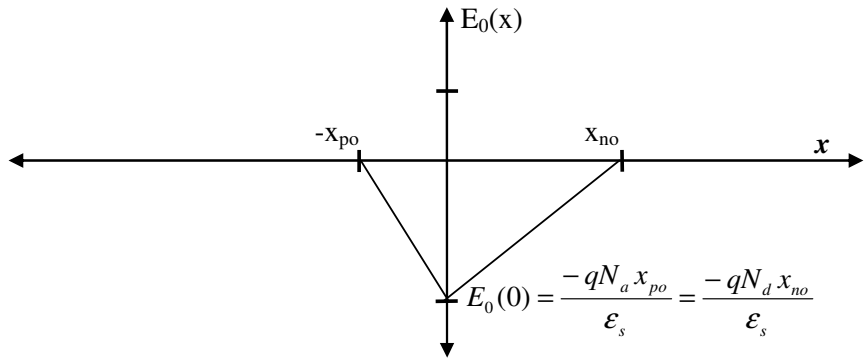


Fig. 18. Electric Field, ***E(x)***, of the PN junction, with depletion region as approximated in Equation (10).

Note that the field is continuous, because we have considered two regions of finite charge density, and there is no sheet charge anywhere. At the interface, $x = 0$, the electric field reaches its maximum magnitude. Substituting for x in both Eqns. (13) and (14), we obtain:

$$E_0(0) = \frac{-qN_a x_{po}}{\varepsilon_s} = \frac{-qN_d x_{no}}{\varepsilon_s}$$

This is in agreement with our earlier observation in Eq. (12) that the net charge on both sides is equal. The electric field is a maximum at $x = 0$ because both charged regions contribute fully to the electric flux. In either P or N regions, there is cancellation of charge, which reduces the electric flux (Gauss's Law).

3.3.1.2 Finding the Electric Potential

By applying Poisson's equation, Eq. (5), and integrating our expressions for electric field in Eqns. (13) and (14), we can obtain the potential throughout our PN junction.

Poisson's Equation

$$\phi(x) - \phi(x_0) = \int_{x_0}^{x} -E(x)dx \qquad (5)$$

On the P-side of the depletion region, $-x_{po}<x<0$,

$$\phi_0(x) = \int_{-x_{po}}^{x} -E_0(x)dx + \phi_0(-x_{po}) = \int_{-x_{po}}^{x} \frac{qN_a}{\varepsilon_s}(x + x_{po})dx + 0$$
$$= \frac{qN_a}{\varepsilon_s}\left(\int_{-x_{po}}^{x} x\,dx + \int_{-x_{po}}^{x} x_{po}\,dx\right)$$

We usually set as 0, the reference potential, $\phi_o(-x_{po})$, at the boundary between the depletion region and bulk silicon on the P-side. The above integral solves to:

$$\phi_0(x) = \frac{qN_a}{2\varepsilon_s}(x + x_{po})^2 \qquad (-x_{po} < x < 0) \qquad (15)$$

For the N-side of the depletion region, we can again integrate our expression for electric field on the N-side – Equation (14), but we must remember to add our constant of integration – the potential created by the charge and electric field of the P-side.

$$\phi_0(x) = \int_0^x -E_0(x)dx + \phi_0(0) = \int_0^x -\frac{qN_d}{\varepsilon_s}(x - x_{no})dx + \frac{qN_a}{2\varepsilon_s}(0 + x_{po})^2$$
$$= \frac{qN_d}{\varepsilon_s}\left(-\int_0^x x\,dx + \int_0^x x_{no}\,dx\right) + \frac{qN_a}{2\varepsilon_s}x_{po}^{\,2}$$

Solving this expression, our potential on the N-side is found to be:

$$\phi_0(x) = \frac{qN_d}{2\varepsilon_s}x(2x_{no} - x)^2 + \frac{qN_a}{2\varepsilon_s}x_{po}^{\,2} \qquad (0 < x < x_{no}) \qquad (16)$$

The electric potential of our PN junction in thermal equilibrium is shown in Fig. 19.

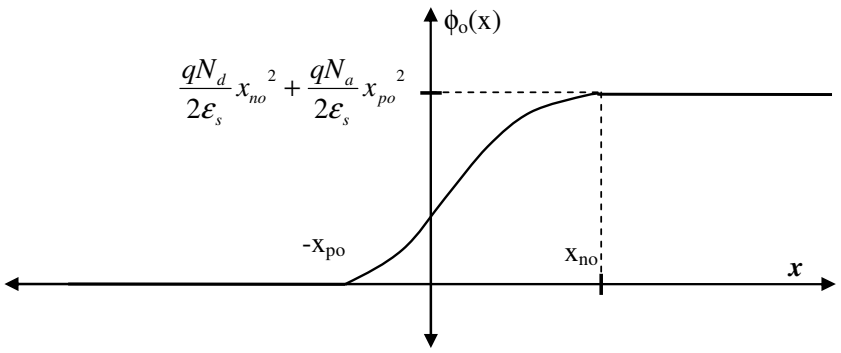


Fig. 19. Electric Potential, $\phi_0(x)$, of the PN junction, with depletion region as approximated in Equation (10).

The potential at $x \geq x_{no}$ can be found by substituting x_{no} for x into Eq. (10). The value of this potential can be written multiple ways:

$$\phi_0(x \geq x_{no}) = \frac{qN_d}{2\varepsilon_s} x_{no}^{\ 2} + \frac{qN_a}{2\varepsilon_s} x_{po}^{\ 2} = \frac{qN_d x_{no}}{2\varepsilon_s}\left(x_{no} + x_{po}\right)$$
$$= \frac{qN_a x_{po}}{2\varepsilon_s}\left(x_{no} + x_{po}\right) \qquad (17)$$

This value in Eq. (17) represents a built-in potential of the PN junction that limits the flow of charge carriers. For example, positive charges naturally move from high potential to lower potential, so holes moving in the $+x$ direction must possess sufficient energy to overcome the potential barrier, and make it into the bulk silicon region, $x \geq x_{no}$. Similarly, electrons naturally move from low to high potential, so for them to move in the $-x$ direction also requires sufficient energy to overcome the built-in potential.

3.3.2 PN Junction in Equilibrium

The PN junction in thermal equilibrium, with no external applied electric field, does not have any current flow. In this case, the drift current due to the depletion region's built-in electric field is equal and opposite in magnitude to the diffusion current caused by the different doping concentrations. The built-in potential has the right size and height so the amount of electrons having enough energy to move up the potential by diffusion equals the amount of electrons moving down it, due to drift. Fig. 20 illustrates an energy level profile of the PN junction:

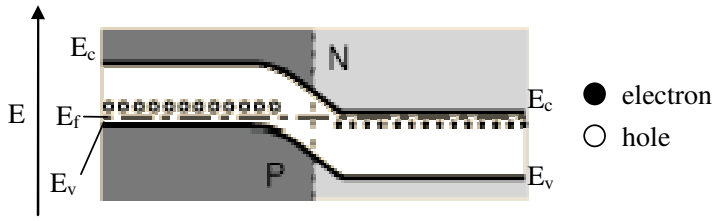


Fig. 20. Energy bands of PN Junction in Equilibrium.

The Fermi level, E_f, is the same in both P-region and N-region, because it is in thermal equilibrium, but the bottom of conduction band, E_c, and the top of the valence band, E_v, are at different levels in the two regions, due to the built-in potential across the depletion region.

Note that the direction of the energy barrier is opposite that of the potential diagram of Fig. 19. This is because Fig. 20 displays electron energy levels, increasing in the upward direction. In Fig. 19, the potential displayed is for positive charges, such as holes. Thus, holes moving from the P-side into the N-side (against the higher potential), require energy to push them down into the valence band, where they are mobile. Likewise, for electrons moving towards the left, the P-region is at lower potential (and thus unfavorable for negative charges). So for electrons to pass through to the bulk region of the P-side, they must have sufficient energy to push them up into the higher energy conduction band of the P-side.

3.3.3 Reverse Bias

When an electric potential, or voltage, is applied, with positive potential on the N-side of the diode, the diode will conduct only negligible current. Current flow through the device requires the combination of holes and electrons at the junction. Instead, the applied potential forces electrons on the N-side away from the junction, and forces holes on the P-side away as well. This results in widening of the depletion region, which increases the charge, electric field, and hence potential barrier across the junction, as shown in Fig. 22.

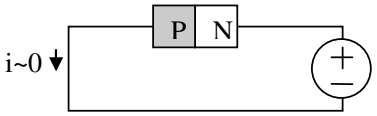


Fig. 21. Circuit of PN junction in reverse bias.

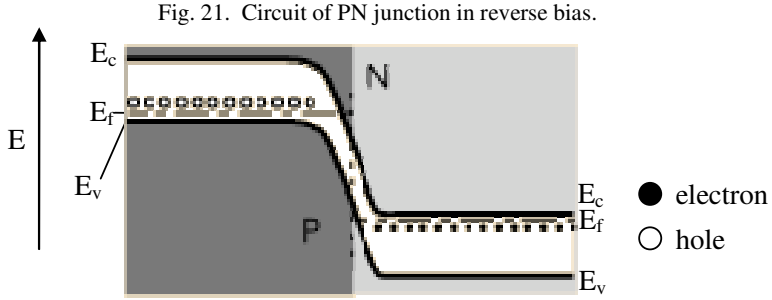


Fig. 22. Energy bands of PN junction in reverse bias.

The tiny amount of current that does flow is due to minority carriers (electrons in p-type and holes in n-type) from the neutral regions (p and n type semiconductors, respectively) diffusing across into the depletion region and drifting across the junction, due to the applied electric field.

3.3.4 Forward Bias

When a voltage is applied with its positive reference at the P-side of the diode, the diode can conduct considerable current.

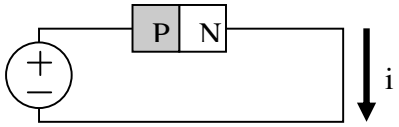


Fig. 23. Circuit of PN junction in forward bias.

The electric field created by the potential forces electrons on the N-side towards the junction, while holes on the P-side are pushed towards the junction as well. This causes current to flow (electrons from n-side to flow to p-side and vice versa), as the built-in potential is overcome by the applied voltage. Now, current can flow with very little resistance, because the depletion region has been diminished, and the built-in potential lowered.

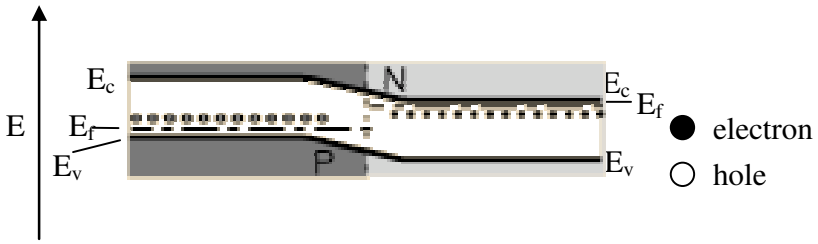


Fig. 24. Energy bands of PN Junction in forward bias.

As illustrated in Fig. 24, an applied voltage above that of the built-in potential will result in electrons high in energy on the N-side, above the conduction band of the P-side. Now the potential is "downhill" for electrons, meaning they can flow across with ease. When they enter the junction, they readily recombine with holes, resulting in a net current flow. It is in both directions in which this process of recombination occurs: majority carriers diffuse across the junction and then becoming minority carriers, combining with the majority carriers in the local region, and "dying out" far from the junction.

3.4 References

Fig. 1., Section 4.1 – Howe & Sodini, Microelectronics: An Integrated Approach, Prentice Hall, 1997.

Fig. 2, 5, 6(a)(b), 7(a)(b), 16, 20, 22, 24 – Hyperphysics, Internet. http://hyperphysics.phy-astr.gsu.edu/hbase/hph.html

Chapter 4. Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

4.1 Introduction

A **transistor** is a semiconductor device that uses a small amount of voltage or electrical current to control a larger change in voltage or current. Because of its fast response and accuracy, it may be used in a wide variety of applications, including amplification, switching, signal modulation, and as an oscillator. The transistor is the fundamental building block of both digital and analog circuits — the circuitry that governs the operation of computers, cellular phones, and all other modern electronics.

The **field-effect transistor** (FET) is a transistor that relies on an electric field to control the shape and hence the conductivity of a 'channel' in a semiconductor material. FETs are sometimes used as voltage-controlled resistors. Field-effect transistors are devices that are used in amplifiers and logic gates.

The **metal-oxide-semiconductor field-effect transistor** (**MOSFET**, **MOS-FET**, or **MOS FET**), is by far the most common field-effect transistor in both digital and analog circuits. A MOSFET is a three-terminal device that uses the voltage between two terminals to control the current flowing in the third terminal. Therefore it can be realized as a voltage-controlled current source.

Some of the basic symbols can be found in the following table.

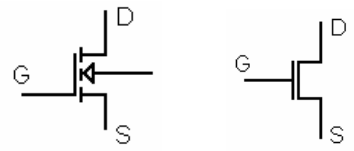
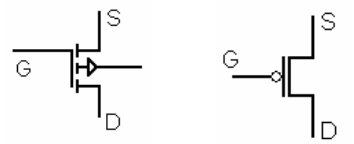
Symbol	Definition
	N-MOSFET symbols. Note that the Drain terminal is on top and the Source terminal on bottom. In the first picture, the arrow points towards the Gate terminal.
	P-MOSFET symbols. Note that the Source terminal is on top and the Drain terminal on bottom. In the first picture, the arrow points away from the Gate terminal.

Table 1. Symbol Information depicting the symbols that will be used throughout the remainder of this text.

4.2 Notation

Superposition is a very important concept while analyzing transistors. For this reason, many types of variables with different subscripts are used. Upper-case letters with upper-case subscripts, e.g. V_{GS}, represent results due to DC analysis. For the value of a single point, it is usually labeled with a subscript "Q", e.g. V_{GSQ}. Lower-case letters with lower-case subscripts, e.g. v_{gs}, represent results due to AC analysis. Finally, lower-case letters with upper-case subscripts, e.g. v_{GS}, represent the general or total, i.e. the result achieved by summing the DC and the AC results.

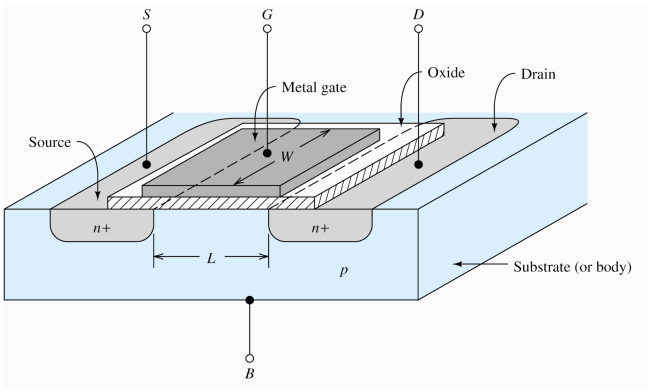


Fig. 1. A device drawing of an NMOS transistor. *L* represents the length of the channel and *W*, the width.

4.3 NMOS and PMOS Transistors

Figure 1 depicts the structure of an n-channel enhancement-mode MOSFET, also known as an **NMOS** transistor. The substrate, or body, is doped with acceptors to form p-type silicon. Two regions on the top surface of the substrate are doped to form n-type silicon as indicated by the n^+ regions in the figure. Metal is deposited to form contacts to the n+ regions. The two contacts are labeled **source** (S) **and drain** (D), with another metal to contact the bottom of the substrate, labeled **body** (B). Between the source and drain, a metal contact is deposited on top of a layer of silicon dioxide, which, in turn, is deposited on top of the p-Si. This contact is labeled **gate** (G). The gate metal, silicon dioxide and semiconductor underneath form the most important constituents, which is the reason that this type of FET is called MOS-FET.

At a first glance, the source-body and drain-body connections are both n-p junction. And hence, we do not expect different characteristics than a simple diode if a voltage is applied to source-body or drain-body independently. However, by placing a MOS junction in-between, very interesting characteristics is achieved.

Instead of using metal electrode, the gate of modern transistors are typically highly doped poly-silicon. Hence, it is best to explain the MOS as n++-O-p junction. When a positive gate-body voltage is applied, the junction is reverse biased. Due to the oxide being an insulator, no current flows through the gate terminal. As the gate-body voltage increased above a certain positive value (called threshold voltage V_{to}), a thin layer of electrons is formed at the oxide-Si interface. This layer is called the inversion layer, which forms a bridge to conduct electrons from source to drain. As the channel is n-type, with electrons as the conducting carriers, this type of MOSFET is called N-MOSFET. Current can flow into the drain, through the channel, and out the source if a drain to source voltage, v_{DS}, is applied. You may notice that the terms "source" and "drain" seem to be backwards. This is because they are the source and drain of *carriers*, which in the case of a NMOS are electrons. Varying the gate-body voltage changes the inversion layer thickness and hence the resistance of the drain-source channel. Typically we short the body and source contacts, and the gate-source voltage v_{GS} is used to control drain-source current i_{DS}. The device characteristics also depend on device dimensions, such as L, the length of the channel, and W, the width of the channel.

P-MOSFET is similar to NMOS, except all n-doped regions in Fig. 1 are p-doped and the substrate is n-doped. With a negative v_{GS}, the MOS junction is reverse biased. When v_{GS} becomes smaller than a certain V_{to} (typically negative), an inversion layer of holes is formed at the oxide-substrate interface, which forms the channel to conduct between drain-source. The source and body are conventionally shorted, as in NMOS. The drain-source voltage v_{DS} is kept the same sign as v_{GS}, which in this case will be negative. Thus i_{DS} is also negative.

4.4 N-MOSFET Operating Regions

The I-V characteristic for a MOSFET is more complicated than a diode, simply because there are two control voltages, v_{DS} and v_{DS}. Depending on their relative values, the MOSFET can be in one of three modes: cut-off, triode or saturation.

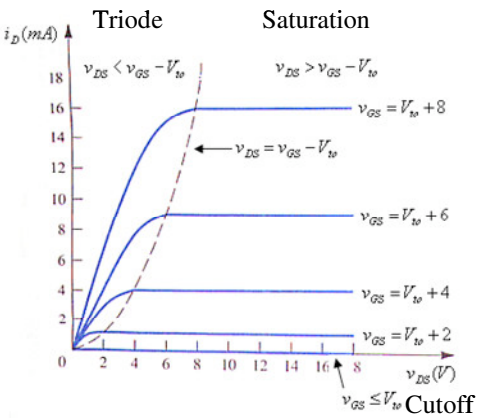


Fig. 2. NMOS characteristic curves. When $v_{GS} < V_{to}$, i_D is zero and the NMOS is in cut-off region. In the triode region, i_D increases for increases in v_{DS}. In the saturation region, i_D increases only if v_{GS} increases. The dashed line shows the boundary between the triode and the saturation region.

4.4.1 Cut-off

If $v_{GS} < V_{to}$, then no channel forms under the oxide insulator and even if a $v_{DS} > 0$ is applied, virtually no current will flow. Note this is indicated in Fig. 2 in which there appears a dark line at $i_D = 0$. This is known as the cut-off region and even as v_{GS} increases, the device remains in the cut-off region until $v_{GS} > V_{to}$.

$$i_D = 0 \quad for \quad v_{GS} < V_{to} \qquad (4.1)$$

4.4.2 Triode

As v_{GS} increases above the threshold voltage and for $v_{DS} < v_{GS} - V_{to}$, the NMOS is in the triode region. The inversion layer is formed under the gate, between the source and the drain. For small positive v_{DS}, the current i_D increases with v_{DS} somewhat linearly. This is because the resistance of the channel is determined by the dimension of the inversion layer, which is independent of v_{DS} for small v_{DS}. As v_{DS} increases, current increases much less rapidly because the channel is getting thinner at the drain side. An equation to approximate the thinning of the inversion channel can be derived, which thus leads to the equation for i_D, which is proportional to v_{DS}^2.

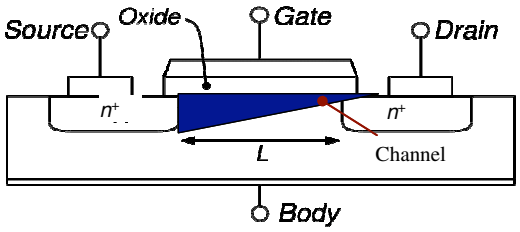


Fig. 3. Channel pinch-off occurs near the drain as v_{DS} increases. The thickness of the channel at the drain is zero when the device goes into saturation region.

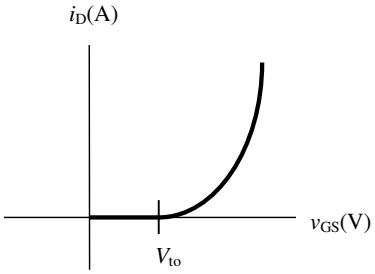


Fig. 4. When $v_{GS}<V_{to}$, the current flowing into the drain is zero. However, after the barrier has been reached, the current follows a quadratic trend with increases in v_{GS}.

In this regime, as v_{GS} increases, the channel becomes thicker, which reduces the resistance and increases i_D. Thus, we can think of the device as a voltage-controlled resistor that decreases its resistance with increases in v_{GS}. The triode region is to the left of the dashed line in Fig. 2.

$$i_D = K\left[2\left(v_{GS} - V_{to}\right)v_{DS} - {v_{DS}}^2\right] \quad for\ v_{DS} + V_{to} < v_{GS} \qquad (4.2)$$

$$where\ K = \frac{W}{L}\frac{KP}{2}$$

where W is the width of the channel, L the length, and KP is a factor depending on the oxide layer.

4.4.3 Saturation

For a fixed v_{GS}, as v_{DS} increases, the gate-to-drain voltage, v_{GD}, will equal the threshold voltage (v_{GS} - v_{DS} = V_{to}). The thickness of the channel at the drain end becomes zero at this point. Thus, for further increases in v_{DS}, there are no further changes to i_D. This refers to saturation of the channel, and the curves begin to flatten as shown in Fig. 2. The saturation occurs due to the channel pinch-off caused by the disappearance of the channel layer close to the drain as shown in Fig. 3. Note, in the saturation region, the current is constant for a fixed v_{GS} and independent of v_{DS}. The drain current is given by:

$$i_D = K(v_{GS} - V_{to})^2 \quad for\ V_{to} \le v_{GS} \le v_{DS} + V_{to} \qquad (4.3)$$

where K is the same as above. Fig. 4 shows i_D versus v_{GS}. Note, i_D=0 when $v_{GS} < V_{to}$.

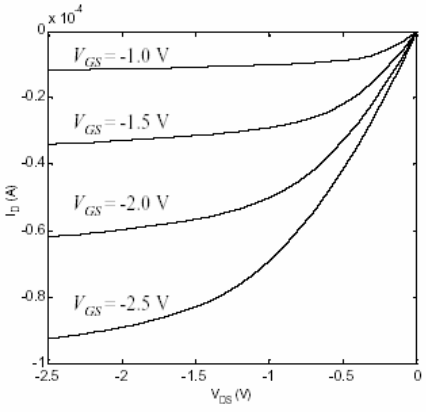


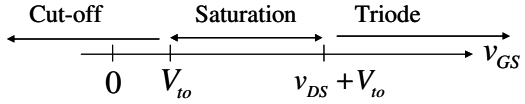
Fig. 5. PMOS characteristic curves. PMOS is in cut-off region when $v_{GS} > V_{to}$ and i_D=0. In the triode region, i_D decreases for decreasing v_{DS}. In the saturation region, i_D decreases only if v_{GS} decreases. The dashed line shows the boundary between the triode and the saturation region.

4.5 PMOSFET Operating Regions

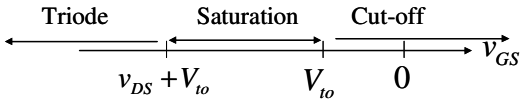
PMOS also has three operating regions, cut-off, saturation and triode. In general, all signs are opposite to those of NMOS. Typical PMOS i_D-v_{DS} curves for various v_{GS} values are shown in Fig. 5. Note that in the following as well as in Fig. 5, $\boldsymbol{i_D=i_{DS}}$. This is different from our text book, where $\boldsymbol{i_D=i_{SD}}$ for PMOS.

	NMOS	PMOS (Note $\boldsymbol{i_D=i_{DS}}$)
Channel carrier	Electrons	Holes
V_{to}	Positive	Negative
Cut-off Region	$i_D = 0 \quad for\ v_{GS} < V_{to}$	$i_D = 0 \quad for\ v_{GS} > V_{to}$
Saturation Region	$i_D = K(v_{GS} - V_{to})^2$ $for\ V_{to} \le v_{GS} \le v_{DS} + V_{to}$	$i_D = -K(v_{GS} - V_{to})^2$ $for\ V_{to} \ge v_{GS} \ge v_{DS} + V_{to}$
Triode Region	$i_D = K\left[2(v_{GS} - V_{to})v_{DS} - {v_{DS}}^2\right]$ $for\ v_{DS} + V_{to} < v_{GS}$	$i_D = -K\left[2(v_{GS} - V_{to})v_{DS} - {v_{DS}}^2\right]$ $for\ v_{DS} + V_{to} > v_{GS}$

The following summarizes the regions of operation for NMOS and PMOS.



NMOS Regions of operation



PMOS Regions of operation

Chapter 5. Simple MOSFET Circuits

5.1 Analysis for MOSFET Amplifiers

As previously discussed, we are interested in analyzing MOSFET circuits for analog and digital applications. For analog applications, we are most concerned with small-signal AC response. In particular, we are interested in three parameters: small-signal gain, input impedance and output impedance. The latter two enables us to cascade the amplifiers. The steps include the following:

1. DC analysis to determine the Quiescent (Q) operating point. The results of this analysis are I_{DQ}, V_{DSQ}, and $V_{GSQ,}$ with which we can get the small-signal MOSFET model
2. Replace the original circuit with the small-signal MOSFET model.
3. Analyze the new AC circuit use KCL, KVL or Thevenin (or Norton) equivalent circuits.

In the following, we will show how to obtain these three parameters in a step-by-step fashion.

5.1.1 DC Analysis – Load-Line Analysis

Since it is DC analysis, we turn-off all AC sources and **replace all capacitors with opens and inductors with shorts**.

After this step, we can write two KVL equations.

∞ Equation (5.1) will be for the loop including V_{DS} and equation will be in the form of I_D as a function of V_{DS}. Remember that there is a voltage drop of V_{DS} from the drain to the source terminal.

∞ Equation (5.2) will be for the loop V_{GS}. The most crucial point to remember is that **there is NO gate current.** This equation will be in the form of I_D as a function of V_{GS}.

A. If equation 5.2 leads to a constant V_{GS}, we can use equation 5.1 as the load line in conjunction with MOSFET I_D-V_{DS} characteristic curve, e.g. Figure 4.2, to solve for I_D and V_{DS}.

B. If equation 5.2 is a functional equation and V_{GS} is a function of I_D. First, we assume the bias is such that the MOSFET is in saturation region, use load-line analysis for equation (5.2) and MOSFET saturation mode equation (4.3) to solve for I_D and V_{GS}. With these two values, we can then find V_{DS} using equation (5.1).

But if there is no solution for V_{GS}, we know MOSFET is in triode mode and will need to use equation (4.2) to solve for I_D, V_{GS}, and V_{DS}.

After determining the DC bias point, i.e. Q point, we label the values for I_{DQ}, V_{GSQ}, *and* V_{DSQ}. We can now move on to the small signal model.

5.1.2 Small-Signal Equivalent Circuit

To do AC analysis on the circuit, we need to replace DC sources by ground, capacitors by short circuits, and inductance by open circuits. Next, we replace the MOSFET a voltage controlled current source in parallel with a resistor. This model is valid only when the MOSFET is biased in the saturation mode.

The reason for the resistor is because in the saturation region, i_D is not exactly flat as shown in Fig. 4.2 but slopes slightly upward. Usually, it is a good approximation for the line to be horizontal (in Figure 4.2), in which case r_d is infinite. Note that the current source is connected between the drain and the source terminal. The value, g_m known as transconductance of the MOSFET is a measure of a transistor's sensitivity to the input voltage. If the characteristic curves such as Figure 4.2 are provided, you can find the value of g_m by holding v_{DS} constant at V_{DSQ} and calculating the change in i_D with respect to a change in v_{GS}:

$$g_m = (\Delta i_D / \Delta v_{GS})\Big|_{v_{DS}=V_{DSQ}} \qquad (5.3)$$

On the other hand, if an equation is provided for i_D, g_m is found by taking the partial derivative of that equation with respect to v_{GS}:

$$g_m = \partial i_D / \partial v_{GS} \qquad (5.4)$$

Plugging in equation 4.3 into equation 5.4 yields another way to find g_m:

$$\begin{aligned} g_m &= 2K(V_{GSQ} - V_{to}) \\ &= 2\sqrt{KI_{DQ}} \\ &= \sqrt{2KP}\sqrt{W/L}\sqrt{I_{DQ}} \end{aligned} \qquad (5.5)$$

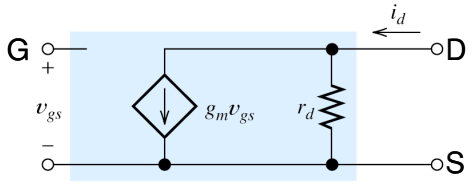


Fig. 5.1. Small signal model for MOSFET under saturation mode. It includes a voltage-controlled current source between drain and source terminals. The direction of the current is always from the drain to the source.

Similarly, through characteristic curves, you can get the value of r_d by holding v_{GS} constant at V_{GSQ} and calculating the change in i_D with respect to a change in v_{DS}:

$$(1/r_d) = (\Delta i_D / \Delta v_{DS})\Big|_{v_{GS}=V_{GSQ}} \qquad (5.6)$$

Remember, you must reciprocate the above equation to find r_d.

Similarly, r_d is found by taking the partial derivative of the i_D equation with respect to v_{DS}:

$$(1/r_D) = \partial i_D / \partial v_{DS} \qquad (5.7)$$

Remember, you must reciprocate the above equation to find r_d.

5.1.3 Finding Voltage Gains, Input, and Output Resistances

After drawing the small-signal equivalent circuit, we can find small signal voltage gain, input, and output resistances. There are examples in the text book (pages 556, and 569-570). The terms are defined as follows:

Voltage gain A_v: the ratio of the output voltage to the input (AC) voltage.

Input Impedance R_{in}: the impedance looking into the circuit from the input terminal; it is equal to input voltage, v_{in}, divided by input current, i_{in}.

Output Impedance R_{out}: The output impedance is the impedance looking into the circuit from the load terminals. It can be found most often with steps 1 and 2 below and then by inspection into the load terminals. However, sometimes it requires step 3 to find the value.

1. Remove the load resistance, R_L from the small-signal equivalent circuit.
2. Turn off independent source (remember voltage sources become short circuits when they are zeroed out and current source will be open).
3. Attach a test source, v_x, to the output terminals. The output terminal is where you removed the load resistance from. Find the current coming out of the test source as i_x. Use KCL or KVL to write down an equation relating v_x and i_x. Simplify the equation such that these are the only two unknowns in your equation. The output resistance, R_{out}, is equal to v_x divided by i_x.

5.2 The Inverter:

Fig. 5.2(a) below shows the symbol of an inverter, also known as a NOT Gate. Fig. 5.2(b) depicts a graph of V_{out} vs. V_{in}, which shows the function of an ideal inverter: when the input voltage is low, the output voltage is high and vice versa.

5.2.1 Constructing a Logic Gate: the Use of Pull-Down and Pull-Up Networks

Because an inverter is a type of logic gate, it will be better to first analyze how logic gates are made. To construct a logic gate, we must make use of both pull-down and pull-up networks. A pull-down network is a set of devices used to carry current from the output node to ground. This discharges the output node hence pulling down the voltage. NMOSFETs function as pull-down devices when they are turned on and are used to connect the output to ground. Note that when an NMOS is on, the n-type channel formed within it allows for current to easily flow when a voltage is applied to it. Remember that the channel can only form when the input voltage to the NMOS, V_{GS}, is high and greater than V_{to}. So, you can think of an NMOS as a short circuit when its input voltage is high and an open circuit when its input voltage is low.

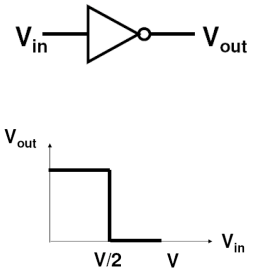


Fig. 5.2(a) above shows the symbol of a basic inverter. (b) shows the ideal characteristic of an inverter. A low input voltage yields a high output voltage and vice versa.

PMOSFETs and resistors function as pull-up devices and are used to connect the output to the DC source, V_{DD}. Note that when a PMOS is on, the p-type channel formed within it allows for current to easily flow when a voltage is applied to it. Remember that the channel can only form when the input voltage to the PMOS, V_{GS}, is low and less than V_{to}. So, you can think of a PMOS as a short circuit when its input voltage is low and an open circuit when its input voltage is high.

Fig. 5.3 shows the setup of a typical pull-up network in series with a pull-down network to yield a logic gate with multiple inputs. In this class, we will be analyzing these networks with mostly one input.

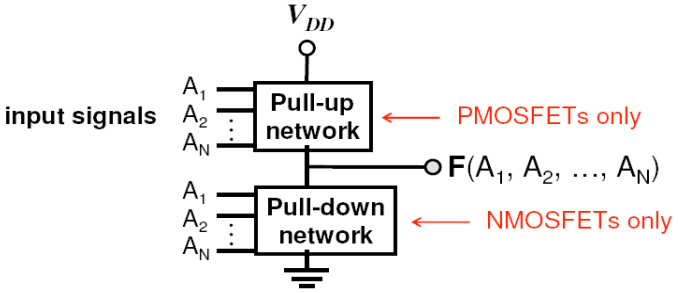


Fig. 5.3. The basic setup of a pull-up network and a pull-down network which yields the basic inverter. F is the output signal and is equal to the voltage drop across the pull-down network.

It is perhaps the most convenient to remember the following: when there is no current flow in the pull-up network, the output voltage is pulled up to V_{DD}, and hence F is 1 in the logic state. On the other hand, if there is current flow, voltage drop in the pull-up network will make the output at F a low voltage and logic state of 0. The condition is just the opposite for the pull-down network. We summary in the table below. This point is illustrated by Fig. 5.7b and 5.7c will become obvious when we discuss logic gates next.

Pull-up current	V_F	logic state of F	Pull-down current	V_F	logic state of F
0	V_{DD}	1	Non-zero	Some value	1
Non-zero	Some value	0	0	GND	0

Fig. 5.4 and Fig. 5.7 show circuit diagrams using specific devices for the pull-up and pull-down network. The reason for the setup in these figures yielding an inverter is discussed later. Note that the pull-up network is used to connect V_{DD} to F (the output node) and the pull-down network is connecting F to ground. Note that the input signals, (A_1, …, A_N), to each network are the same. So, if the signals are high, the pull-up network is off (it's an open circuit), and the pull-down network is on (it's a short circuit). This means that the voltage drop across the pull-down network which equals F is 0 V or low. This is where the name pull-down comes from, as F is pulled to ground. On the other hand, if the signals are low, the pull-up network is on (it's a short circuit), and the pull-down network is off (it's an open circuit). This means that the voltage drop across the pull-up network is 0 V and there is voltage drop of V_{DD} across the pull-down network. Because F equals the voltage drop across the pull-down network, it is also V_{DD}, or high. Because of a 0 V drop across itself, the pull-up network yields the high output voltage across F. This is where the name pull-up comes from.

5.2.2 NMOS Resistor Pull-Up

Fig. 5.4 shows the NMOS resistor pull-up device, which acts as an inverter. The resistor acts as the pull-up device and the NMOS as the pull-down device. Note that the pull-up device connects V_{DD} to the output, V_{OUT}, and the pull-down device connects V_{OUT} to the ground. The way this device works as an inverter can readily be seen in Fig. 5.5 and in Fig. 5.6.

Fig. 5.5 shows the load-line analysis of this circuit. The load line has been constructed in the same way mentioned earlier and is graphed with the NMOS's characteristic curves. Note that V_{GS} is simply V_{IN} and V_{DS} is equal to V_{OUT}. Each intersecting point gives the value of V_{DS} for a given V_{GS}. Note when V_{GS} or V_{IN} is small, V_{DS} or V_{OUT} is large and vice versa. This also makes sense intuitively. When V_{GS} or V_{IN} is low (below V_{to}), no channel forms within the NMOS and therefore no current flows through it, which means the transistor is off. Because no current flows through the transistor, no current flows through the resistor. This means that V_{OUT} equals V_{DD}, which is high. When V_{IN} is high (above V_{to}), a channel does form and current flows easily through the transistor, which means there is current flowing through the resistor and there is a voltage drop across the resistor. As the current gets larger, most of V_{DD} is dropped across the resistor and the V_{DS} gets smaller. The current gets larger when the channel gets wider, which only occurs with an increase in V_{GS} or V_{IN}. Fig. 5.6 is derived from the intersecting points of Fig. 5.5. For example, when V_{GS} is very high, V_{DD} is very low, which is represented by the green diamond point labeled in Fig. 5.5. This point is also labeled in Fig. 5.6 with a green diamond. As V_{GS} lowers, V_{DD} increases and this point is represented by the square in figures 5.5 and 5.6.

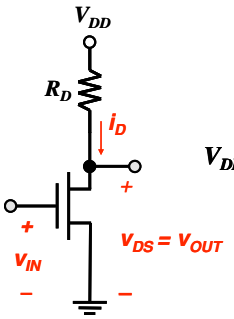


Fig. 5.4. The NMOS resistor pull-up

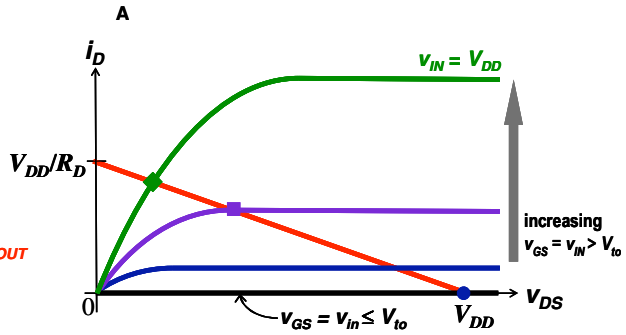


Fig. 5.5. The load line analysis of the NMOS resistor pull-up. Note V_{GS} increases upward. Note V_{GS} equals V_{IN} and V_{DS} equals V_{OUT}.

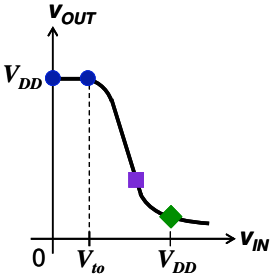


Fig. 5.6 A plot of V_{IN} vs. V_{OUT} for the NMOS resistor pull-up. This is derived from Fig. 5.5, so the diamond point in Fig. 5.5 corresponds to the diamond point in this figure.

5.2.3 The CMOS Inverter

Fig. 5.7(a) shows a CMOS inverter, which contains a PMOS and an NMOS. The PMOS acts as the pull-up device and connects the DC source, V_{DD}, to the output node. The NMOS acts as the pull-down device and is connected in the same way as in the NMOS Resistor pull-up device. To see how the inverter works in digital is simple: when V_{IN} is high, both V_{GSN} (V_{GS} of NMOS) and V_{GSP} (V_{GS} of PMOS) are also high. This means that a channel forms in the NMOS, but no channel forms within the PMOS, so the NMOS acts as a short circuit, but the PMOS is an open circuit. Fig. 5.7(b) shows the circuit diagram for when V_{IN} is high. Because V_{OUT} is measured across the NMOS, it becomes 0 V and is therefore low. Conversely, when V_{IN} is low, a channel forms within the PMOS and no channel forms with the NMOS, so the PMOS acts like a short and the NMOS like an open. Fig. 5.7(c) shows the circuit diagram for when V_{IN} is low. Here also, V_{OUT} is measured across the NMOS, which makes V_{OUT} equal V_{DD} and therefore high.

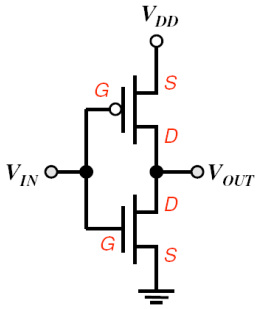


Fig. 5.7(a). The CMOS inverter. This inverter uses a PMOS as the pull-up device and an NMOS as the pull-down device.

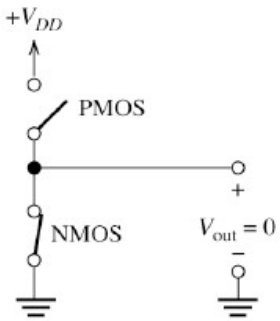


Fig. 5.7(b). The circuit diagram for when V_{IN} is high. The PMOS acts like an open circuit while the NMOS acts like a short circuit.

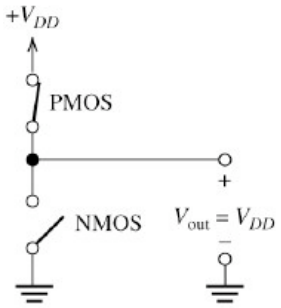


Fig. 5.7(c). The circuit diagram for when V_{IN} is low. The PMOS acts like a short circuit while the NMOS acts like an open circuit.

To analyze this circuit using a more analog method is a bit more complex. We must place the characteristic curves of both the NMOS and the PMOS on the same set of axes. Fig. 5.8(a) shows the *I-V* characteristic of a PMOS. Note the axes are labeled I_{DSP} and V_{DSP}. Earlier, in Fig. 3, we saw the *I-V* characteristic of an NMOS. Even though the axes are labeled I_D and V_{DS}, they should really be labeled as I_{DSN} and V_{DSN}. To plot the two graphs on the same set of axes, we must first find a relationship between these variables. Looking at Fig. 5.7(a), we can obtain the following equations:

$$V_{IN} = V_{DD} + V_{GSP} \qquad (5.8)$$

$$V_{OUT} = V_{DD} + V_{DSP} \qquad (5.9)$$

Note that V_{IN} is the same as V_{GSN} and V_{OUT} is the same as V_{DSN}, so the above equations become:

$$V_{GSN} = V_{DD} + V_{GSP} \qquad (5.10)$$

$$V_{DSN} = V_{DD} + V_{DSP} \qquad (5.111)$$

Also note, that:

$$I_{DSN} = -I_{DSP} \qquad (5.12)$$

So, to plot the PMOS characteristic curves on an I_{DSN} vs. V_{DSN}, we must change the axes from those labeled in Fig. 5.8(a) to those labeled in Fig. 5.8(c). So, we must invert all the values on the y-axis, which yields a reflection of the PMOS graph across its x-axis. This is shown in the Fig. 5.8(b). Note the axes now read I_{DSN} and V_{DSP}. To change the x-axis of the new PMOS graph to V_{DSN}, we use the equation above which states that $V_{DSN} = V_{DD} + V_{DSP}$. This means that we must shift the x-axis of the new PMOS graph to the right by V_{DD}. This is shown in Fig. 5.8(c). Now, placing the new PMOS graph and the NMOS graph, we obtain Fig. 5.9.

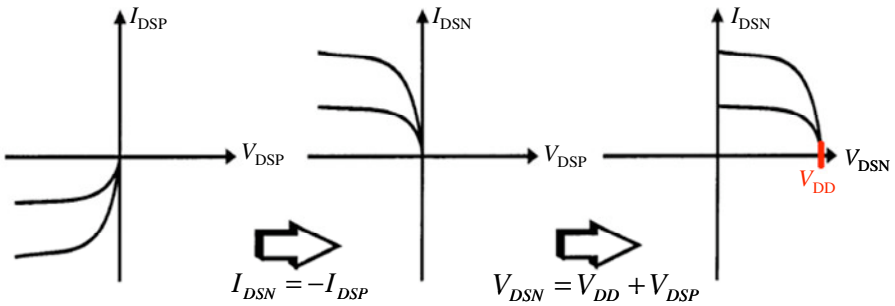


Fig. 5.8(a) shows the *I-V* characteristic curves of a PMOS. Note that the axes are I_{DSP} and V_{DSP}. In Fig. 5.8(b), the y-axis has been

changed to I_{DSN} by the relationship indicated by the arrow. In Fig. 5.8(c), the x-axis has been changed to V_{DSN} by the relationship indicated by the arrow. Fig. 5.8(a) and (c) both show the characteristic curves for a PMOS, however on two different set of axes.

In Fig. 5.9, V_{GSN} increases upward for the NMOS while for the PMOS, V_{GSP} increases downward because for a PMOS, all sign conventions are opposite that of an NMOS. Note that V_{GSN} equals V_{IN} and that there are many intersecting points in the graph, so how do we know which is the right one? The answer is, for a given DC voltage, V_{DD}, and a chosen V_{IN}, the equations above will yield exactly one V_{GSP}. For example, suppose that V_{to}, for the NMOS is 1 V, -1 V for the PMOS, and V_{DD} is fixed at 5 V. Now, let V_{IN} be 1 V, which means that V_{GSN} is also 1 V. Using these values, and the above equations, we find that V_{GSP} equals -4 V. We must find the point where V_{GSN} is 1 V and V_{GSP} is -4 V. This is labeled by the black-colored circle in Fig. 5.9. At this point V_{DSN} equals V_{DD} which equals 5 V. Because V_{DSN} also equals V_{OUT}, V_{OUT} also equals 5 V. So, for V_{IN} equaling 1 V, V_{OUT} equals 5 V. This is labeled in Fig. 5.10 by the same black-colored circle. You should try other values for V_{IN} keeping V_{DD} fixed to see if you obtain the other points labeled in Fig. 5.9. The points labeled in Fig. 5.9 have corresponding points labeled in the same manner in Fig. 5.10, so the white-colored square in Fig. 5.9 corresponds to the white-colored square in Fig. 5.10, etc. By analyzing Fig. 5.9 to yield Fig. 5.10, it becomes clear that the device yields a low output for a high input and vice versa.

5.3 2-Input NAND Gate:

Fig. 5.11 below shows a 2-input NAND gate. It has two NMOS devices in series and two PMOS devices in parallel. To make an M-input NAND gate, you can place M-NMOS devices in series and M-PMOS devices in parallel. To see how this works, remember a NAND gate yields low only wh inputs are high as indicat truth table in Table 2. Tc this works in Fig. 5.11, remember that when the input to an NMOS is high, the NMOS turns on and becomes a short circuit, and when the input is low, the NMOS is off becoming an open circuit. For a PMOS, the conditions are reversed. When both A and B are low, N_1 and N_2 are off, and P_1 and P_2 are on. V_{out} therefore equals V_{DD} and is high. When A is low and B high, P_1 and N_2 are on, and P_2 and N_1 are off. Because N_1 is an open circuit, there is a voltage drop across it which means V_{out} is high. When A is high and B low, N_1 and P_2 are on, and N_2 and P_1 are off. Because N_2 is an open circuit, there is a voltage drop across it which means V_{out} is high. When both A and B are high, N_1 and N_2 are on, and P_1 and P_2 are off. V_{out} therefore equals 0 and is low. This satisfies the truth table shown in Table 2.

$$I_{DSN} = -I_{DSP}$$

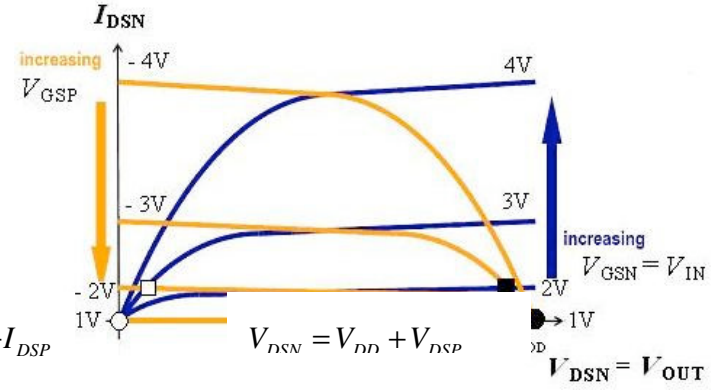


Fig. 5.9. PMOS and NMOS characteristic curves on the same graph with axes I_{DSN}-V_{DSN}. NMOS is in dark and PMOS in light. Note for PMOS, V_{GS} increases as we go down, while for the NMOS, it increases when we go up. The labeled points have corresponding points labeled in the same manner as in Fig. 5.10.

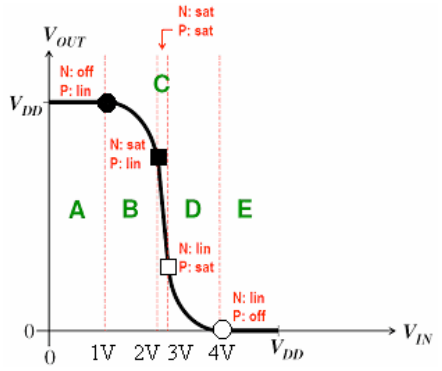


Fig. 5.10. This shows the plot of VOUT vs. VIN for the CMOS inverter. Note when VIN is low, the NMOS is off and the PMOS is in triode region, and VOUT is high. Conversely, when VIN is high, the PMOS is off and the NMOS is in triode region, and VOUT is low. The graph labels the transitions of each transistor as VIN and VOUT change. The labeled points correspond to those in Fig. 5.9.

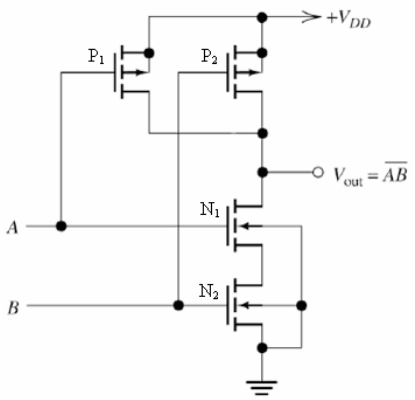


Fig. 5.11. A 2-input NAND gate. There are two NMOS transistors in series and two PMOS transistors in parallel. The output voltage is low only when both NMOS transistors are on, which means that both inputs, A and B, are high.

A	B	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

Table 2. The truth table for a NAND gate. Note that the output voltage is low only when both its inputs are high.

5.4 2-Input NOR Gate

Fig. 5.12 shows a 2-input NOR gate. It has two NMOS devices in parallel and two PMOS devices in series. To make an M-input NOR gate, you can place M-NMOS devices in parallel and M-PMOS devices in series. To see how this works, remember a NOR gate yields high only when all its inputs are low as indicated in the truth table in Table 3. When both A and B are low, N_1 and N_2 are off, and P_1 and P_2 are on. V_{out} therefore equals V_{DD} and is high. When A is low and B high, P_1 and N_2 are on, and P_2 and N_1 are off. Because N_2 is a short circuit, there is no voltage drop across it which means V_{out} is low. When A is high and B low, N_1 and P_2 are on, and N_2 and P_1 are off. Because N_1 is a short circuit, there is no voltage drop across it which means V_{out} is low. When both A and B are high, N_1 and N_2 are on, and P_1 and P_2 are off. V_{out} therefore equals 0 and is low. This satisfies the truth table shown in Table 3.

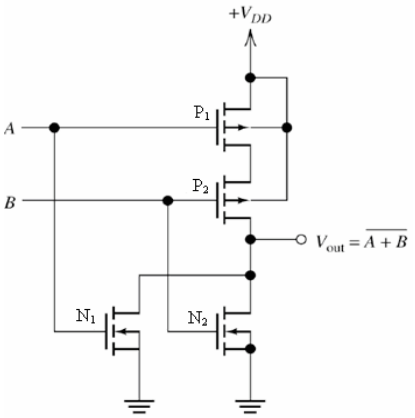


Fig. 5.12. A 2-input NOR gate. There are two NMOS transistors in parallel and two PMOS transistors in series. The output voltage is high only when both NMOS transistors are off, which means that both inputs, A and B, are low.

A	B	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

Table 3. The truth table for a NOR gate. Note that the output voltage is high only when both its inputs are low.

Past Exams

EECS 40, Fall 2006
Prof. Chang-Hasnain
Midterm #1

September 27, 2006
Total Time Allotted: 50 minutes
Total Points: 100

1. This is a closed book exam. However, you are allowed to bring one page (8.5" x 11"), single-sided notes
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. SHOW all the steps on the exam. Answers without steps will be given only a small percentage of credits. Partial credits will be given if you have proper steps but no final answers.
4. Draw BOXES around your final answers.
5. **Remember to put down units.** Points will be taken off for answers without units.

Last (Family) Name: Perfect

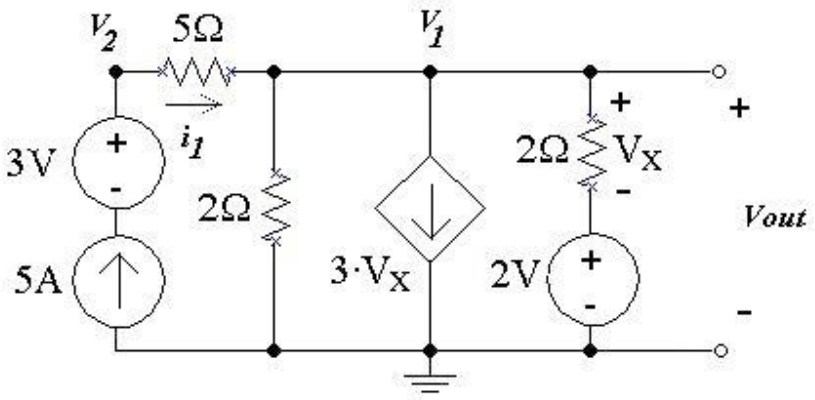
First Name: Peter

Student ID: 00000001 Discussion Session: 000

Signature: _____

Score:	
Problem 1 (50 pts)	
Problem 2 (50 pts):	
Total	

1. (50 pts) Equivalent circuit.



(a) (5 pts) What is the current i_1 through the 5 Ohm resistor?

$$i_1 = 5A$$

(b) (5 pts) Use KVL, write down the equation for V_x in terms of V_1 and/or V_2

$$V_x = V_1 - 2$$

(c) (5 pts) Use KCL, write down the equation for V_1 and solve for V_1

$$-5 + \frac{V_1}{2} + 3 \cdot V_x + \frac{V_x}{2} = 0$$
$$-10 + V_1 + 6 \cdot V_x + V_x = 0$$

$$-10 + V_1 + 7 \cdot V_x = 0$$
$$-10 + V_1 + 7 \cdot (V_1 - 2) = 0$$
$$-24 + 8 \cdot V_1 = 0$$
$$V_1 = 3V$$

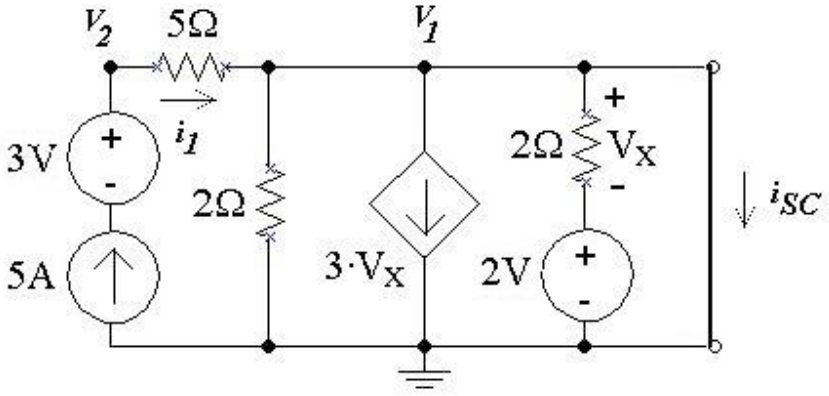
(d) (5 pts) Use KCL, write down the equation for V_2 and solve for V_2

$$-5 + \frac{V_2 - V_1}{5} = 0$$
$$-25 + V_2 - V_1 = 0$$
$$V_2 = 25 + V_1$$
$$V_2 = 28V$$

(e) (5 pts) Solve for V_{out} (this is simply the Thevenin Voltage)

$$V_{out} = V_1$$
$$V_{out} = V_1 = 3V$$

(f) Now we short the two end terminals.



(5 pts) What is V_x ?

$$V_x = V_1 - 2$$
$$V_1 = 0$$
$$V_x = 0 - 2$$
$$V_x = -2V$$

(g) (5 pts) What is V_1 ?

$$V_1 = 0$$

(h) (5 pts) What is I_{sc}?

$$-5+3\cdot V_x + I_{sc} + \frac{V_x}{2} = 0$$

$$-5+3\cdot(-2) + I_{sc} + \frac{-2}{2} = 0$$

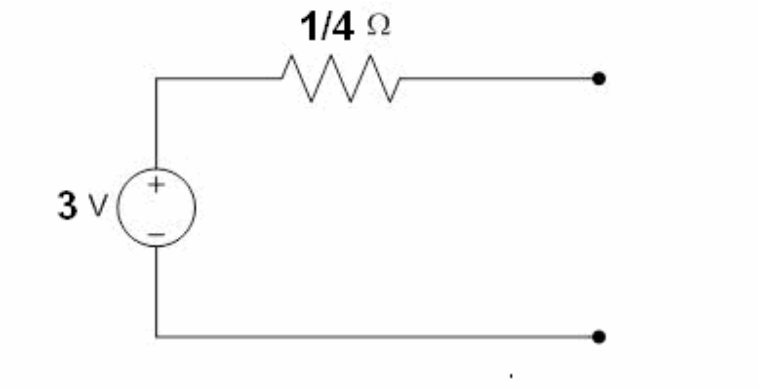
$$I_{sc} = 12A$$

(i) (5 pts) what is the Thevenin Resistance?

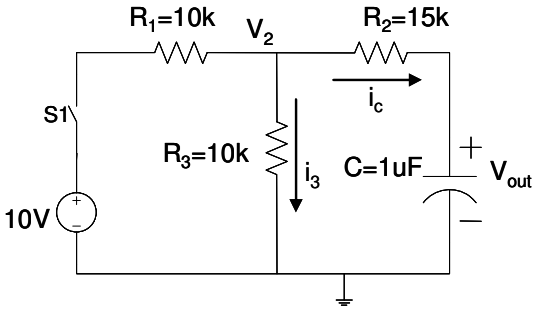
$$R = \frac{V_{oc}}{I_{sc}}$$

$$R = \frac{3V}{12A} = \frac{1}{4}\Omega$$

(j) (5 pts) Draw the Thevenin Equivalent Circuit.



2. For t<0, the switch was open and V_{out}=0. At t = 0s, S1 closes. NOTE: =10^{-6} ; k=10^{3}; e^{-1}=0.37; e^{-2}=0.14 **Remember to put down units.**



(a) (12 pts) Construct the differential equation of V_{out} in terms of all the given quantities. *Hint:you may solve this use Mesh or Nodal analysis, or, even simpler, Thevnin equivalent circuit. Write all your steps.*

Thevenin Equivalence:

Rewrite the 10V source and R1 into a Nodal Equivalent Circuit:

10V source becomes 1A source

R1 is now in parallel with the 1A source.

Combine R1 and R3 together to create a 5k ohm resister.

Rewrite the 1A source and 5k ohm resister into Thevenin Equivalent Circuit.

1A source becomes 5V source

5k ohm resister is in series with the 5V source.

Combine R1||R3 with R2 to yield 20k ohm resister.

We now have a 5V source in series with a 20k ohm resister in series with a 1uF capacitor. Using the predetermined equations, we can fill in the variables and obtain the equation show below.

Nodal Analysis:

$$\frac{V_2 - V_{in}}{10k} + \frac{V_2}{10k} + \frac{V_2 - V_{out}}{15k} = 0$$

$$\frac{V_{out} - V_2}{15k} + C\frac{dV_{out}}{dt} = 0$$

multiply both sides by $30k$

$$3V_2 - 3V_{in} + 3V_2 + 2V_2 - 2V_{out} = 0$$

$$8V_2 - 3V_{in} - 2V_{out} = 0$$

$$V_2 = \frac{3V_{in} + 2V_{out}}{8}$$

$$\frac{V_{out}}{15k} - \frac{1}{15k}\left(\frac{3}{8}V_{in} + \frac{1}{4}V_{out}\right) + C\frac{dV_{out}}{dt} = 0$$

$$V_{out} - \frac{3}{8}V_{in} - \frac{1}{4}V_{out} + 15k \cdot C\frac{dV_{out}}{dt} = 0$$

$$\frac{3}{4}V_{out} + 15k \cdot C\frac{dV_{out}}{dt} = \frac{3}{8}V_{in}$$

$$V_{out} + 20k \cdot C\frac{dV_{out}}{dt} = \frac{1}{2}V_{in}$$

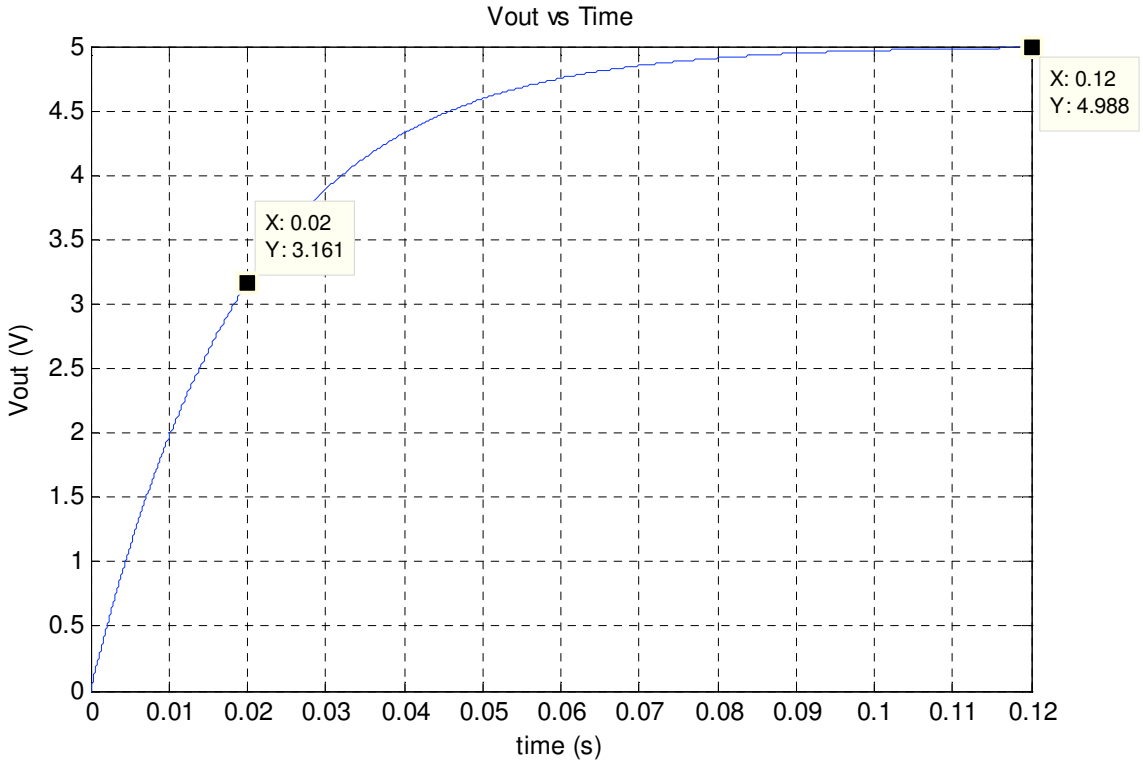
$$V_{out} + 15k \cdot 1uF\frac{dV_{out}}{dt} = 5$$

$$V_{out} + 20ms\frac{dV_{out}}{dt} = 5V$$

(b) (5 pts) Write a closed-form expression for $V_{out}(t)$ for t>0

$$Vout = 5(1 - e^{-t/20ms})$$

(c) (8 pts) Plot V_{out} as a function of time t = 0 to t = 100ms. **Label the y-axis and all key points:** starting value, 1 time constant value, value at infinity.



(Note at 20ms, Vout = 3.15 using the above approximation for e^{-1})
(Note at infinity, Vout should approach 5V)

(d) (5 pts) As t approaches infinity, what value will i_3 approach?

Because at infinity, the capacitor becomes an open,

$$I = \frac{V}{R} = \frac{10}{R1 + R2} = \frac{10}{20k} = \frac{1}{2} mA$$

(e) (5 pts) Now, suppose someone disturbed the circuit and S1 is re-opened at 40 ms again! Construct the new differential equation.

If switch S1 is open, R1 becomes irrelevant because it is connected to an open circuit.
Therefore we combine R2 and R3 to yield a 25k ohm resister.
Again we have a predetermined form and therefore the equation is

$$V_{out} + RC\frac{dV_{out}}{dt} = 0$$

$$V_{out} + 25k \cdot 1uF\frac{dV_{out}}{dt} = 0$$

$$V_{out} + 25ms\frac{dV_{out}}{dt} = 0$$

(f) (6 pts) What is the new time constant? What is the new expression for $V_{out}(t)$ for t>40 ms.

$$\tau = RC = 25ms$$

$$Vout = Ke^{-t/25ms}$$

$$Vout(t = 40ms) = 5(1 - e^{-40ms/20ms}) = Ke^{-0/25ms} = 4.3$$

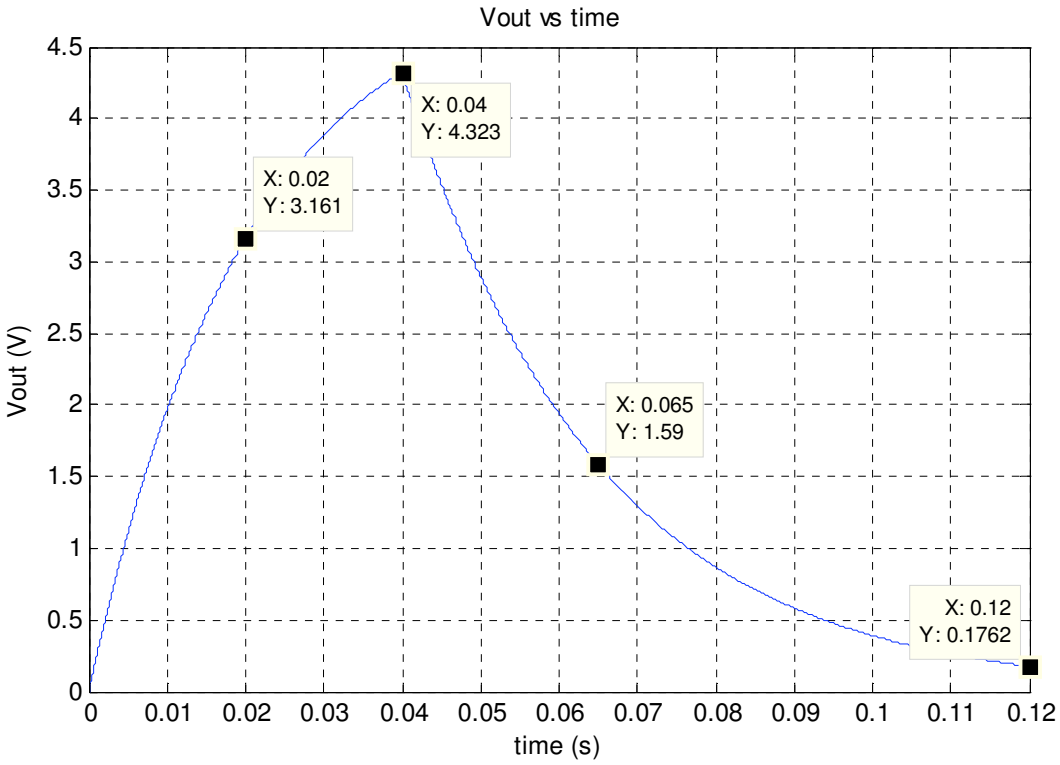
$$K = 4.3$$

$$Vout = 4.3Ke^{-t/25ms}$$

with a $40ms$ *timeshift*

$$Vout = 4.3e^{-(t-40ms)/25ms}$$

(g) (5 pts) Plot the new V_{out} from t=0ms to 100 ms to include the re-opening of the switch at 40 ms. **Label the y-axis and all key points:** starting value, value at switching point, 1 time constant values, value at infinity.



(Note that at 20ms, Vout = 3.15V, using approximation)

(Note that at 40ms, Vout = 4.3V, using approximation)

(Note that at 65ms, Vout = 1.591V, using approximation)

(Note that at infinity, Vout approaches 0V)

(h) (5 pts) In this case, as t approaches infinity, what value will i_3 approach?

$I_3 = 0A$

EECS 40, Fall 2006
Prof. Chang-Hasnain
Midterm #2

October 25, 2006
Total Time Allotted: 50 minutes
Total Points: 100 / Bonus: 10 pts

1. This is a closed book exam. However, you are allowed to bring one page (8.5" x 11"), single-sided notes PLUS your 1-page notes from midterm 1.
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. Slide rules are allowed.
4. SHOW all the steps on the exam. **Answers without steps will be given only a small percentage of credits.** Partial credits will be given if you have proper steps but no final answers.
5. **Remember to put down units.** Points will be taken off for answers without units.

Last (Family) Name: Perfect

First Name: Peter

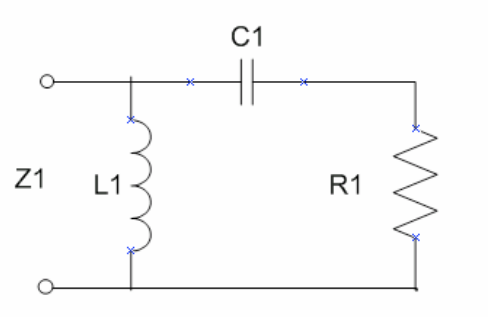
Student ID: 314159265 Discussion Session: 2718

Signature: PP

Score:	**110**
Problem 1 (16 pts) Complex Impedances	16
Problem 2 (54 pts): Bode Plots	54
Bonus (10 pts):	10
Problem 3 (30 pts): Second-order Circuits	30
Total	110

1. [16 points] Parallel and Series Complex Impedance

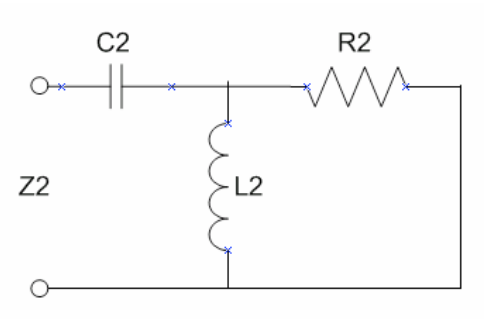
a) [8 pts] What is the complex impedance Z_1?



$$Z_1 = Z_L \,//\, (Z_C + R)$$
$$= j\omega L \,//\, (\frac{1}{j\omega C} + R) = j\omega L \,//\, (\frac{1 + j\omega RC}{j\omega C})$$
$$= \left(\frac{1}{j\omega L} + \frac{j\omega C}{1 + j\omega RC}\right)^{-1} = \left(\frac{1 + j\omega RC + (j\omega L)(j\omega C)}{j\omega L(1 + j\omega RC)}\right)^{-1} = \left(\frac{j\omega L(1 + j\omega RC)}{1 + j\omega RC + j^2\omega^2 LC}\right)$$
$$= \frac{-\omega^2 RLC + j\omega L}{1 - \omega^2 LC + j\omega RC}$$

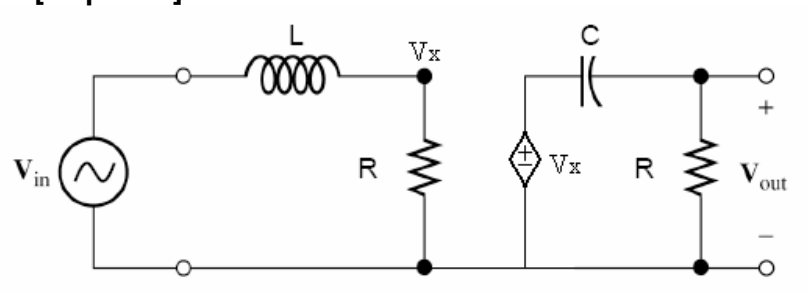
(subscripts omitted for clarity)

b) [8 pts] What is the complex impedance Z_2?



$$Z_1 = Z_C + (Z_L \,//\, R)$$
$$= \frac{1}{j\omega C} + (j\omega L \,//\, R) = \frac{1}{j\omega C} + \left(\frac{1}{j\omega L} + \frac{1}{R}\right)^{-1}$$
$$= \frac{1}{j\omega C} + \left(\frac{j\omega RL}{R + j\omega L}\right) = \left(\frac{R + j\omega L + (j\omega C)(j\omega RL)}{j\omega C(R + j\omega L)}\right) = \left(\frac{R + j\omega L + j^2\omega^2 RLC)}{j\omega RC + j^2\omega^2 LC}\right)$$
$$= \frac{R - \omega^2 RLC + j\omega L}{-\omega^2 LC + j\omega RC}$$

2. [54 points] Bode Plots:



(a) [10 points] For the above circuit, show $H(f) = \frac{1}{1+j\frac{f}{f_2}} \times \frac{1}{1-j\frac{f_1}{f}}$

Express f_1 and f_2 in terms of R, L, C. (Hint: Remember $\omega = 2\pi f$)

Voltage divider on left:

$$V_x = \frac{R}{R + j\omega L} V_{in} = \frac{1}{1 + j\omega \frac{L}{R}} V_{in}$$

Voltage divider on right:

$$V_{out} = \frac{R}{R + \frac{1}{j\omega C}} V_x = \frac{1}{1 - j\frac{1}{\omega RC}} V_x$$

Combining, $V_{out} = \frac{1}{1-j\frac{1}{\omega RC}} \times \frac{1}{1+j\omega\frac{L}{R}} V_{in}$

Swapping the terms, $H(f) = \frac{V_{out}}{V_{in}} = \frac{1}{1+j\omega\frac{L}{R}} \times \frac{1}{1-j\frac{1}{\omega RC}}$

$$= \frac{1}{1+j2\pi f\frac{L}{R}} \times \frac{1}{1-j\frac{1}{2\pi fRC}}$$

f_1 *occurs with* f *in the denominator, and* f_2 with f in the numerator:

$$f_1 = \frac{1}{2\pi RC} \qquad f_2 = \frac{R}{2\pi L}$$

(b) [6 points] Now Let R = 1kΩ, L = 0.16 mH, C = 0.16 uF, what are f_1 and f_2? Remember to put down units.

$$f_1 = \frac{1}{2\pi(1\,k\Omega)(0.16\quad F)} = \frac{6.25}{2\pi \times 10^{-3} s} \approx 1\,kHz$$

$$f_2 = \frac{1\,k\Omega}{2\pi(0.16\,mF)} = \frac{6.25\times10^6}{2\pi\ \ s} \approx 1\,MHz$$

(c) [22 pt] Bode Magnitude Plot. ***You must put down all the steps leading to your results.*** ***Hint:*** **You may consider** $f_1 << f_2$

[4 points] Write down the expression for $y = 10\log\left|H(f)\right|^2$

$$y = 10\log\left|\frac{1}{1+j\frac{f}{f_2}}\right|^2 + 10\log\left|\frac{1}{1-j\frac{f_1}{f}}\right|^2$$
$$= -10\log\left(1+\left(\frac{f}{f_2}\right)^2\right) - 10\log\left(1+\left(\frac{f_1}{f}\right)^2\right)$$

Units are: dB
Note: The other acceptable expression can be found by multiplying the terms in H(f), and finding the magnitude of the resulting product.

[4 points] As frequency goes to a very small value, what is the slope of y as a function of $\log f$?

Constant 1 dominates in left term, f^{-1} dominates in the right term:

$$y = -10\log(1) - 10\log\left(\frac{f_1}{f}\right)^2 = 0 + 20\log\left(\frac{f}{f_1}\right)$$
$$= 20\log f - 20\log f_1$$

Slope: 20 dB / decade

[4 points] As frequency goes to a very large value, what is the slope of y as a function of $\log f$?

f dominates in left term, constant 1 dominates in the right term:

$$y = -10\log\left(\frac{f}{f_2}\right)^2 - 10\log(1) = -20\log\left(\frac{f}{f_2}\right) - 0$$
$$= -20\log f - (-20\log f_2)$$

Slope: -20 dB / decade

[4 points] What is y, $f_1 << f << f_2$?
In both terms, constant 1 dominates:

$$y = -10\log(1) - 10\log(1) = -0 - 0$$
$$= 0\ dB$$

[2 points] What is y at f_1 ?

$$y = -10\log\left(1+\left(\frac{f_1}{f_2}\right)^2\right) - 10\log\left(1+\left(\frac{f_1}{f_1}\right)^2\right)$$

Since $f_1 << f_2$, $y = -10\log(1) - 10\log(1+1)$
$$= -10\log 2 = -3\ dB$$

[2 points] What is y at f_2 ?

$$y = -10\log\left(1+\left(\frac{f_2}{f_2}\right)^2\right) - 10\log\left(1+\left(\frac{f_1}{f_2}\right)^2\right)$$

Again, $f_1 \ll f_2$, $y = -10\log(1+1) - 10\log(1)$

$$= -10\log 2 = -3\ dB$$

[2 points] What filter is this?

Bandpass filter

Bonus [5 points] If the input $|V_{in}| = 1\ V$ and the frequency is 1 MHz, what is the output $|V_{out}|$?

$f_2 = 1\ MHz$ **,** *so* $y = -3\ dB = 10\log(\frac{1}{2})$

$$\frac{1}{2} = |H(f)|^2 = \left|\frac{V_{out}}{V_{in}}\right|^2 \qquad |V_{out}| = \frac{1}{\sqrt{2}}|V_{in}| \approx 0.707V$$

Bonus [5 points] If the input $|V_{in}| = 1\ V$ and the frequency is 10 MHz, what is the output $|V_{out}|$?

$10\ MHz = 10 f_2$ *: one decade past break frequency*

At large f *, slope is -20 dB/decade. Thus, y = -20 dB, since* f *is 1 decade higher than the break frequency, where the Bode approximation is 0 dB.*

$y = -20\ dB = 10\log(\frac{1}{100})$

$$\frac{1}{100} = |H(f)|^2 = \left|\frac{V_{out}}{V_{in}}\right|^2 \qquad |V_{out}| = \frac{1}{\sqrt{100}}|V_{in}| = 0.1V$$

(d) [16 pt total] Bode Phase Plot. ***You must put down all the steps leading to your results. Hint:*** **You may consider** $f_1 \ll f_2$

[4 points] Write down the expression for $\angle H(f)$

$$\angle H(f) = \tan^{-1} 0 - \tan^{-1}\left(\frac{f}{f_2}\right) + \tan^{-1} 0 - \tan^{-1}\left(-\frac{f_1}{f}\right)$$

$$= \tan^{-1}\left(\frac{f_1}{f}\right) - \tan^{-1}\left(\frac{f}{f_2}\right)$$

[4 points] What does the value of $\angle H(f)$ approaches to as $f \to 0$?

$$\angle H(f) = \tan^{-1}(\infty) - \tan^{-1}(0) = \frac{\pi}{2}\ radians$$

[4 points] What does the value of $\angle H(f)$ approaches to as $f \to \infty$?

$$\angle H(f) = \tan^{-1}(0) - \tan^{-1}(\infty) = -\frac{\pi}{2}\ radians$$

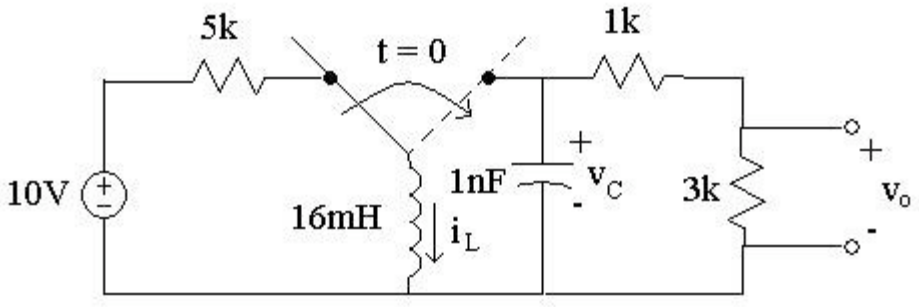
[2 points] What is $\angle H(f)$ at $f = f_1$?

$$\angle H(f) = \tan^{-1}\left(\frac{f_1}{f_1}\right) - \tan^{-1}\left(\frac{f_1}{f_2}\right) = \tan^{-1}(1) - \tan^{-1}(0)$$
$$= \frac{\pi}{4}\ radians$$

[2 points] What is $\angle H(f)$ at $f = f_2$?

$$\angle H(f) = \tan^{-1}\left(\frac{f_1}{f_2}\right) - \tan^{-1}\left(\frac{f_1}{f_2}\right) = \tan^{-1}(0) - \tan^{-1}(1)$$
$$= -\frac{\pi}{4}\ radians$$

3. [30 points] Second-order Circuits:



Assume the switch has been to the left for a long time before switching to the right at t = 0.

(a) Find the following values: [18 points] (Hint: What is $v_o(t)$ in terms of $v_C(t)$?)

$i_L(0+) = \frac{10\,V}{5\,k\Omega} = 2\,mA$ *Inductor is short circuit right before switch is thrown.*	$i_L(\infty) = 0\,A$ *All power is dissipated through resistors.*
$v_C(0+) = 0\,V$ *No stored charge.*	$v_C(\infty) = 0\,V$ *Discharges through resistors.*
$v_o(0+) = 0\,V$ *All current initially flows through capacitor (short).*	$v_o(\infty) = 0\,V$ *Power dissipated, no current.*
$\frac{d}{dt} i_L(0+) = 0\,A/s$ $v_L(0+) = L\frac{d}{dt} i_L(0+) = V_C(0+) = 0\,V$	
$\frac{d}{dt} v_C(0+) = -2\,MV/s$ $i_C(0+) = C\frac{d}{dt} v_C(0+) \quad \Rightarrow \quad \frac{d}{dt} v_C(0+) = \frac{-i_L(0+)}{C} = \frac{-2\,mA}{1\,nF} = -2\times10^6\,V/s$	
$\frac{d}{dt} v_o(0+) = -1.5\,MV/s$ *Voltage divider:* $v_o = \frac{3\,k\Omega}{1\,k\Omega + 4k\Omega} v_C \Rightarrow \frac{d}{dt} v_o(t) = \frac{3}{4}\frac{d}{dt} v_C(t)$	

(b) [6 points] Write the differential equation in terms of v_c.

KCL @ node above capacitor, (the 2 resistors are combined into R):

$$0 = i_L(t) + C\frac{d}{dt}v_C(t) + \frac{1}{R}v_C(t)$$
$$= \frac{1}{L}\int v_C(t)dt + C\frac{d}{dt}v_C(t) + \frac{1}{R}v_C(t)$$

Differentiating,

$$0 = \frac{1}{L}v_C(t) + C\frac{d^2}{dt}v_C(t) + \frac{1}{R}\frac{d}{dt}v_C(t)$$

$$0 = \frac{d^2}{dt}v_C(t) + \frac{1}{RC}\frac{d}{dt}v_C(t) + \frac{1}{LC}v_C(t)$$

(c) [6 points] What are the values of the natural frequency (ω_0) and the damping ratio (ζ)?

Damped harmonic oscillation:

$$0 = \frac{d^2}{dt}v_C(t) + 2\alpha\frac{d}{dt}v_C(t) + \omega_0^2 v_C(t)$$

$$\omega_0 = \sqrt{\frac{1}{LC}} = \sqrt{\frac{1}{(16\ mH)(1\ nF)}} = \frac{1}{\sqrt{16\times10^{-12}\ s^2}}$$
$$= 250\ krad/s$$

$$\alpha = \frac{1}{2RC} = \frac{1}{2(4\ k\Omega)(1\ nF)} = \frac{1}{8\times10^{-6}\ s}$$
$$= 125\ krad/s$$

$$\zeta = \frac{\alpha}{\omega_0} = \frac{125\ krad/s}{250\ krad/s} = 0.5 \qquad \textit{(underdamped behavior)}$$

EECS 40, Fall 2006
Prof. Chang-Hasnain
Midterm #3

November 29, 2006
Total Time Allotted: 50 minutes
Total Points: 100 pts

1. This is a closed book exam. However, you are allowed to bring one page (8.5" x 11"), single-sided notes PLUS your 1-page notes from midterm 1 and 2.
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. Slide rules are allowed.
4. SHOW all the steps on the exam. **Answers without steps will be given only a small percentage of credits.** Partial credits will be given if you have proper steps but no final answers.
5. **Remember to put down units.** Points will be taken off for answers without units.

Last (Family) Name:_____

First Name: _____

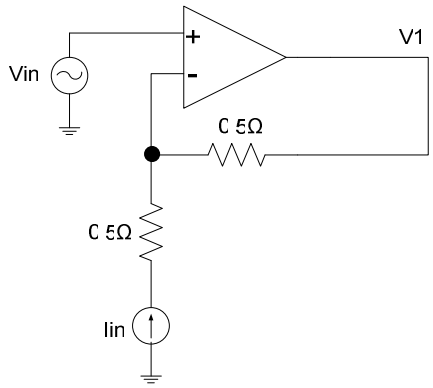
Student ID: _____Discussion Session: _____

Signature: _____

Score:	
Problem 1 (30 pts) Op Amp Circuit	
Problem 2 (40 pts): Diode Circuit	
Problem 3 (30 pts): Semiconductor Physics	
Total	

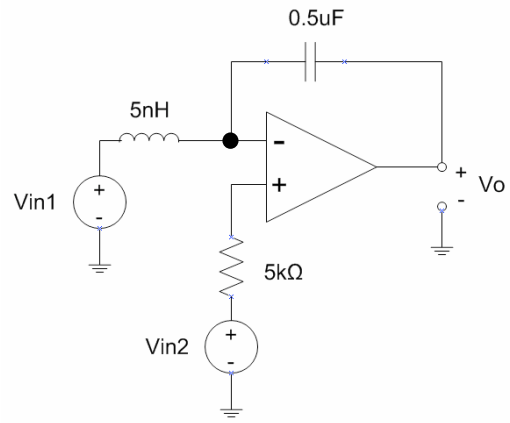
1. [30 points] Op. Amp. Circuit

a) [8 pts] Find V1 in terms of Vin and Iin.



By the summing point constraint:
$V_- = V_+ = V_{in}$
By Ohm's Law:
$V_1 = V_{in} - I_{in}(0.5\Omega)$

b) [12 pts] Find V0 in terms of Vin1, Vin2, and ω. Use complex impedances. Assume Vin1 and Vin2 are AC signals.

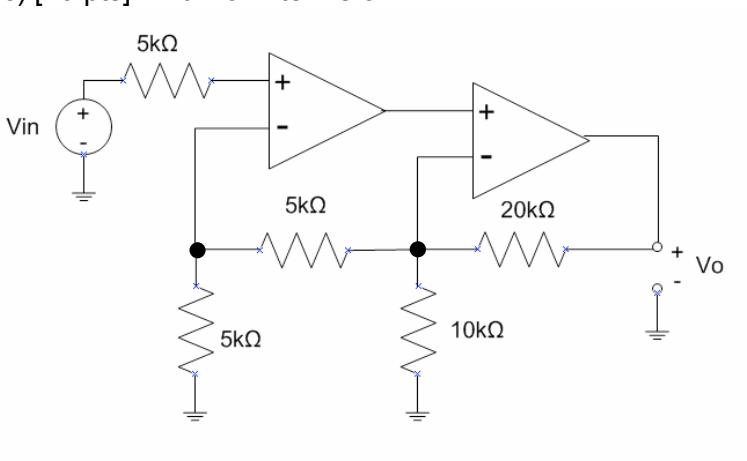


Since no current flows into the (+) terminal:
$V_+ = V_{in2}$
By the summing point constraint:
$V_- = V_{in2}$
By KCL:

$$V_0 = V_{in2} - \frac{Z_C}{Z_L}(V_{in1} - V_{in2}), Z_C = \frac{1}{j\omega 0.5\mu F}, Z_L = j\omega 5nH$$

$$V_0 = V_{in2} + \frac{1}{\omega^2 (0.5\mu F)(5nH)}(V_{in1} - V_{in2})$$

c) [10 pts] Find Vo in terms of Vin.



Since no current flows into the (+,1) terminal:
$V_{+,1} = V_{in}$
By the summing point constraint:
$V_{-,1} = V_{in}$
Since no current flows into the (-,1) terminal:
$V_{-,2} = 2(V_{-,1})$ by voltage divider across 2 resistors

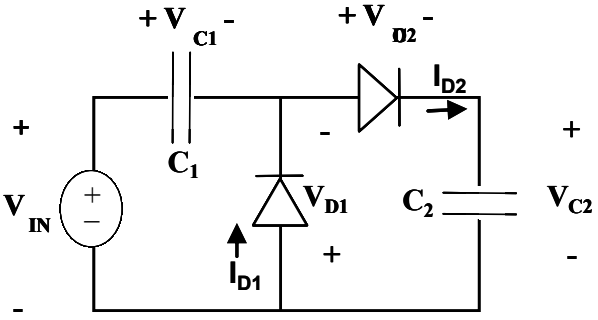
Since no current flows into the (-,2) terminal:
$V_{-,2} = V_O[5k\Omega/(5k\Omega+20k\Omega)]$
$V_O = 5V_{-,2} = 5(2V_{-,1}) = 10V_{in}$

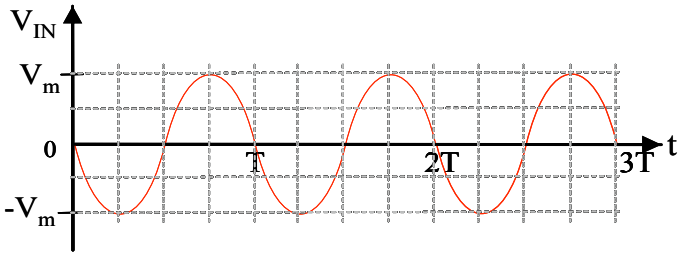
2. [40 points] Diode Circuit:
Given the following circuit and input. Assume C1 >> C2. Use the Ideal Diode model:

If $V_D < 0$, then the diode is OFF and does not pass current ($I_D=0$)
If $I_D >= 0$, then the diode is ON and $V_D=0$

V_D is the voltage drop across the diode and I_D is current through the diode.

$V_{IN}(t) = -V_m sin(2\pi t/T)$ for t>0,
and
$V_{C1}(t=0^-)= V_{C2}(t=0^-)=0$.





(a) (20 pts) **For the time period** $0 \le t \le \frac{T}{4}$

Is Diode 1 on or off? *On, Vin is -, so Diode 1 is turned on, charging C1*

V_{D1}=? *0V (on, Ideal)*

V_{C1}=? *Vin(t) , Diode 1 on grounds the node above the diode, (Vc1 = Vin – 0)*

I_{D1}=? $C_1 \frac{2\pi}{T} V_m \cos\left(\frac{2\pi t}{T}\right)$, Id1 enters negative reference of C1, $I_{D1} = -C_1 \frac{dV_{C1}}{dt}$

If this was done in the frequency domain, $I = -\frac{V_{in}}{\left(\frac{1}{j\omega C_1}\right)}$

Is Diode 2 on or off? On, node between diodes is ground (0V), Vc2 is 0V above the ground

V_{D2}=? *0V (on, Ideal)*

V_{C2}=? 0V (ground on both sides of C2)

I_{D2}=? 0 A, no current flows through capacitor, all current is through D1 and C1

(b) (20 pts) **For the period** $\frac{T}{4} \le t \le \frac{3T}{4}$

Is Diode 1 on or off? *Off, Voltage begins decreasing on + reference of diode. (At t = T/4, treat VC1+ node as ground, Voltage on both sides of diode is +Vm. This magnitude begins decreasing, shutting off diode, since VD+ < VD-)*

V_{D1}=? *-Vin + Vc1, KVL requires Vin – Vc1 + Vd1 = 0*

V_{C1}=? *-Vm,* (If you assume that C1 >> C2, the same current through both will charge C2 without significantly discharging C1)

I_{D1}=? 0A, Diode off

Is Diode 2 on or off? on

V_{D2}=? *0V (on, Ideal)*

V_{C2}=? *Vin + Vm (KVL: Vin – Vc1 – Vd2 – Vc2 = 0)*

I_{D2}=? $-C_2 \frac{2\pi}{T} V_m \cos\left(\frac{2\pi t}{T}\right),\ I_{D2} = C_2 \frac{dV_{C2}}{dt}$

In the frequency domain, $I = \frac{V_{in}}{\left(\frac{1}{j\omega C_2}\right)}$

3. [30 points] Semiconductor Physics

Suppose two doped blocks of silicon, one with an N-dopant concentration of $5x10^{18}$ cm^{-3}, and the other with a P-dopant concentration of $1x10^{17}$ cm^{-3}.

a) (5 pts) What is the concentration of majority charge carriers in N-block? What type of charge carriers is in the majority?

Answer:

$5x10^{18}$ cm^{-3}

Electrons

b) (5 pts) What is the concentration of majority charge carriers in P-block? What type of charge carriers is in the majority?

Answer:

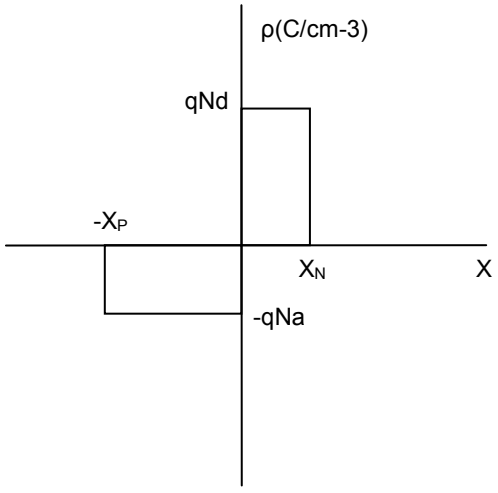
$1x10^{17}$ cm^{-3}

Holes

c) (6 pts) Suppose the two regions are connected together to form a PN junction with the junction as x = 0, p-side on the left (x<0) and n-side on the right (x>0). Use depletion approximation and assume the depletion region in the N side is $x \in [0, x_N]$ and P side is $x \in [-x_P, 0]$. Plot the charge density ρ(x) over the pn junction. What is x_N / x_P?

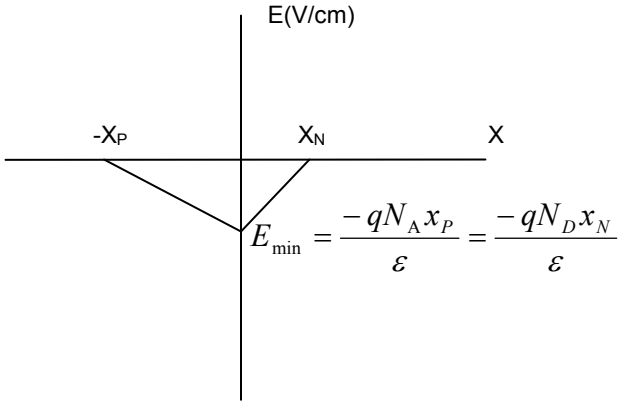
Answer:

$x_N / x_P = Na/Nd = 1x10^{17}/5x10^{18} = 0.02$



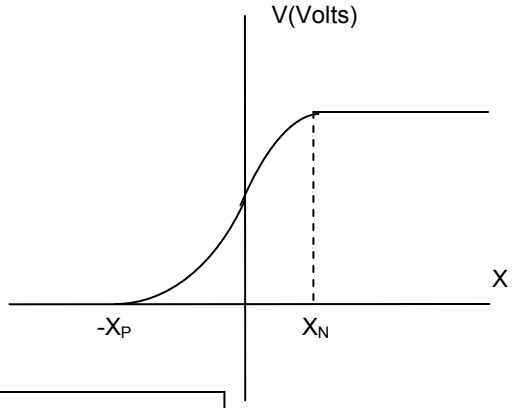
d) (7 pts) Plot electric field *E*(x) vs. distance x. Assuming the ε is the permittivity of the material Label your plot. Write E_{max} as a function of x_N.

Answer:



e) (7 pts) Plot electrostatic potential V(x) vs. distance x. Assume the reference point V=0 at p-side x<<-x_p. Label your plot and write V_{max} as a function of x_N.

Answer:



$$V_{\max} = \frac{qN_D(x_N)^2}{2\varepsilon} + \frac{qN_A(x_P)^2}{2\varepsilon}$$

where

$$x_P = \frac{N_D x_N}{N_A}$$

so

$$V_{\max} = \frac{qN_D(x_N)^2}{2\varepsilon}\left(1 + \frac{N_D}{N_A}\right)$$

Quiz #1, EECS 40, Fall 2006
Total: 100 pts and 20 pts Bonus

Last (Family) Name: Perfect First Name: Peter

Student ID: 314159265 Discussion Session: 000

1. (14 pts) Consider a transfer function, $H(f)=\dfrac{-jQ\left(\dfrac{f_0}{f}\right)}{1+jQ\left(\dfrac{f}{f_0}-\dfrac{f_0}{f}\right)}$

(a) What is $|H(f)|^2$?

$$|H(f)|^2=\frac{\left(Q\frac{f_0}{f}\right)^2}{1^2+Q^2\left(\frac{f}{f_0}-\frac{f_0}{f}\right)^2}$$

(b) What is the phase $\angle H(f)$?

$$\angle\left(-jQ\frac{f_0}{f}\right)=-\frac{\pi}{2}$$

$$\angle\left(1+jQ\left(\frac{f}{f_0}-\frac{f_0}{f}\right)\right)=\tan^{-1}\left(Q\left(\frac{f}{f_0}-\frac{f_0}{f}\right)\right)$$

$$\angle H(f)=-\frac{\pi}{2}-\tan^{-1}\left(Q\left(\frac{f}{f_0}-\frac{f_0}{f}\right)\right)$$

2. (50 pts) Bode Magnitude Plot: Use the same transfer function in 1, $y=10\log|H(f)|^2$

(a) What is the break frequency (or resonance frequency in the text book)?

$f_B=f_0$

(b) What is y at the break frequency?

$$y = 10\log|H(f)|^2 = 10\log\left(\frac{\left(Q\frac{f_0}{f_0}\right)^2}{1^2 + Q^2\left(\frac{f_0}{f_0} - \frac{f_0}{f_0}\right)^2}\right)$$
$$= 10\log\left(\frac{Q^2}{1+Q^2(0)}\right) = 10\log\left(Q^2\right)$$
$$= 20\log Q$$

(c) What is y for very small f?

The f term in the numerator is by itself, cannot be ignored. The f^{-1} term in the denominator dominates at very small f.

$$y = 10\log\frac{\left(Q\frac{f_0}{f}\right)^2}{Q^2\left(\frac{f_0}{f}\right)^2} = 10\log 1 = 0\ dB$$

(d) What is y for very large f? What is the slope of this portion?

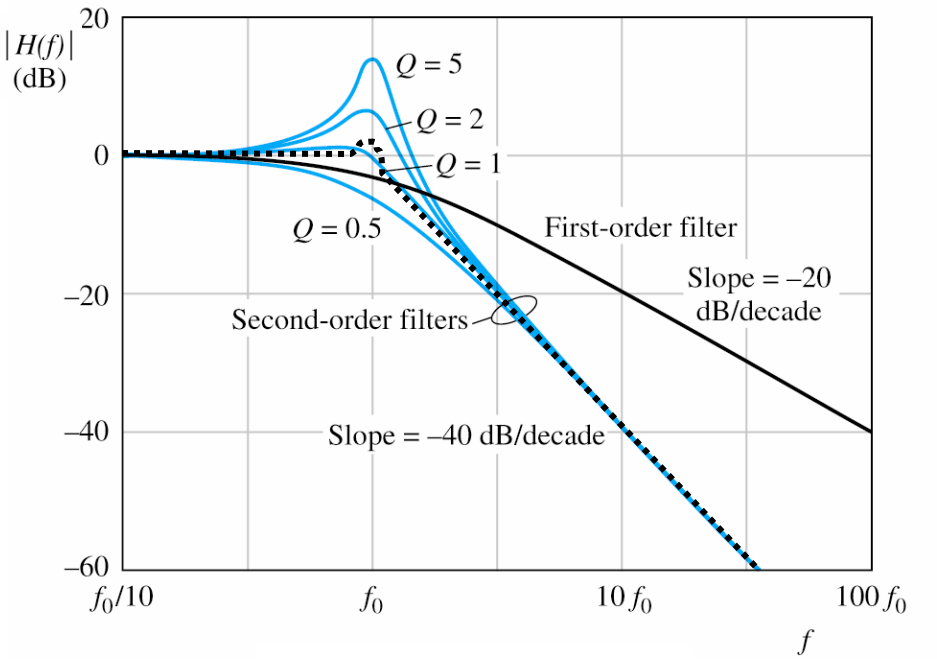
Again, we cannot ignore the lone f term in the numerator. At large f, the f^{-1} term in the denominator becomes 0. The f term dominates.

$$y = 10\log\frac{\left(Q\frac{f_0}{f}\right)^2}{Q^2\left(\frac{f}{f_0}\right)^2} = 10\log\left(\frac{f_0}{f}\right)^4$$
$$= 40\log f_0 - 40\log f$$

Thus, the slope is -40 dB/decade.

(e) Sketch the Bode magnitude plot.

The figure below shows the Bode magnitude plot (blue lines) for different values of Q. The humps at f_0 have the value 20 log Q. The thick dashed line represents the approximate values, emphasizing the linear portions of the Bode plot.



3. (36 pts) Bode Magnitude Plot: Use the same transfer function in 1, let $y = 10\log|H(f)|^2$

(a) At the break frequency, $\angle H(f)$ =?

$$\angle H(f) = -\frac{\pi}{2} - \tan^{-1}\left(Q\left(\frac{f_0}{f_0} - \frac{f_0}{f_0}\right)\right)$$
$$= -\frac{\pi}{2} - \tan^{-1}(0) = -\frac{\pi}{2}$$

(b) In radians, what does $\angle H(f)$ approach as $f \to \infty$?

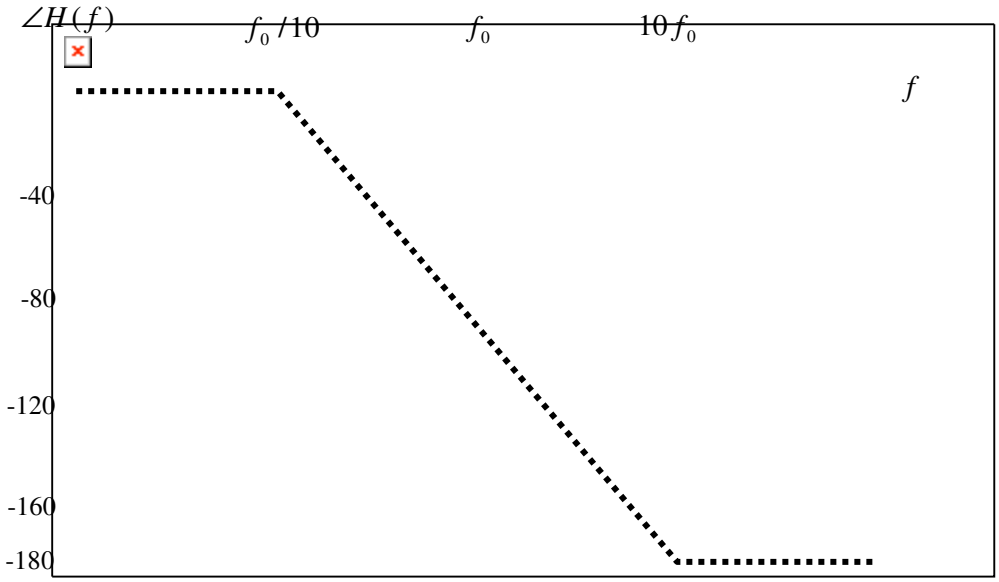
$$\angle H(f) = -\frac{\pi}{2} - \tan^{-1}(\infty)$$
$$= -\frac{\pi}{2} - \frac{\pi}{2} = -\pi$$

(c) In radians, what does $\angle H(f)$ approach as $f \to 0$?

$$\angle H(f) = -\frac{\pi}{2} - \tan^{-1}(-\infty)$$
$$= -\frac{\pi}{2} - \left(-\frac{\pi}{2}\right) = 0$$

(d) Sketch the Bode Phase plot.

The curve shows the actual values, the dotted line is the Bode approximation.

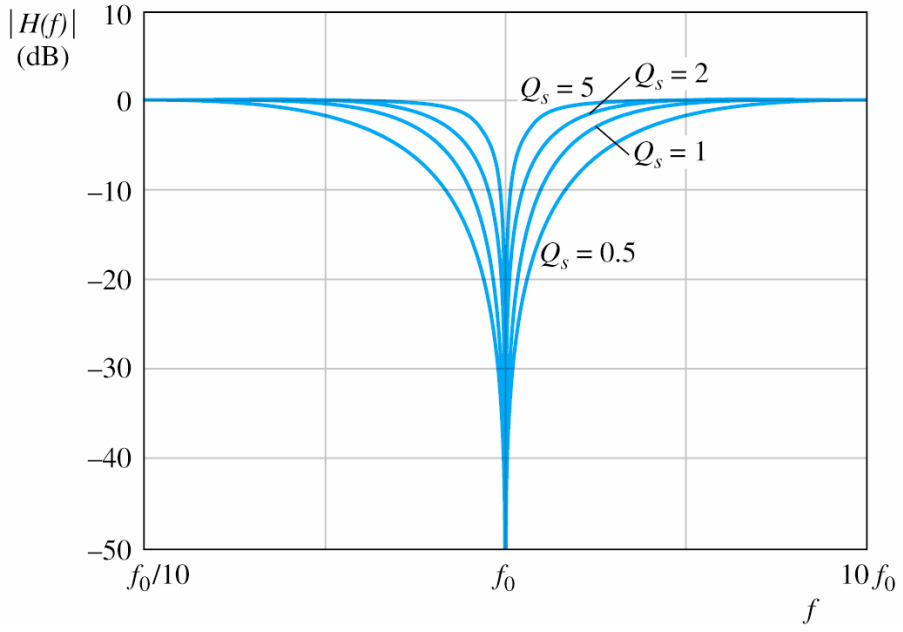


3. (20 pts) Bonus: Given the transfer function $H(f) = \dfrac{jQ(\frac{f}{f_0} - \frac{f_0}{f})}{1 + jQ(\frac{f}{f_0} - \frac{f_0}{f})}$

What kind of filter is this? Sketch the Bode Magnitude Plot.

This is a notch filter, with V_{out} taken across the L and C in a series RLC circuit.

The slope of the response does not take a constant asymptotic slope around the resonant frequency, but does approach $-\infty$ at the resonant frequency. The width of the stop band decreases with higher Q.



EECS 40, Fall 2006
Prof. Chang-Hasnain
Final Exam

December 12, 2006
Total Time Allotted: 180 minutes
Total Points: 350 pts

1. This is a closed book exam. However, you are allowed to bring one page (8.5" x 11"), single-sided notes PLUS your 1-page notes from midterm 1, 2 and 3.
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. Slide rules are allowed.
4. SHOW all the steps on the exam. **Answers without steps will be given only a small percentage of credits.** Partial credits will be given if you have proper steps but no final answers.
5. **Remember to put down units.** Points will be taken off for answers without units.

Last (Family) Name:_____

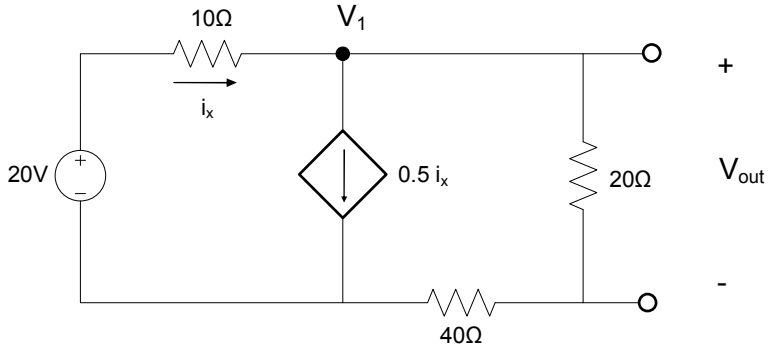
First Name: _____

Student ID: _____Discussion Session: _____

Signature: _____

	Score
1. [30 pts] Thevenin Equivalent Circuit 2. [30 pts] Equivalent Impedances 3. [50 pts] Semiconductor Device Physics 4. [40 pts] Diodes/Op-Amps 5. [60 pts] Second Order Circuits 6. [140 pts] MOSFET	
TOTAL	

1. [30pts] Thevenin Equivalent Circuit



a) What is the current i_x through the 10Ω resistor?

$$KVL: 20V - (i_x \cdot 10\Omega) - (0.5i_x \cdot 20\Omega) - (0.5i_x \cdot 40\Omega) = 0$$
$$20V = 10\Omega \cdot i_x + 30\Omega \cdot i_x$$
$$i_x = \left(\frac{20V}{40\Omega}\right) = 0.5A$$

b) Find V_1 when there is no load connected to the ports a and b (as depicted by the figure above).

Voltage drop across the 2 resistors:
$$V_1 = (0.5i_x)(20\Omega + 40\Omega)$$
$$= (0.25A)(60\Omega)$$
$$= 15V$$

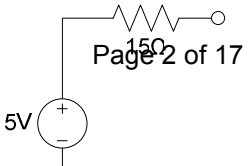
c) What is the open circuit voltage across a-b, V_{oc}?

Voltage across the 20Ω resistor:
$$V_{oc} = (0.5i_x)(20\Omega)$$
$$= (0.25A)(20\Omega)$$
$$= 5V$$

d) What is the short circuit current across a-b, I_{sc}?

$0.5i_x$ flows directly from V_1 to 40Ω resistor, KVL now reads:
$$20V - (i_x \cdot 10\Omega) - (0.5i_x \cdot 40\Omega) = 0$$
$$20V = 10\Omega \cdot i_x + 20\Omega \cdot i_x$$
$$i_x = \left(\frac{20V}{30\Omega}\right) = \frac{2}{3}A$$
$$i_{sc} = 0.5i_x = \frac{1}{3}A$$

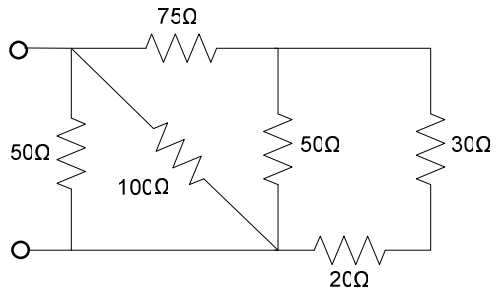
e) What is R_{th}? Draw the Thevenin equivalent circuit.



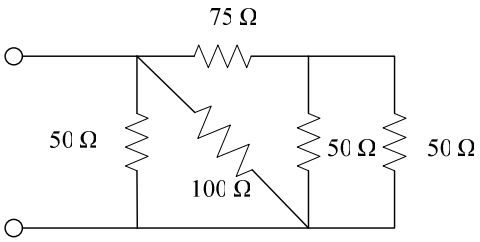
$$R_{Th} = \frac{V_{oc}}{i_{sc}} = \frac{5V}{1/3A} = 15\Omega$$

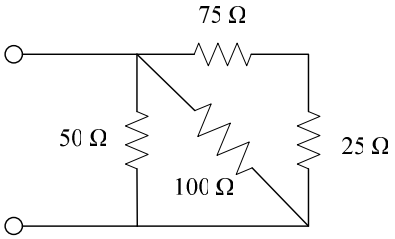
2. [30pts] Equivalent Impedances

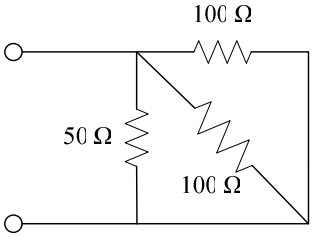
a) What is Req across the indicated nodes?

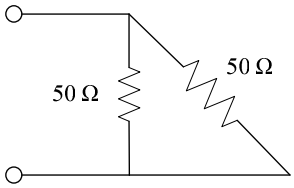


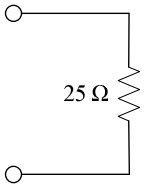
Break down 2 resistors at a time:





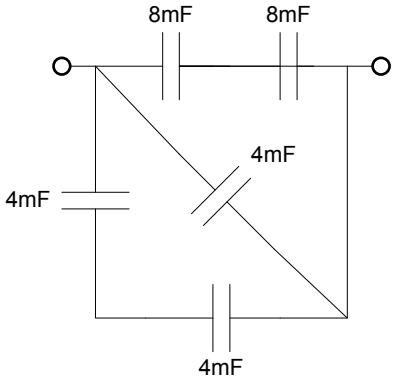




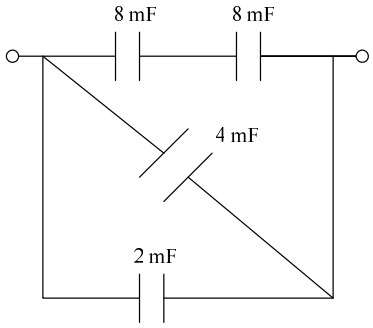


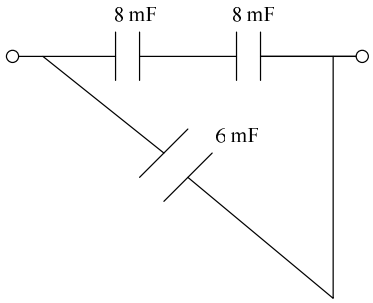
$R_{eq} = 25\,\Omega$

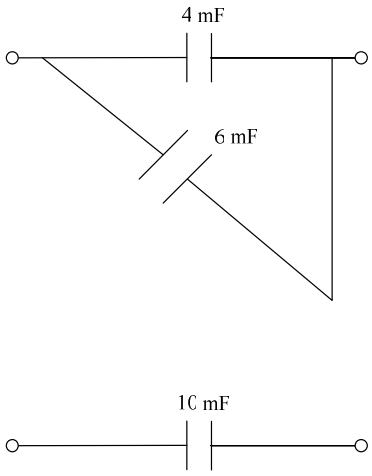
b) What is Zeq across the indicated nodes?



Break down 2 capacitors at a time:





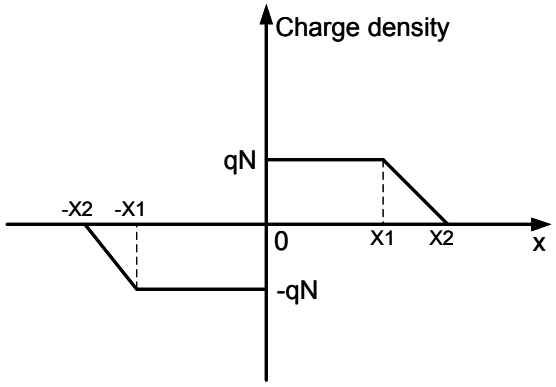


$$C_{eq} = 10mF$$

$$Z_{eq} = \frac{1}{j\omega C_{eq}} = \frac{100}{j\omega}\Omega \;\; or \;\; \frac{1}{10j\omega}k\Omega$$

3. [50 pts] Semiconductor Device Physics

Suppose we have the charge density distribution given by the figure. The permittivity of the material is ε.



a) (5 pts) Which side is p side and which side n side?

Left side (x<0): p
Right side (x>0): n

b) (5 pts) What is the direction of the built-in electric field?

The built-in electric field is in –x direction

c) (10 pts) What is the value for the electric field E(x) for $x \le -x_2$ and $x_2 \le x$?

E(x)=0 for both regions.

d) (10 pts) What is E(x) for $-x_2 \le x \le -x_1$?

From the figure, we can write down the expression for charge density in this region

$\rho(x) = \dfrac{qN}{x_1 - x_2}(x + x_2)$.

According to Gauss's law

$\dfrac{d}{dx}E(x) = \dfrac{\rho(x)}{\varepsilon}$,

we can arrive at the following result by carrying out the integration

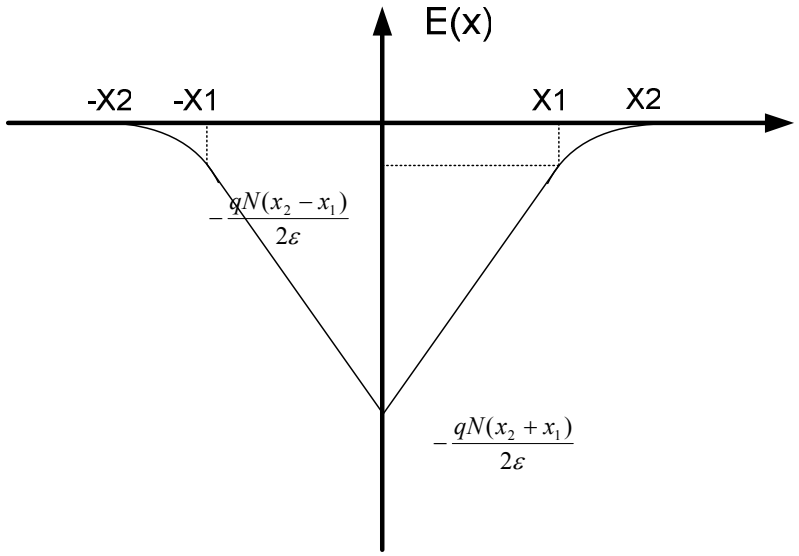
$E(x) = \dfrac{qN}{\varepsilon(x_1 - x_2)}\dfrac{(x + x_2)^2}{2}$

e) (10 pts) What is E_{max}? Here E_{max} represents the maximum absolute value.

The electric field reaches its maximum value at the x=0. The magnitude can be calculated by evaluating the area enveloped by the curve on the left hand side, and divide the area by ε. Therefore,

$$E_{\max} = \frac{qN(x_2 - x_1)}{2\varepsilon} + \frac{qNx_1}{\varepsilon}$$
$$= \frac{qN(x_2 + x_1)}{2\varepsilon}$$

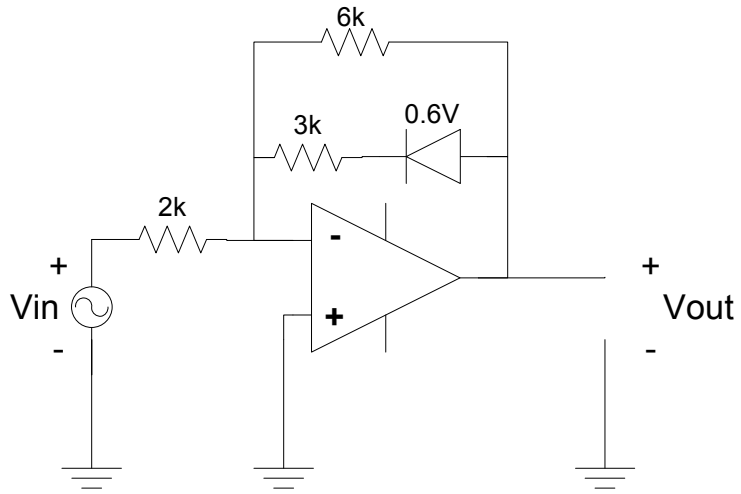
f) (10 pts) Sketch E(x) vs. X. Label your plot. Also describe the curves.



E(x) is symmetrical with respect to x. It is a quadratic function when $x \in [-x_2,-x_1] \cup [x_1,x_2]$, a linear function when $x \in [-x_1,0] \cup [0,x_1]$, and zero anywhere else.

4. [40 pts] Diodes/Op-Amps

Assume the op-amp is ideal.
Use the large-signal model for the diode with turn-on voltage of 0.6V.



(a) (10 pts) When the diode is on, what is V_{out} as a function of V_{in}?

When the diode is on, it acts like a 0.6V source.
By the summing-point constraint, V- = V+ = 0V.
By applying KCL at V-, we get Vin/2k + Vout/6k + (Vout-0.6V)/3k = 0V.
Solving yields Vout = 0.4 - Vin.

(b) (10 pts) When the diode is off, what is V_{out} as a function of V_{in}?

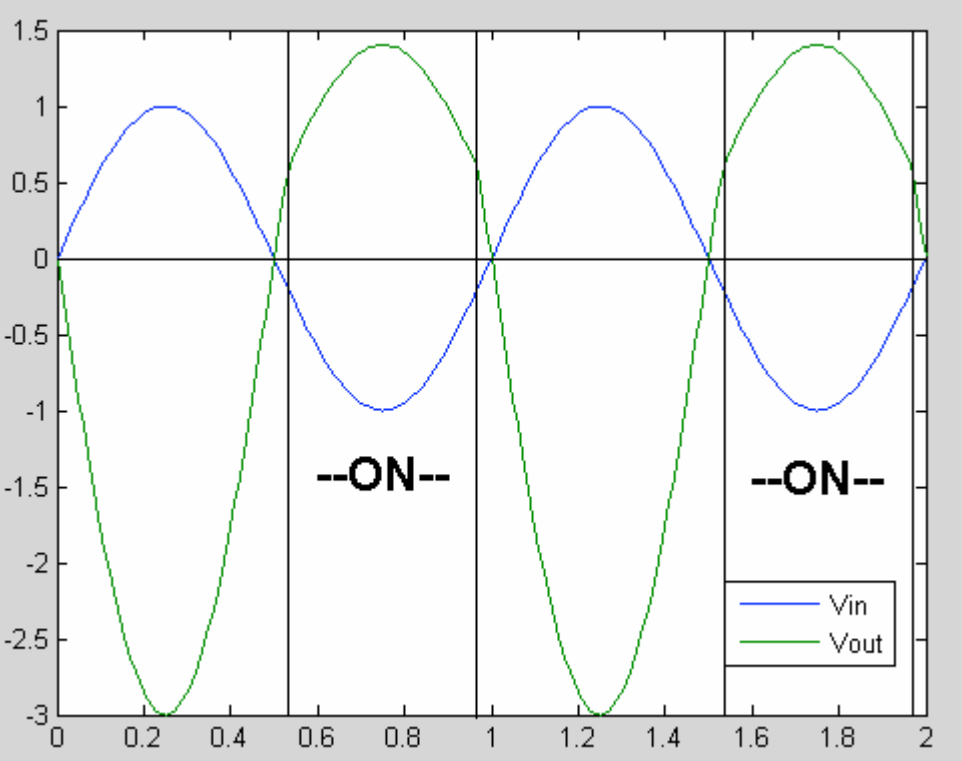
When the diode is off, it acts as a open circuit.
Now KCL at V- gives Vin/2k + Vout/6k = 0V.
Solving yields Vout = -3Vin.
Also notice that this is just a regular inverting amplifier.

(c) (5 pts) For what range of V_{in} will the diode be on?

For the diode to be on, there must be positive current through the diode or, alternatively, through the 3k resistor (since they are in series).
This means there must be a voltage drop across the resistor must be positive.
So that gives us Vout - 0.6V > 0V.
Substituting in our expression from (a), we get 0.4V - Vin - 0.6V > 0V.
Solving yields Vin < -0.2V.

Alternatively, we can see that for the diode to be off, we need the diode voltage to be less than the threshold of 0.6V, which gives us Vout -0 < 0.6V.
Plugging in our expression from (b) gives us -3Vin < 0.6V.
Solving yields Vin > -0.2V.
This means the diode will be on for Vin < -0.2V

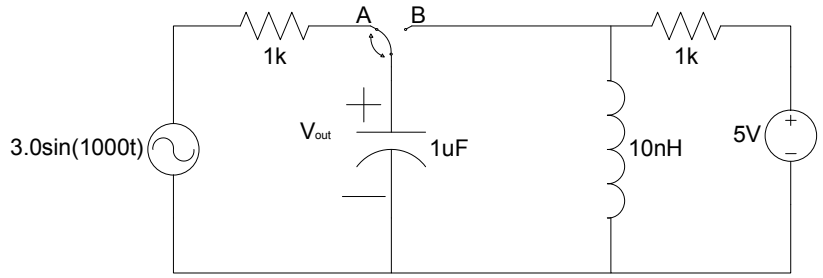
(d) (15 pts) Complete the following plot for Vout. Indicate which regions the diode is on. Make sure to label your axes.



The key points are that the diode switches when Vin = -0.2V and Vout = 0.6V.
The negative peak is -3V, and the positive peak is 1.4V.
Also notice that When Vin = 0V, Vout = 0V.

5. [60 pts] Second Order Circuits

Suppose the following circuit. Assume that the switch has been in position A for an infinitely long time before t = 0. $v_{in} = 3.0\sin(1000t)$



a) (10 pts) Write the input voltage in the Phasor format, $\mathbf{V_{in}}$?

Noting the input is a sin, we apply the identity:

$\cos(\omega t - \pi/2) = \sin(\omega t)$

Thus, $V_{in} = 3.0\angle -\frac{\pi}{2}$

This angle is equivalent to -90 degrees.

b) (10 pts) Assuming an AC steady state condition and the switch is in the A position. What is the output voltage in Phasor format, $\mathbf{V_{out}}$?

$$V_{out} = \frac{Z_c}{Z_c + R}V_{in} = \frac{1}{1 + j\omega RC}V_{in} = \frac{1}{1+j}3.0\angle -\frac{\pi}{2} = \frac{3.0\angle -\frac{\pi}{2}}{\sqrt{2}\angle\frac{\pi}{4}} = \frac{3}{\sqrt{2}}\angle -\frac{3\pi}{4}$$

c) (10 pts) What is the output voltage in time domain, $v_{out}(t)$?

By inspection, $V_{out} = \frac{3}{\sqrt{2}}\cos\left(1000t - \frac{3\pi}{4}\right)$

This angle is equivalent to -135 degrees or +225 degrees.

d) (20 pts) At time t = π ms, the switch flips from position A to B, disconnecting the AC source from the output. Provide a differential equation describing v_{out} with respect to time. The solution should be a second-order differential equation of $V_{out.}$

$$\frac{V_{out} - 5V}{R} + C\frac{dV_{out}}{dt} + \frac{1}{L}\int V_{out}\,dt = 0$$

Taking the derivative,

$$\frac{d^2V_{out}}{dt^2} + \frac{1}{RC}\frac{dV_{out}}{dt} + \frac{1}{LC}V_{out} = 0$$

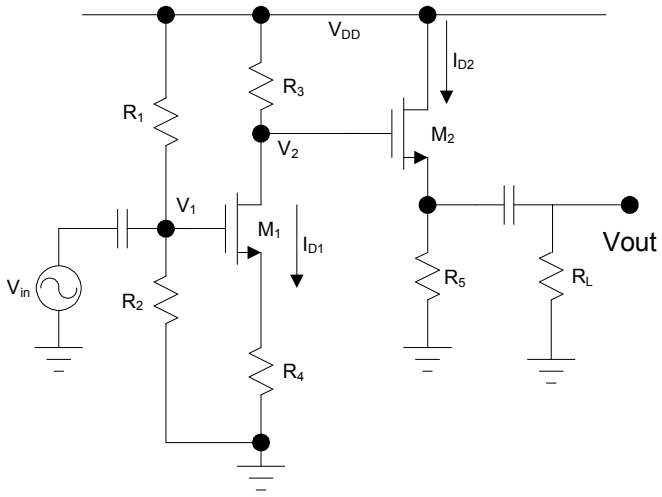
Plugging in values,

$$\frac{d^2V_{out}}{dt^2} + 10^3\frac{dV_{out}}{dt} + 10^{14}V_{out} = 0$$

e) (10 pts) What is the V_{out} at very large t?
In steady state, the inductor becomes a short circuit (while it is in parallel with the capacitor).
So, $V_{out} \rightarrow 0V$.

6. [140 pts] MOSFET

In the circuit below, V_{DD}=5V, and both transistors are identical with V_{to}=1V, K=0.1 mA/V^2.



(A) (50 pts) DC analysis

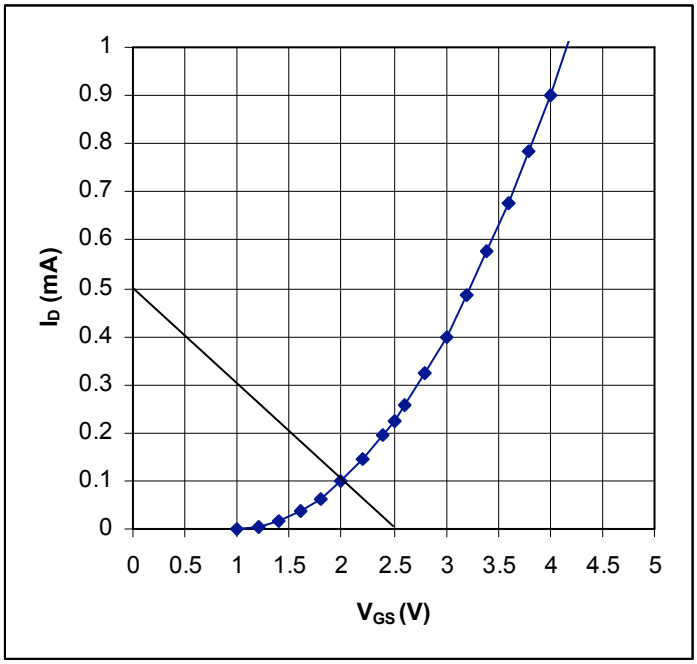
a) (5 pts) What is V_1? Given $R_1 = R_2 = 5k\Omega$

$$V_1 = Vdd\frac{R2}{R1+R2} = 5\frac{5k\Omega}{5k\Omega+5k\Omega} = 2.5V$$

b) (10 pts) What is I_{D1}? Given $R_3 = R_4 = 5k\Omega$. Write down the necessary equation(s) and draw load line in the following graph.

$$V_1 - I_D R_4 = V_{GS}$$
$$2.5 - I_D * 5k = V_{GS}$$
$$I_D = \frac{2.5 - V_{GS}}{5k} = \frac{2.5 - V_{GS}}{5}\,mA$$

From the Load Line
I_D = 0.1 mA
Vgs = 2V



c) (5 pts) Which mode is transistor M1 in?

Saturation

d) (5 pts) What is V_{DS1}?

$$V_{DS1} = Vdd - I_{D1}R3 - I_{D1}R4 = 5 - .1m * 5k - .1m * 5k = 5 - 0.5 - 0.5 = 4V$$

e) (5 pts) What is V_2?

$$V_{DS1} = Vdd - I_{D1}R3 = 5 - .1m * 5k = 4.5V$$

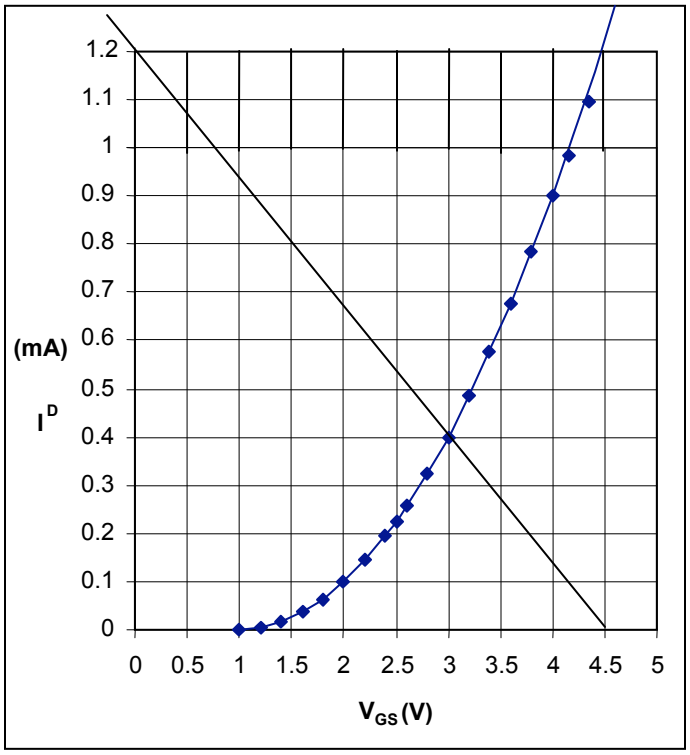
f) (5 pts) For transistor M2, write down the equations for V_{DS2} and V_{GS2}. What mode is this transistor in?

$$V_{DS1} = Vdd - I_{D2}R5$$
$$V_{GS2} = 4.5 - I_{D2}R5$$

The transistor is also in saturation.

g) (10 pts) What is I_{D2}? Given R_5 = 3.75kΩ. Write down the necessary equation(s) and draw load line in the following graph.

$$V_{GS2} = V_2 - I_{D2}R5$$
$$I_{D2} = \frac{4.5 - V_{GS2}}{3.75k} = \frac{4.5 - V_{GS2}}{3.75} mA$$
$$I_{D2} = 0.4mA @ V_{GS} = 3V$$

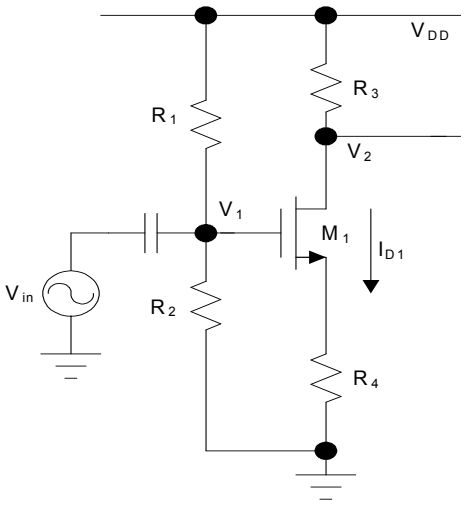


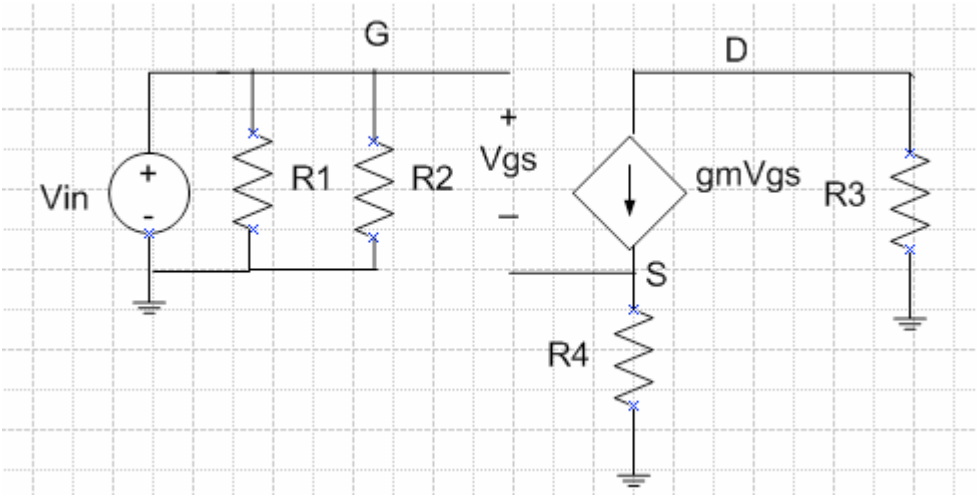
h) (5 pts) What is V_{DS2}?

$$V_{DS1} = Vdd - I_{D1}R5 = 5 - .4m * 3.75k = 3.5V$$

(B) (90 pts) AC small-signal analysis:

a) (20 pts) For transistor M1, the small signal gain $A_{V1} = V_2/V_{in}$. Draw the small signal model for M1. Consider $r_d \to \infty$ for both transistors.





b) (15 pts) What is A_{V1}?

To find Av, we first find GM and then find Rout.
To find GM, we short the output (V2) and apply a test voltage at the input.
Applying KCL at V2 and VS (source of M1):

$$\frac{Vs}{R4} - gm(Vt - Vs) = 0$$

$$Vs = \frac{gmR4 * Vt}{1 + gmR4}$$

$$Iout + gm(Vt - Vs) = 0$$

$$Iout = -gm(Vt - \frac{gmR4 * Vt}{1 + gmR4}) = -gmVt(1 - \frac{gmR4 * Vt}{1 + gmR4}) = -gmVt(\frac{1 + gmR4}{1 + gmR4} - \frac{gmR4}{1 + gmR4})$$

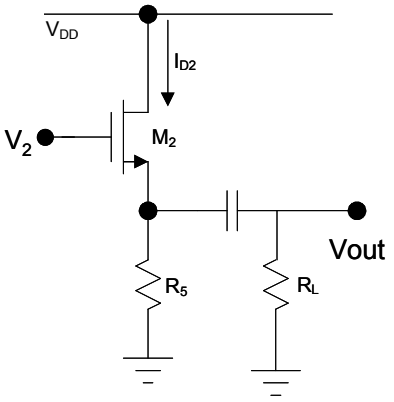
$$Iout = \frac{-gmVt}{1 + gmR4}$$

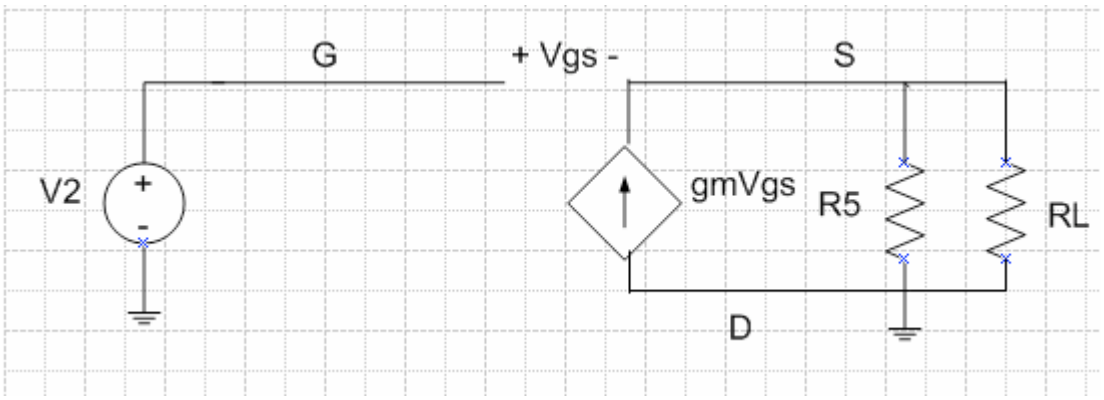
$$GM = \frac{Iout}{Vt} = \frac{-gm}{1 + gmR4}$$

Ro is simply R3, because rd is infinity.
Therefore the gain Av1:

Av1 = GM*Ro = $-\frac{gmR3}{1 + gmR4}$

c) (20 pts) For transistor M2, the small signal gain $A_{V2} = V_{out}/V_2$. Draw the small signal model for M2.





d) (15 pts) What is A_{V2}?

To find the gain, we find GM and Ro.
If we short the output VS (the source of M2), and apply a test voltage at the gate (V2), we see that GM = Iout / Vt = gm.

$$Iout - gm(Vgs) = Iout - gm(V2 - 0)$$

$$Iout = gmV2$$

$$GM2 = \frac{Iout}{V2} = gm$$

To find Ro, we short the input (V2) and apply a test voltage at the output VS. Then we measure the current flowing into the output node.
First, combine R5 and RL together to form RL'.

Using KCL:

$$-Iout + \frac{Vt}{RL'} - gm(0 - Vt) = 0$$

$$Iout = Vt(\frac{1}{RL'} + gm)$$

$$RO2 = \frac{Vt}{Iout} = \frac{1}{(\frac{1}{RL'} + gm)} = \frac{RL'}{1 + gmRL'}$$

Av2=GM2 * RO2

Av2= $\frac{gmRL'}{1 + gmRL'}$

e) (5 pts) What is the overall gain $A_{V2} = V_{out}/V_{in}$?

Av = Av1 * Av2 = $-\frac{gmR3}{1 + gmR4} \frac{gmRL'}{1 + gmRL'}$

f) (5 pts) What is the input impedance of the overall circuit?

The input impedance is simply R1 || R2 because the input impedance of a NMOS is infinity.
Rin = R1 || R2 = 2.5kΩ

g) (10 pts) What is the output impedance of the overall circuit?

As found above in part d), the output impedance of the overall circuit is the same as the output impedance of the second stage (consisting of M2).

Zo = RL'|| (1/gm) = $\frac{RL'}{1 + gmRL'}$

Midterm 1 Solution for EE40 Sp 2006

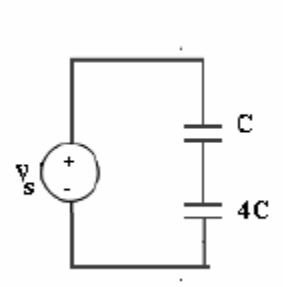
(Prepared by Josh Hug, jhug@eecs.berkeley.edu)

1. Resistive Circuits and Capacitors
   a. This is most easily solved by using the current divider rule:
      $I_7 = I_s/8$
   b. If we treat the two resistances R in parallel as a ½R ohm resistor, we can use the voltage divider rule:
      $V_1 = V_s * ½ / (½ + 1) * V_s = 1/3\ V_s$
   c. At the node of interest, we have 2I current coming in from the right, and I current leaving from the bottom, so we know that there must be I current leaving through the top. Thus, by Ohm's law, we know that $V_1 = 10+I*5$. Furthermore, we also know by Ohm's law that $V_1 = 10I$. Using these two equations, we can find that $V_1 = 20$ Volts.

      Another way to solve this problem is to use KCL at the V_1 node:

      $$\frac{V_1 - 10}{5} + \frac{V_1}{10} - \frac{2V_1}{10} = 0$$
      $$2V_1 - 20 + V_1 - 2V_1 = 0$$
      $$V_1 = 20 Volts$$

   d. We know that for two capacitors in series, the charges are equal, and for two capacitors in parallel, the voltages are equal. If we treat the pair of 2C capacitors in parallel as a single 4C capacitor. Then we have the following equivalent circuit:



      We know that $Q_C = Q_{4C}$, and $V_C + V_{4C} = V_S$, $Q_C = C*V_C$, and $Q_{4C} = 4C*V_{4C}$.

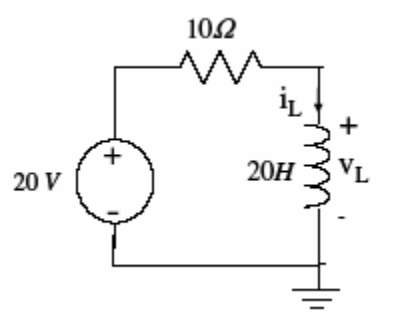
      From $Q_C = C*V_C$, $Q_{4C} = 4C*V_{4C}$, and $Q_C = Q_{4C}$, we know that $V_C = 4V_{4C}$

      Thus $4V_{4C} + V_{4C} = V_S$, so $V_{4C} = 1/5 * V_S$, and $V_C = 4/5 * V_S$

      $Q_C = Q_{4C} = 4C/5 * V_S$

2. One solution is to use the trick from homework 4.

   For $0 < t < 2$ sec, we have the following circuit:



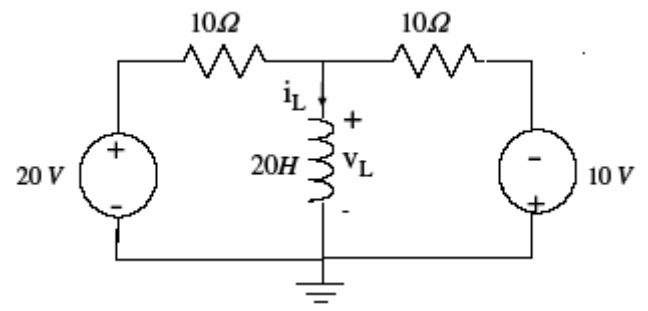
First we note that $i_L(0^-) = i_L(0^+) = 0$, and $i_L(\infty) = 20/10 = 2$ Amps

Next, we find the Thevenin resistance that the inductor sees, which is trivially 10 Ohms. This gives us the time constant L/R = 20/10 = 2 seconds

Now that we know the initial current (0 Amps), the steady state voltage (2 Amps), and the time constant (2 seconds), we use the shortcut from Homework 4 and get:

$$I_L(t) = I_f - (I_f - I_i)e^{-t/\tau}$$
$$= 2 - 2e^{-t/2\,\text{sec}}\ Amps$$

For t > 2 sec, we have the following circuit:



First we note that $i_L(2^-) = i_L(2^+) = 2 - 2e^{-2/2} = 2 - 2e^{-1} = 1.26$ Amps

To find $i_L(\infty)$, we can use superposition. From the 20 volt source, $i_L(\infty)$ is increased by 2 Amps. From the 10 volt source, $i_L(\infty)$ is decreased by 1 amp. Thus, $i_L(\infty) = 2 - 1 = 1$ Amp.

Next, we find the Thevenin resistance that the inductor sees by zeroing out the independent sources, yielding the following circuit:

This is just a 10 ohm resistor in parallel with another 10 ohm resistor, which means that the resistance the inductor sees is 5 ohms.

Thus our time constant is 20/5=4 seconds.

So, again using the trick from homework 4, we have

$$I_L(t) = I_f - (I_f - I_i)e^{-(t-2)/\tau}$$
$$= 1 - (1 - 1.26)e^{-(t-2)/4}$$
$$= 1 + 0.26e^{-(t-2\,\text{sec})/4\,\text{sec}}\,Amps$$

Another possible solution is to write the differential equations in both cases and solve.

For the first case, we can use KVL to find that:

$$10 - 10I_L - 20I_L' = 0$$
$$2 - I_L - 2I_L' = 0$$
$$I_L + 2I_L' = 2$$

We first find the complementary solution $I_C(t) = Ke^{-t/\tau}$. Since we have our equation in the form $I_L + \tau I_L' = f(t)$, we know that $I_C(t) = Ke^{-t/2\,\text{sec}}\,Amps$.

Next we can find the particular solution by guessing that our solution is of the form $I_P(t) = A * f(t) + B * f'(t) = A$. Plugging this into our differential equation above, we get that A+0=2, or A=2.

Finally, we know that I(0)=0, so we find I(0)= $I_C(0) + I_P(0) = K + 2 = 0$, or K=-2. Thus, our final solution for 0 < t < 2 is $I(t) = 2 - 2e^{-t/2\,\text{sec}}\,Amps$.

For the second part of the problem, we write a new differential equation using KCL at our node of interest. (We could also write two KVL equations and add them).

Doing this, we obtain:

$$\frac{V_L - 20}{10} + \frac{V_L + 10}{10} + \int \frac{V_L}{20} = 0$$
$$V_L = LI_L'$$
$$\frac{20I_L' - 20}{10} + \frac{20I_L' + 10}{10} + \frac{20I_L}{20} = 0$$
$$2I_L' - 2 + 2I_L' + 1 + I_L = 0$$
$$4I_L' - 1 + I_L = 0$$
$$4I_L' + I_L = 1$$

Since our equation is in the form $I_L + \tau I_L' = f(t)$, we know that our complementary solution is of the form $I_{L_C}(t) = Ke^{-(t-2\sec)/4\sec} Amps$.

Next we find the particular solution. As above, we assume that $I_{L_P}(t) = A$, and plug this into our differential equation, finding that A=1.

Now we add our particular and complementary solution and have that $I_L = Ke^{-(t-2)/4} + 1$. To find K, we know that $I_L(2) = 2 - 2e^{-1} = 1.26A$, so $I_L(2) = Ke^{-(2-2)/4} + 1 = K + 1 = 1.26A$, and therefore K=0.26A.

Thus our final solution is $I_L(t) = 1 + 0.26e^{-(t-2\sec)/4\sec} Amps$

There are many more possible solutions, such as using separation of variables, etc,

3.

a. For t < 0, the circuit has been closed for a long time, and since we have a DC source, we can perform DC steady state analysis. We treat the capacitor as an open circuit, and the inductor like a short. Thus, we find that $I_L = 5/500{,}000 = 10^{-5} Amps$, and since the inductor acts like a short, $V_C = 0$ Volts.
b. One method is to write KCL at the node, take the derivative of both sides, and reorganize the terms, as shown below:

$$\frac{V_L - \cos(t)}{R} + CV_L' + \int \frac{V_L}{L} = 0$$
$$\frac{V_L' + \sin(t)}{R} + CV_L'' + \frac{V_L}{L} = 0$$
$$\frac{V_L'}{RC} + V_L'' + \frac{V_L}{LC} = -\frac{\sin(t)}{RC}$$
$$V_L'' + 2V_L' + V_L = -2\sin(t)$$

c. Since, our equation is in the form $\frac{d^2x(t)}{dt^2} + 2\alpha\frac{dx(t)}{dt} + \omega_0^2 x(t) = f(t)$, we know that

$$\alpha = 1,\ \omega_0 = 1,\ \zeta = \frac{\alpha}{\omega_0} = \frac{1}{1} = 1$$

Therefore, the complementary/transient solution is:

$$V_C(t) = K_1 e^{-\alpha t} + K_2 t e^{-\alpha t} \text{ Volts}$$

d. Critically damped
e. We assume a solution of the form $V_p(t) = A\cos(t) + B\sin(t)$

$V_p(t) = A\cos(t) + B\sin(t)$

$V_P'(t) = -A\sin(t) + B\cos(t)$

$V_P''(t) = -A\cos(t) - B\sin(t)$

Then we plug them into our equation from part b, and get:

$$-A\cos(t) - B\sin(t) - 2A\sin(t) + 2B\cos(t) + A\cos(t) + B\sin(t) = -2\sin(t)$$

By collecting sine and cosine terms, we find the following:
-A+2B+A=0
-B-2A+B = -2

From the first equation we find that B=0.

Plugging B=0 into the second equation, we get -2A=-2, or A=1.

Thus our particular solution $V_p(t) = \cos(t)$

f. We obtain the complete solution by adding the particular solution and the complementary solution, so we have:

$$V(t) = K_1 e^{-t} + K_2 t e^{-t} + \cos(t)$$

To find the constants, we can first use the initial condition v(0)=0, and obtain:

$V(0) = K_1 e^0 + K_2 0 e^0 + \cos(0) = 0$

$K_1 + 1 = 0$

$K_1 = -1$

To find K_2, we know that $i_L(0^-) = i_L(0^+) = 10^{-5}$ *Amps*. However, to use this information directly, we'd need an equation for $I_L(t)$.

Instead, it's easier to find $i_C(0^+)$. Note: $i_C(0^+) \neq i_C(0^-)$!! At time 0^+, we can write KCL at node V_L, which gives us:

$$\frac{V_L(0^+) - \cos(0)}{500000} + I_C(0^+) + I_L(0^+) = 0$$

We also know the following facts:

$V_L(0^+) = V_C(0^+) = V_C(0^-) = 0$

$I_L(0^+) = I_L(0^-) = 10^{-5}\ Amps$

So our above KCL equation becomes:

$$\frac{-10^{-5}}{5} + I_C(0^+) + 10^{-5}\ Amps = 0$$

This gives us:

$I_C(0^+) = -4/5 * 10^{-5}$ amps

Next, we find $I_C(t) = CV_C'(t) = 10^{-6}(e^{-t} + K_2 e^{-t} - K_2 te^{-t} - \sin(t))$, and thus :

$I_C(0) = 10^{-6}(1 + K_2) = -4/5 * 10^{-5}$

$(1 + K_2) = -40/5$

$(1 + K_2) = -8$

$K_2 = -9$

Thus, we have our final solution:

$$V_L(t) = -e^{-t/\sec} - 9te^{-t/\sec} + \cos(t)\ \text{Volts}$$

EECS 40, Spring 2006
Prof. Chang-Hasnain
Midterm #2

April 6, 2006
Total Time Allotted: 80 minutes
Total Points: 100

1. This is a closed book exam. However, you are allowed to bring two pages (8.5" x 11"), double-sided notes
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. SHOW all the steps on the exam. Answers without steps will be given only a small percentage of credits. Partial credits will be given if you have proper steps but no final answers.
4. Draw BOXES around your final answers.
5. **Remember to put down units.** Points will be taken off for answers without units.
6. **NOTE: $\mu=10^{-6}$; $k=10^{3}$; $M=10^{6}$**

Last (Family) Name:_____

First Name: _____

Student ID: _____Lab Session: _____Dis. Session: _____

Signature: _____

Score:	
Problem 1 (20 pts)	
Problem 2 (35 pts):	
Problem 3 (15 pts):	
Problem 4 (30 pts):	
Total	

1.(20 pts) Match the transfer function to the Bode plot. Each transfer function matches to exactly one Bode plot. Also, there is no partial credit for this question.

a. $H(f)=\frac{1}{\left(\frac{jf}{100}\right)^2+0.5\left(\frac{jf}{100}\right)+1}$	b. $H(f)=\frac{1}{\left(\frac{jf}{100}+1\right)^2}$	c. $H(f)=\frac{1}{\frac{jf}{1000}+1}$
d. $H(f)=\frac{1}{\frac{jf}{100}+1}$	e. $H(f)=\frac{1}{\left(\frac{jf}{100}\right)^2+1}$	

Mark your answer here

Magnitude Plot (dB)

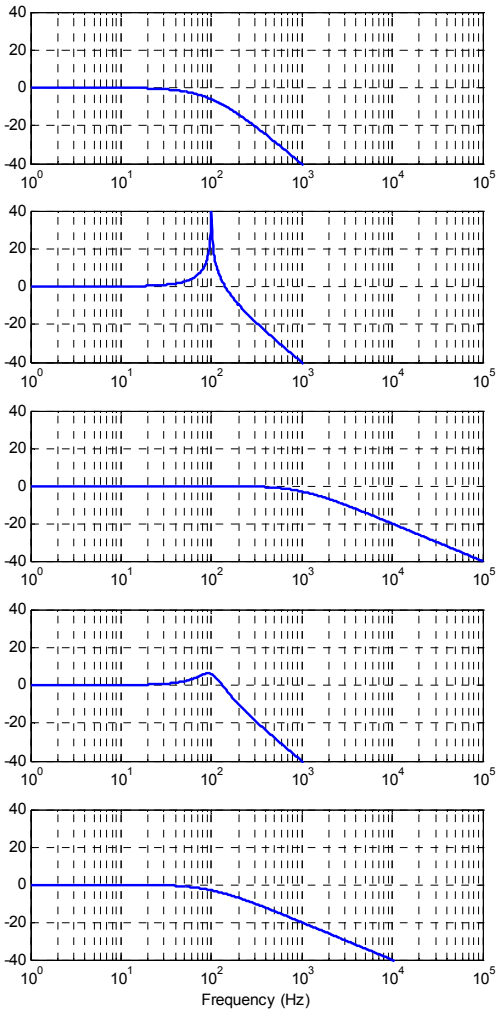
b

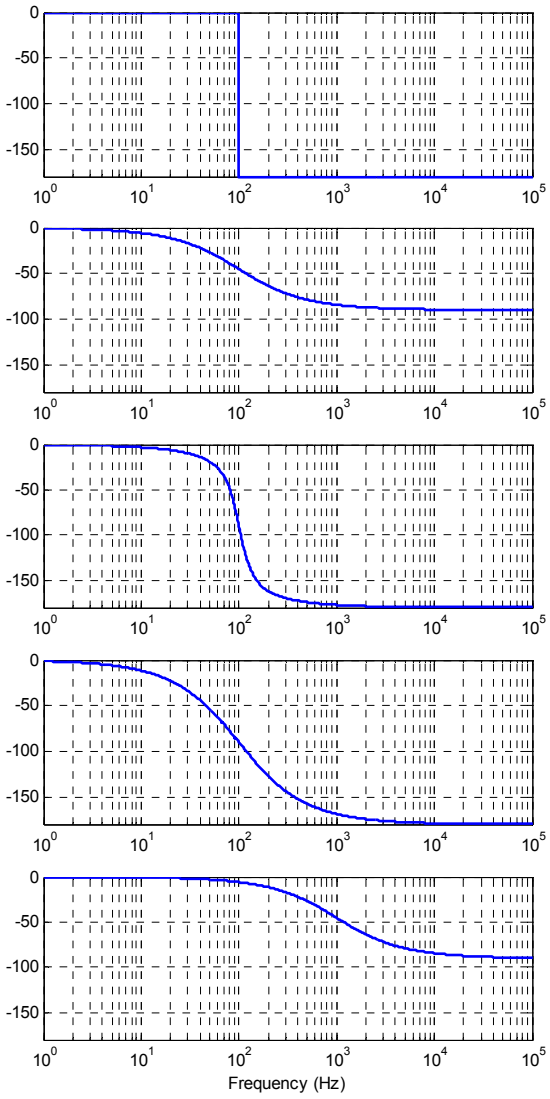
e

c

a

d



Mark your answer here	Phase Plot (degrees)
e	
d	
a	
b	
c	

For the magnitude plot, we first split the list into first- and second-order Bode plots. The first order Bode plots have a -20dB/decade slope, and the second-order Bode plots have a -40dB/decade slope.

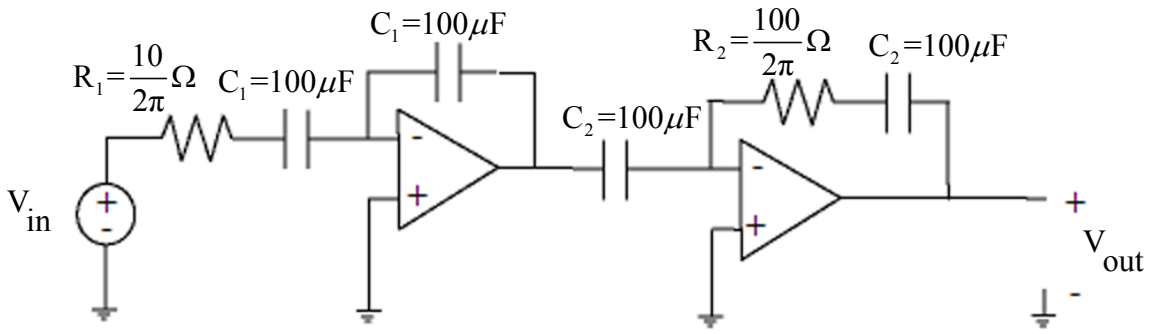
Looking at the breakpoints of the first-order Bode plots, we see that (c) has a breakpoint at f = 1000Hz, and that (d) has a breakpoint at f = 100Hz.

Looking at the size of the humps/peaks of the second-order Bode plots, decreasing values of zeta gives rise to a larger peak. (Note that technically speaking, (b) is two first-order terms but we can think of it as having a zeta = 1).

From this, we have that the magnitude plots match as: (b), (e), (c), (a), (d).

For the phase plot, we again split the list into first- and second-order terms. For first-order terms, the phase plot is -45 degrees at the breakpoint. For second order terms, decreasing values of zeta gives rise to a sharper phase transition.

2.(35 pts) The circuit schematic for a functional block known as a lead compensator is:



a (15 pts) Let $R_1 = 10/(2\pi)$ ohms, $R_2 = 100/(2\pi)$ ohms, $C_1 = 100$ uF, and $C_2 = 100$ uF. Show that the transfer function of the circuit shown above is:

$$H(\mathrm{f}) = \frac{\frac{\mathrm{jf}}{100}+1}{\frac{\mathrm{jf}}{1000}+1}$$

Method 1: all at once

1) $V_{in} - I_1\left(R_1 + \frac{1}{j\omega C_1}\right) = 0$

2) $0V - I_1\left(\frac{1}{j\omega C_1}\right) - I_2\left(\frac{1}{j\omega C_2}\right) = 0$; $I_1\left(\frac{1}{j\omega C_1}\right) = I_2\left(\frac{1}{j\omega C_2}\right)$; $I_1 = I_2\left(\frac{j\omega C_1}{j\omega C_2}\right) = I_2\left(\frac{C_1}{C_2}\right)$

3) $0V - I_2\left(R_2 + \frac{1}{j\omega C_2}\right) = V_{out}$; $I_2 = \frac{-V_{out}}{\left(R_2 + \frac{1}{j\omega C_2}\right)}$

3+2) $I_1 = \left(\frac{C_1}{C_2}\right)\frac{-V_{out}}{\left(R_2 + \frac{1}{j\omega C_2}\right)}$

Combine with 1): $V_{in} - \left[\left(\frac{C_1}{C_2}\right)\frac{-V_{out}}{\left(R_2 + \frac{1}{j\omega C_2}\right)}\right]\left[\left(R_1 + \frac{1}{j\omega C_1}\right)\right] = 0$

$$-\left(\frac{C_2}{C_1}\right)\frac{\left(R_2+\frac{1}{j\omega C_2}\right)}{\left(R_1+\frac{1}{j\omega C_1}\right)}=\frac{V_{out}}{V_{in}};$$

$$\frac{V_{out}}{V_{in}}=-\frac{\left(R_2C_2+\frac{1}{j\omega}\right)}{\left(R_1C_1+\frac{1}{j\omega}\right)}=-\frac{\left(j\omega R_2C_2+1\right)}{\left(j\omega R_1C_1+1\right)}=-\frac{\left(j2\pi f\left(\frac{100}{2\pi}\Omega\right)100\mu F+1\right)}{\left(j2\pi f\left(\frac{10}{2\pi}\Omega\right)100\mu F+1\right)}=\frac{\left(j\left(\frac{f}{100}\right)+1\right)}{\left(j\left(\frac{f}{1000}\right)+1\right)}$$

Method 2: Two Inverters

$$\frac{Vout1}{Vin1}=-\frac{\frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1}+R_1}=-\frac{1}{1+j\omega R_1C_1}=-\frac{1}{1+j2\pi f(\frac{10}{2\pi})(100\mu F)}=-\frac{1}{1+j\frac{f}{1000}}$$

$$\frac{Vout2}{Vin2}=-\frac{\frac{1}{j\omega C_2}+R_2}{\frac{1}{j\omega C_2}}=-\frac{1+j\omega R_2C_2}{1}=-\left[1+j2\pi f(\frac{100}{2\pi})(100\mu F)\right]=-\left(1+j\frac{f}{100}\right)$$

$$\frac{Vout}{Vin}=-\frac{1}{1+j\frac{f}{1000}}\times-\left(1+j\frac{f}{100}\right)=\frac{j\frac{f}{100}+1}{j\frac{f}{1000}+1}$$

Method 3: Solve in stages:

$$\frac{Vin-0}{R_1+\frac{1}{j\omega C_1}}=\frac{0-Vout1}{\frac{1}{j\omega C_1}};\frac{Vout1}{Vin1}=-\frac{\frac{1}{j\omega C_1}}{R_1+\frac{1}{j\omega C_1}}$$ .. then same analysis as above

$$\frac{Vin2-0}{\frac{1}{j\omega C_2}}=\frac{0-Vout2}{R_2+\frac{1}{j\omega C_2}};\frac{Vout2}{Vin2}=-\frac{R_2+\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2}}$$ .. then same analysis as above

2b (12 pts) In the following table, write the magnitude and phase values for H(f) for f=100Hz, f=1000 Hz, very low f values ($f \to 0\,Hz$) and very high f values ($f \to \infty\,Hz$). These answers only need to be within 1.5 times the correct answer (but only because of rounding errors or sketching inaccuracies that you might have. Do not use the "straight line" approximation if it will cause your answer will be off from the exact value by more than 1.5 times).

Note – terms in red should be f, not ω. Was announced during midterm

f value (Hz)	**10 log $\|H(\omega)\|^2$**	**$\angle H(\omega)$**
Very low f ($f \to 0\,Hz$)	3dB	39.7 deg
f = 100Hz	17dB	39.7 deg
f = 1000Hz	0dB	0 deg
Very high f ($f \to \infty\,Hz$)	20dB	0 deg

Given terms:

$\tan^{-1}(0.1) = 5.7$ deg
$\tan^{-1}(0.5) = 26.6$ deg
$\tan^{-1}(1) = 45$ deg
$\tan^{-1}(2) = 63.4$ deg
$\tan^{-1}(10) = 84.3$ deg

Magnitude: $10\log|H(f)|^2 = 10\log\left[\frac{\left(1+\frac{f^2}{10^4}\right)}{\left(1+\frac{f^2}{10^6}\right)}\right] = 10\log\left[\left(1+\frac{f^2}{10^4}\right)\right] - 10\log\left[\left(1+\frac{f^2}{10^6}\right)\right]$

Phase: $\tan^{-1}\left(\frac{f}{100}\right) - \tan^{-1}\left(\frac{f}{1000}\right)$

For f=100Hz, becomes 3dB – 0 dB = 3dB
For f=1000Hz, becomes 20dB – 3dB = 17dB
Low f becomes 0dB – 0dB

High f becomes $10\log\left[\frac{\left(\frac{f^2}{10^4}\right)}{\left(\frac{f^2}{10^6}\right)}\right] = 10\log[100] = 20dB$

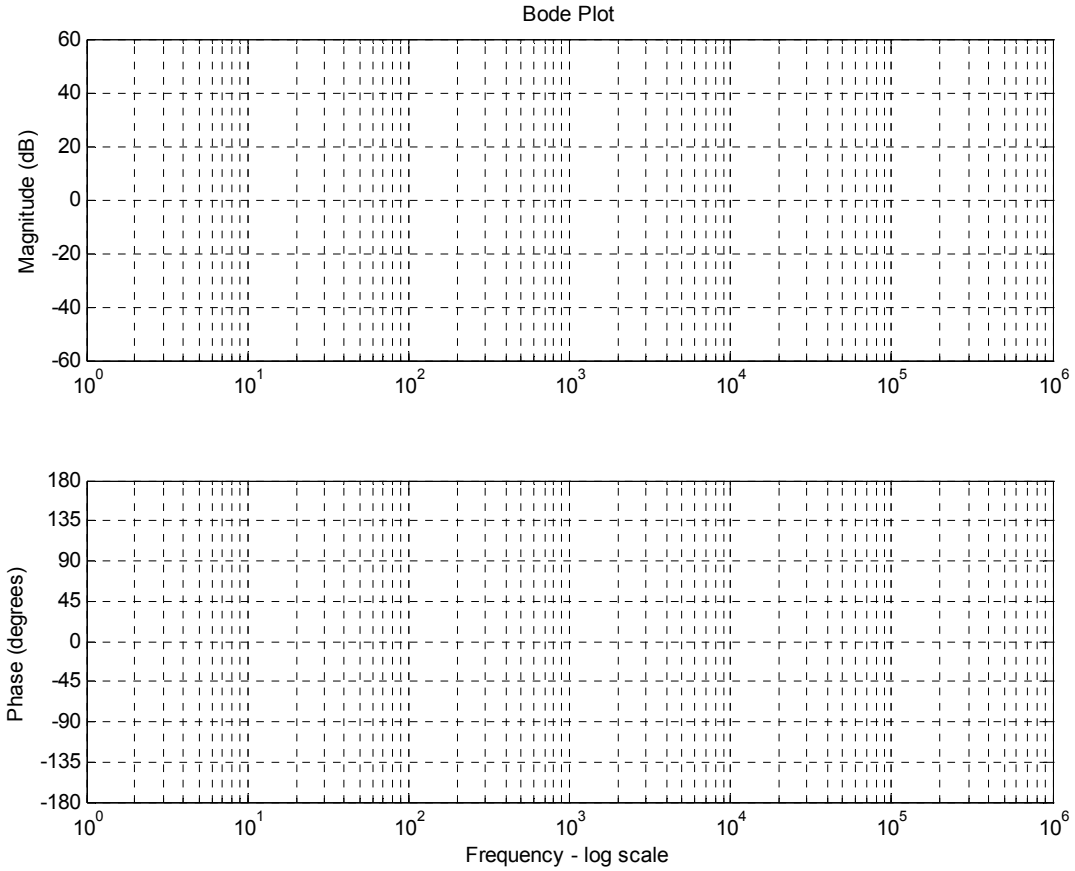
For f=100Hz, becomes $\tan^{-1}(1) - \tan^{-1}(.1) = 45° - 5.7° = 39.3°$

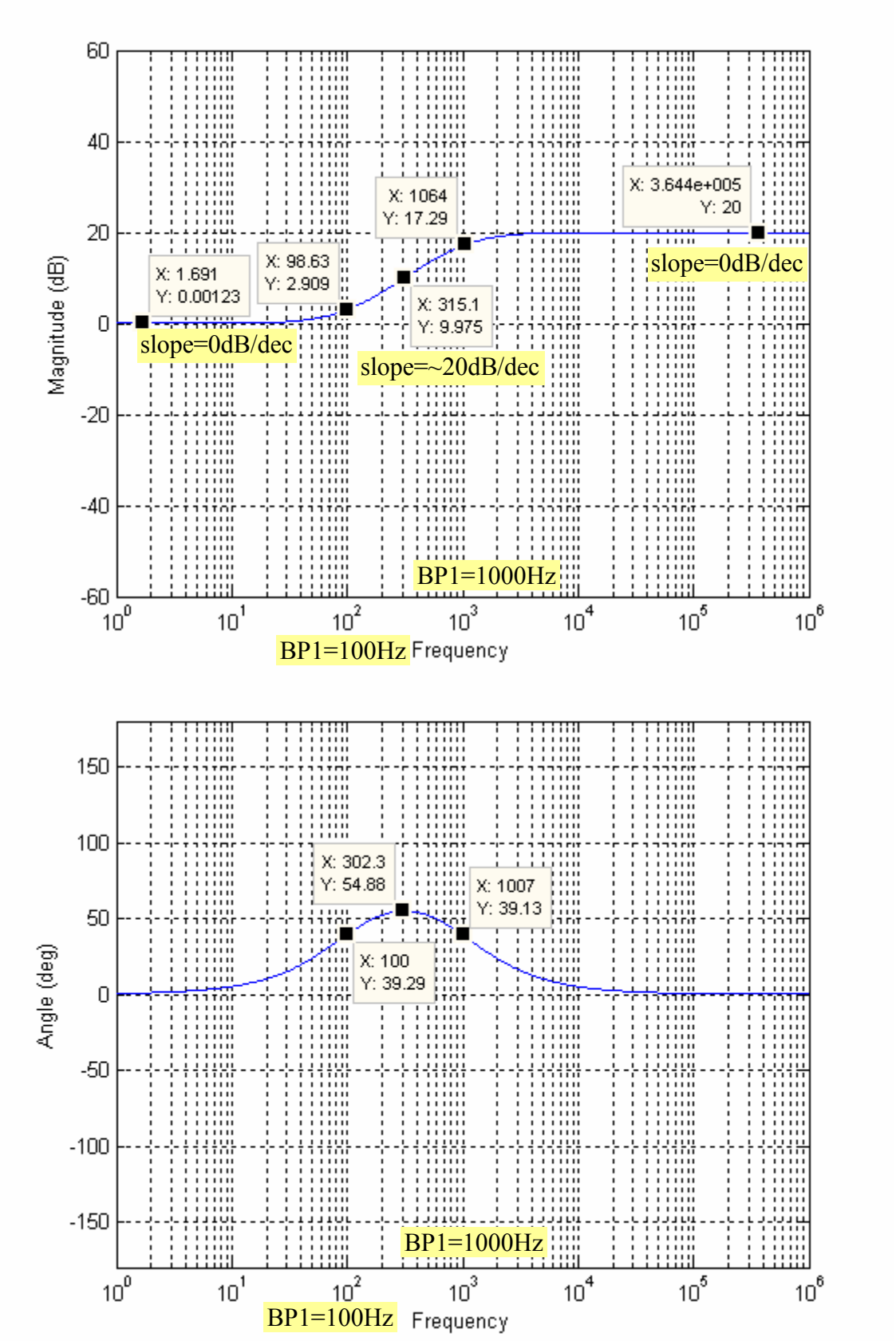
For f=1000Hz, becomes $\tan^{-1}(10) - \tan^{-1}(1) = 84.3° - 45° = 39.3°$

For f-> 0, becomes $\tan^{-1}(0) - \tan^{-1}(0) = 0°$

For f-> infinity, becomes $\tan^{-1}(\infty) - \tan^{-1}(\infty) = 90° - 90° = 0°$

2c (8 pts) Sketch the Bode plot of this transfer function. Sketch BOTH the magnitude and phase plot. Make sure to label the slopes of segments, the two break points of the transfer function, the low frequency magnitude, the high frequency magnitude, and the highest value on the phase plot. Be as accurate as you can, i.e., do not use the "straight line" approximation except as a starting guide if you wish for plotting the actual transfer function.

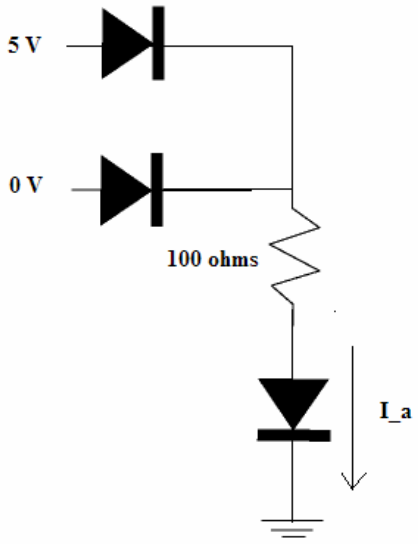



Magnitude (dB)
60
40
20
0
-20
-40
-60
X: 1.691
Y: 0.00123
X: 98.63
Y: 2.909
X: 1064
Y: 17.29
X: 315.1
Y: 9.975
X: 3.644e+005
Y: 20
slope=0dB/dec
slope=0dB/dec
slope=~20dB/dec
BP1=1000Hz
BP1=100Hz
Frequency
Angle (deg)
150
100
50
0
-50
-100
-150
X: 302.3
Y: 54.88
X: 1007
Y: 39.13
X: 100
Y: 39.29
BP1=1000Hz
BP1=100Hz
Frequency

3.(15 pts) Find the unknown values in the circuits below. For the diodes, use the "0.8V ON-OFF" model:

~~If I_d < 0, then the diode is open or OFF~~
If I_d = 0, then the diode is open or OFF
~~If I_d >= 0, then the diode is a 0.8V source or ON~~
If I_d > 0, then the diode is a 0.8V source or ON

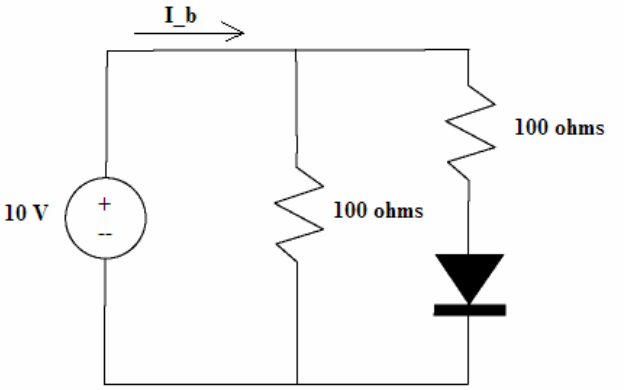
a. (5 pts) Find I_a in the circuit below:



0V diode is off, 5V diode and I_a diode are on.

$$I\_a = \frac{5V - 0.8V - 0.8V}{100\Omega} = 34mA$$

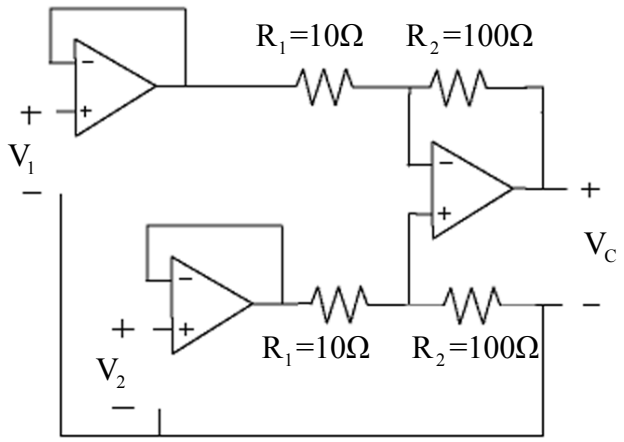
b. (5 pts) Find I_b in the circuit below:



1) 10V – I_1(100ohm) = 0;
   I_1=100mA (I_1 is current in left branch)
2) 10V – I_2(100ohm)-0.8V = 0
   I_2=92mA (I_2) is current in right branch with diode)

So I_b=I_1+I_2=192mA

c. (5 pts) Let R_1 = 10 ohms and R_2 = 100 ohms. Find V_c in the circuit below, in terms of V_1 and V_2:



1) V2 – I2(R1) – I2(R2) = 0
1) V2 – I2(R1+R2)=0

1) $\frac{V_2}{R_1 + R_2} = I_2$

2) V1 – I1(R1) – I1(R2) = Vc
2) V1 – I1(R1 + R2) = Vc
2) $\frac{V_1 - V_C}{R_1 + R_2} = I_1$

3) Vc + I1(R2) = I2(R2) (on far right opamp both voltages same)

3 + 2 + 1) Vc + $\frac{V_1 - V_C}{R_1 + R_2}$ R2 = $\frac{V_2}{R_1 + R_2}$ R2

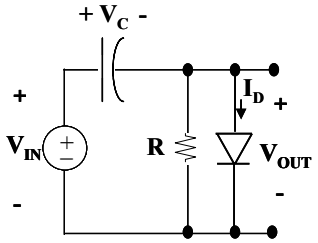
$$V_c\left(1 - \frac{R_2}{R_1 + R_2}\right) = -\frac{R_2 V_1}{R_1 + R_2} + \frac{R_2 V_2}{R_1 + R_2};\ V_c\left(\frac{R_1}{R_1 + R_2}\right) = \frac{R_2}{R_1 + R_2}\left(V_2 - V_1\right);\ V_c = \frac{R_2}{R_1}\left(V_2 - V_1\right)$$

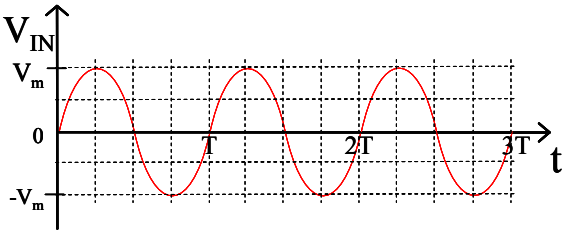
4.(30 pts) Consider the circuit shown below, in which the RC time constant is very long compared to the period *T* of the input $V_{IN}(t)$. Use the Ideal Diode model:

If $V_D < 0$, then the diode is OFF and does not pass current ($I_D=0$)

If $I_D >= 0$, then the diode is ON and $V_D=0$

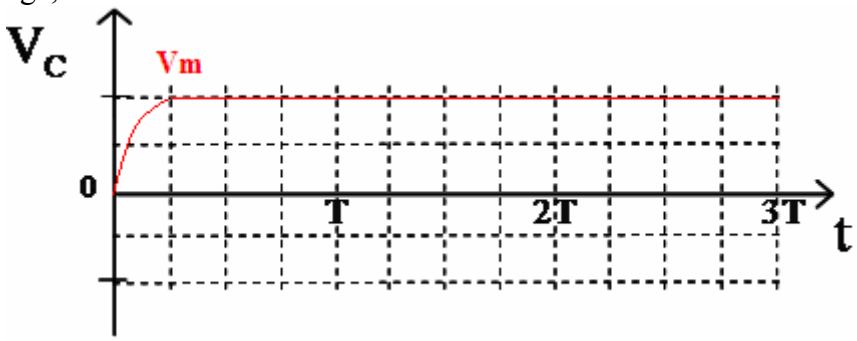
V_D is the voltage drop across the diode and I_D is current through the diode. $V_D = V_{OUT}$ in this problem. Analyze the following circuit. Given $V_{IN}(t)=V_m sin(2\pi t/T)$ for t>0, and $V_C(t=0^-)=0$.



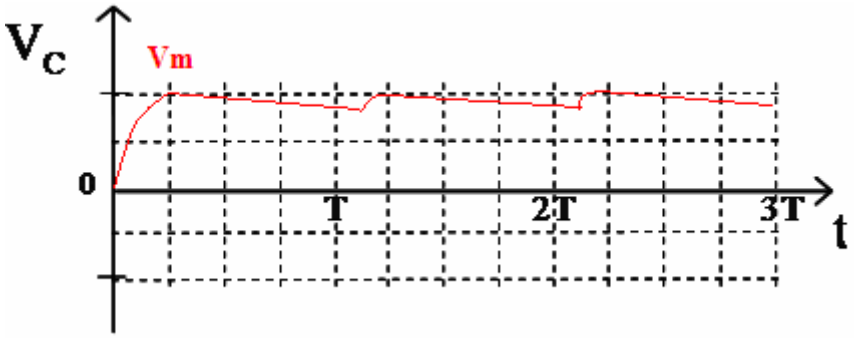


(a) (8 pts) Sketch $V_C(t)$? Label all key values.

The capacitor is initially able to charge up, since V_out starts at 0V and so the diode is a short. However, the capacitor is not able to discharge through the diode since the diode is an open when reverse biased. Thus, the capacitor discharges through the resistor. Since the RC constant is large, we have either:

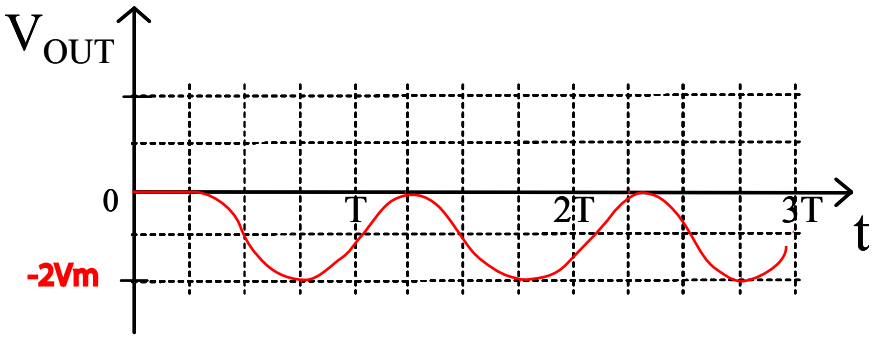


Or:

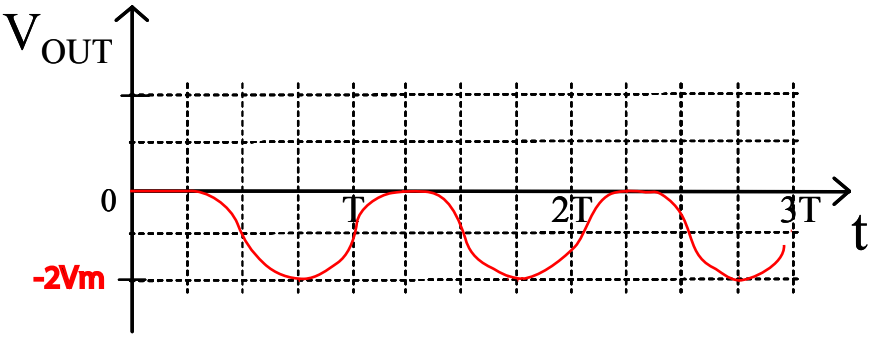


(b) (8 pts) Sketch $V_{OUT}(t)$? Label all key values.

Simple application of KVL gives that V_out = V_in – V_c. The respective sketches of V_out are:



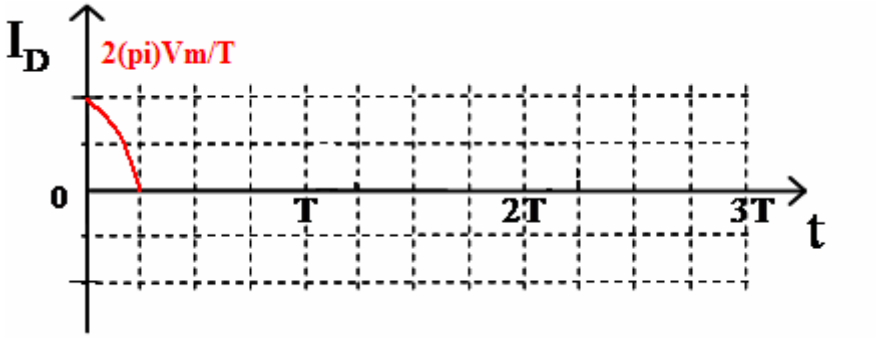
Or:



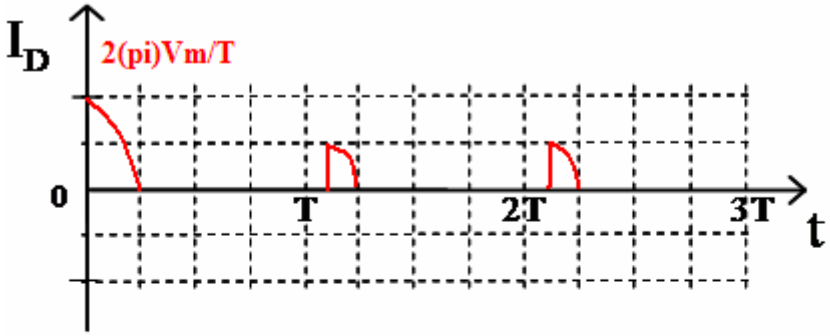
Note the concavity of the curves above.

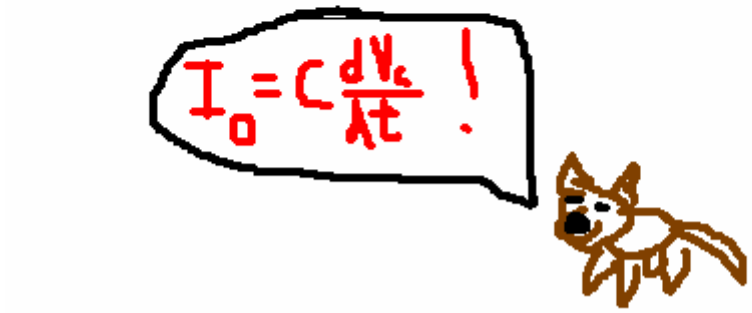
(c) (8 pts) Explain what is happening for different time duration.
The capacitor is initially able to charge up, since V_out starts at 0V and so the diode allows current flow in the positive direction. However, the capacitor is not able to discharge through the diode since the diode is an open when reverse biased. Thus, the capacitor discharges through the resistor. Since the RC time constant is large, the capacitor will discharge very slowly (in the limit it will not discharge at all). When V_C matches V_in, then V_out is 0V and so the diode will again allow the capacitor to charge up. We repeat this process.

(d) (6 pts) Sketch $I_D(t)$? Label all key values.



Or:





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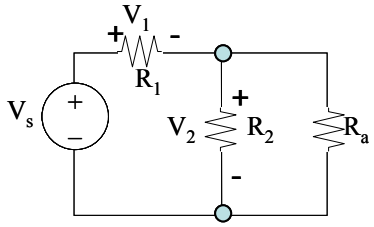
EECS 40, Spring 2006
Closed-book Quiz #1
Prof. Chang-Hasnain

Total Time: 15 minutes
Total Points: 100

1. No electronic devices, i.e. calculators, cell phones, computers, etc.
2. SHOW all the steps on the exam.

1. (40 pts) (a) Express V_2 in terms of R_1, R_2, R_a, and V_s



R_2 and R_a are parallel. We only care about the voltage across them both, so when analyzing the circuit, we can treat their total resistance as $R_{eq} = (R_2 \times R_a)/(R_2 + R_a)$.

Then the circuit just looks like a simple voltage divider. So $V_2 = V_s \times \left(\frac{R_{eq}}{R_{eq} + R_1} \right)$

Or:

$$V_2 = V_s \times \frac{R_2 R_a}{R_1 R_a + R_1 R_2 + R_2 R_a}$$

(b) (30 pts) Set R_a to open circuit. What is V_2 ?

Just looking at the equation above, if we set $R_a \to \infty$ (the definition of an open circuit), then the equation becomes:

$$V_2 = V_s \times \frac{R_2}{R_1 + R_2}$$

Which is the standard equation for a simple voltage divider circuit. We get the same result of course if we just look at the circuit with R_a taken out, and use the voltage divider equation.

These equations are important for your labs, because it shows exactly what happens when we put a

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voltmeter with some finite input resistance into a circuit! Think of R_a as being the input resistance of a voltmeter, which is measuring the voltages in a voltage divider circuit. You can see by the equation in part (a) that we'll end up getting a slightly altered answer.

We often assume voltmeters are perfect open circuits, but they really have a resistance on the order of mega-ohms. So, when we place them in a circuit, we have to be careful that we aren't affecting the rest of the circuit.

In this example, if we are using typical resistor values for R_1 and R_2 (1kΩ for example), and the input resistance of our voltmeter (R_a) is 1MΩ, we only affect the result by around 0.04%, basically negligible. But if we were using higher values for R_1 and R_2, like 1MΩ also, then we change V_2 by 33%, a huge difference!

(c) (15 pts) Comparing V_1 in case (a) and (b). (which one is bigger?)

By inspection, we can see by the equation in part (a), that as we increase R_a, we increase V_2. So by KVL, **V_1 is bigger in case (a)**

Physically speaking, since this is a voltage divider circuit, the potential from the source is split in proportion to each resistance in the loop. So in the case where R_a is finite (case a), the effective total resistance of R_2 and R_a is lower than just R_2 alone (case b), so V_1 is bigger in case a.

(d) (15 pts) Comparing V_2 in case (a) and (b).

Again, since we get rid of R_a in part (b) (make it an open circuit), we increase the total resistance in that section of the voltage divider circuit, so **V_2 is bigger in part (b)**.

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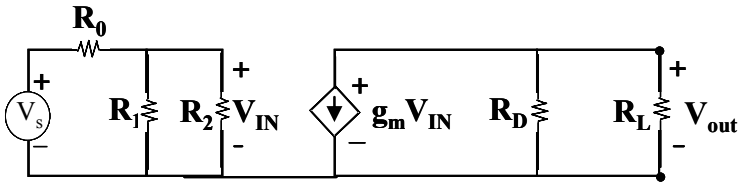
EECS 40, Spring 2006
Closed-book Quiz #2: February 14, 2006
Prof. Chang-Hasnain

Total Time: 15 minutes
Total Points: 100

1. No electronic devices, i.e. calculators, cell phones, computers, etc.
2. SHOW all the steps on the exam.

1. (50 pts) (a) Express V_{out} in terms of R_0, R_1, R_2, R_D, R_L, g_m and V_s



This circuit is easier than it may look at first. The single wire connecting the two loops doesn't really have any effect except to provide something like a ground wire between the two sections of the circuit. You can always arbitrarily make one of the nodes a "ground" node for any circuit if it isn't already labeled. So this ends up just looking like two separate grounded circuits.

You can also notice that you can't have charge building up on one side of the circuit. Charge in these passive circuits is conserved. Even when charge is stored on a capacitor, you still have +Q on one plate and –Q on the other.

OK, so for the actual analysis: R_1 is || to R_2. So we can make that $R_{eq} = R_1R_2/(R_1+R_2)$. So

$V_{in} = V_s * R_{eq} / (R_{eq} + R_o)$

since this is just a voltage divider circuit.

Again, for the right side of the circuit, R_D is || to R_L, so we can combine them into $R_{eq2} = R_DR_L/(R_D+R_L)$.

Then since we have a voltage controlled current source and a resistor in one loop, we can easily figure out the voltage from ohm's law. V= - IR, $I=g_mV_{IN}$. Careful of the sign convention here. It's negative since the current is flowing from the – to + signs on the V_{out} resistor.

$$V_{out} = -\frac{g_m V_s \, R_{eq2} \, R_{eq}}{R_{eq} + R_o}$$

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and substituting in:

$$V_{out} = -\frac{g_m V_s \left(\frac{R_D R_L}{R_D + R_L} \right) \left(\frac{R_1 R_2}{R_1 + R_2} \right)}{\left(\frac{R_1 R_2}{R_1 + R_2} \right) + R_o}$$

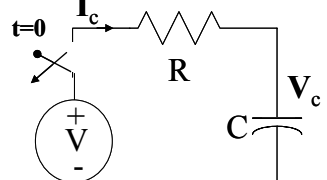
It's usually good to try to substitute values in at the last step to keep the algebra simple.

(b) (30 pts) For the load resistor R_L, what is the Thevenin equivalent voltage V_{th} and Thevenin equivalent resistance R_{th}?

The right side of the circuit is already set up like a Thevenin equivalent current source and resistor. We know $I_{sc} = - g_m V_{IN}$ (remember the sign convention again), and $R_{th} = R_D$ in this configuration. R_{th} doesn't change for either case, and $V_{th} = -R_D g_m V_{IN}$ which is equal to (looking at our V_{IN} expression above:

$$V_{th} = -R_D g_m V_S \frac{\left(\frac{R_1 R_2}{R_1 + R_2} \right)}{\left(\frac{R_1 R_2}{R_1 + R_2} \right) + R_o}$$

2(a) (10 pts) At t=0 the switch is opened, prior to that, the switch had been closed for a long, long time. V is a battery, what are Ic and Vc at t<0?



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If the switch is closed for a very long time, the circuit is in steady state (no signals are varying with time at this point).

So the capacitor acts like an open circuit (since basically our values are all 0Hz at this point). So no current can be flowing in the loop (Ic=0) and since V_R must consequently be 0, then $V_C = V$

(b) (10 pts) What are Ic and Vc when t goes to infinity?

When the switch opens, no current flows. The charge that was on V_C stays on V_C. So at t=infinity, $V_C = V$, and $I_C = 0$.

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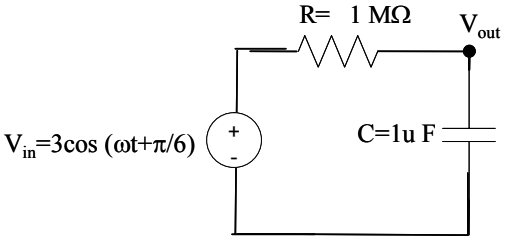
EECS 40, Spring 2006
Closed-book Quiz #3: March 14, 2006

Prof. Chang-Hasnain
Total Time: 15 minutes
Total Points: 100

1. No electronic devices, i.e. calculators, cell phones, computers, etc.
2. SHOW all the steps on the exam.

1. You are given the circuit on the right.
a) (30 pts) What are V_{in} and V_{out} in phasors? Write them in terms of ω.



V_{in} in phasor form is just $V_{in}=3\angle 30^\circ$.

The phasor form for V_{out} can be found using V_{in} and the transfer function for V_{out} as shown:

$$V_{out} = V_{in}\frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C}+R} = 3\angle 30^\circ \frac{1}{1+j\omega RC} = 3\angle 30^\circ \frac{1}{1+j\omega * 1s} = \frac{3\angle 30^\circ}{\sqrt{1+\omega^2}\angle \tan^{-1}(\omega)} = \frac{3}{\sqrt{1+\omega^2}}\angle(30^\circ - \tan^{-1}(\omega))$$

Note I omitted the "1 second" term in the last two steps. To be more clear, the final answer with proper units would be something like

$$V_{out} = \frac{3}{\sqrt{1+(\omega * 1\sec)^2}}\angle(30^\circ - \tan^{-1}(\omega * 1\sec))$$

b) (5 pts) What is the break point frequency in Hz?

The break frequency is just when $|V_{out}|=|V_{out\text{-}max}/\text{sqrt}(2)|$. So looking at the magnitude of V_{out}, the break point f_B in Hz occurs when:

$$\frac{3}{\sqrt{2}} = \frac{3}{\sqrt{1+(\omega_B)^2}}; 2 = 1+(\omega_B)^2; \omega_B = 1\,rad/s$$

$$f_B = 1/2\pi\, Hz$$

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c) (5 pts) What type of filter is this?

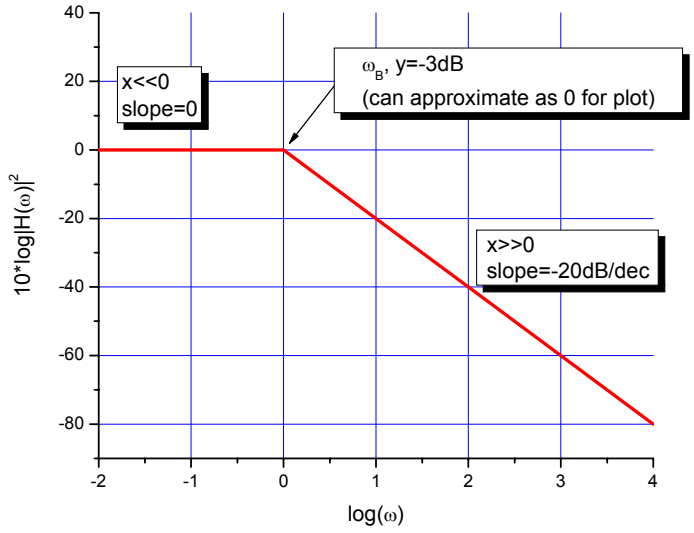
This is a low pass filter. Remember, an easy way to tell is to think of what happens when the input is 0Hz, and when the input is ∞Hz. At 0Hz, a capacitor acts like an open circuit so V_{out} is maximum. At ∞Hz, capacitors act like a short circuit, so V_{out} is 0V. Hence, it "passes" the low frequency signals.

(d) (30 pts) The transfer function is $H(\omega)=\frac{V_{out}}{V_{in}}$. Plot the magnitude Bode Plot of the transfer function. Plot x-y plot, where $y=10\log\left|H(\omega)\right|^2$ and x = log ω. Label y at x<<0, 0, and the slope of the line as x>>0.

The transfer function is written above:

$$H(\omega)=\frac{1}{1+j\omega*1s}$$

We already know the break angular frequency which is $\omega_B=1^{rad}/_{s}$. So this is the point where the graph switches from a slope of 0 to a slope of -20dB/decade. We can do a quick "sanity check" and note that if we compare ω=1rad/s and ω=10rad/s, indeed |H(w)| drops by a factor of 10 for a frequency that's about 10 times higher than the break point. Hence, since the plot is of $y=10\log\left|H(\omega)\right|^2$, the slope is -20dB per decade above the break frequency.



At x<<0, y is 0. At x=0 (w=1), the break point, we can approximately draw the plot at y=0, but

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really this is the “3dB” point, so the y value is exactly -3dB. At x>>0, the slope is labeled as -20dB/decade.

(e) (30 pts) Plot phase Bode plot of the transfer function. Plot x-y plot where $y = \angle H(\omega)$ and x = log ω. Label y at x<<0, 0, and the slope of the line as x>>0.

For the phase plot, we know the phase portion of the transfer function is

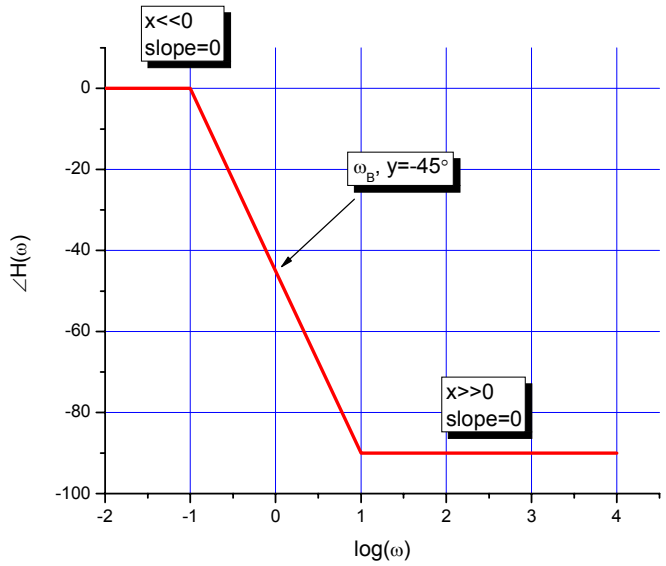
$\angle H(\omega)$ =tan^{-1}(w*1s)

At frequencies w<<w_B, the phase is just tan^{-1}(~0) = 0° .

At frequency w=w_B, the phase is - tan^{-1}(1)=−45

At frequencies w>>w_B, the phase is just - tan^{-1}(infinity)= -90° .

So we draw the low frequency part up to 1/10th of w_B and the high frequency part down to 10w_B and then connect them across the phase point for w=w_B



When x<<0, the value of y is 30 degrees. At x=0, the y value is exactly -15 degrees. At x>>0, the slope is zero, as shown in this plot.

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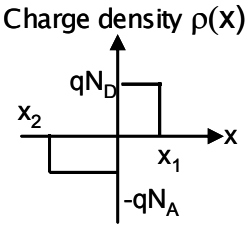
EECS 40, Spring 2006
Closed-book Quiz #4: April 27, 2006

Prof. Chang-Hasnain
Total Time: 15 minutes
Total Points: 100
No electronic devices, i.e. calculators, cell phones, computers, etc.

Hints:	Gauss's Law $\boxed{\frac{dE}{dx} = \frac{\rho}{\varepsilon}}$	Poisson Equation $\boxed{E(x) = -\frac{d\phi(x)}{dx}}$	$\frac{5}{8} = 0.625$

1. p-n junction. You are given the space charge diagram on the right.



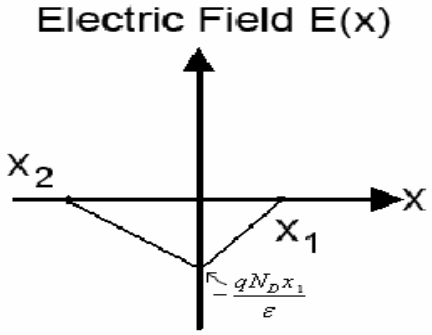
a) (10 pts) Express x_1 in terms of x_2, N_A and N_D

Since the sum of the total charges on each side has to equal 0, you can write $qN_Dx_1 + -(qN_Ax_2) = 0$

$x_1 = N_Ax_2/N_D$

b) (10 pts) Plot electric field *E*(x) vs. distance x. Assuming the ε is the permittivity of the material Label your plot.

By Gauss' Law, $E(x) = \frac{1}{\varepsilon}\int \rho(x)\,dx$



So we just draw the integral of the plot of p(x) Since this is a square function, E(x) ends up looking like a triangle

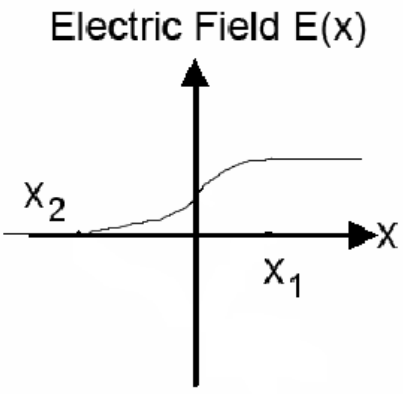
$E(x)_{min} = -\frac{qN_Dx_1}{\varepsilon}$ or $-\frac{qN_Ax_2}{\varepsilon}$

This is a plot of the electric field in the x direction – so the Electric field is actually pointing to the left in this junction.

c) (10 pts) Plot electrostatic potential V(x) vs. distance x. Label your plot.

$V(x) = -\int E(x)\,dx$

So you just have to draw the negative of the integral of your previous plot. Since the E field is zero outside the junction, the voltage is constant outside the junction too



Remember, potential has an arbitrary “ground”. We’ll say that the p-side is 0 volts.

So that makes the voltage on the n (right) side equal to the opposite of the area under the E(x) plot above.

This is just $-\frac{1}{2}\cdot(x_1+x_2)\cdot-\frac{qN_Dx_1}{\varepsilon}=\frac{qN_Dx_1}{2\varepsilon}(x_1+x_2)$

The voltage in the middle of the plot (x=0) is just half the triangle: $-\frac{1}{2}\cdot x_1\cdot-\frac{qN_Dx_1}{\varepsilon}=\frac{qN_Dx_1^{\,2}}{2\varepsilon}$

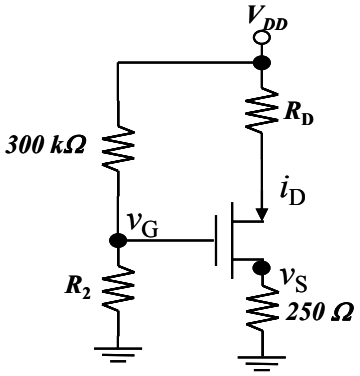
d) (10 pts) If what is described here is the depletion region of a pn junction, which side is n-side? Which is p-side?

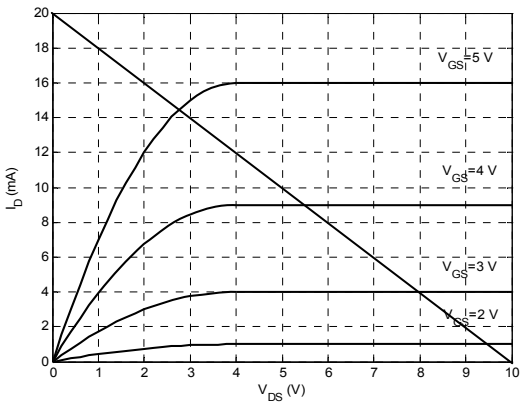
The left side is the p-side, the right side is the n-side. You can tell by the plot of charge density in the depletion region. The p-side has extra holes, which go to the other side and leave negatively charged atoms. The opposite occurs on the n-side

(e) (10 pts) If I connect the positive side of a battery to the $x_0 > x_1$ side, which direction will the current flow?

If you connect a battery positive terminal to a point beyond x_1, you are connecting it to the n-side, so it is reversed bias, so no current will flow.

2 Given the circuit on the left and the load line analysis for i_D and v_{DS} on the right figure.





(a) (10 pts) Determine V_{DD}, R_D

The load line plot tells us the voltage across the D to S terminals of the transistor. So we can see that if we cut the current to zero (open circuit, essentially as if we removed the transistor completely), then the voltage across those terminals would be 10V. Since we said I=0, the voltage across R_D and the 250Ω resistor are 0

So V_{DD}=10V

If we short the terminals, we see I_D=20mA. So we know that 10V – 20mA(R_D + 250Ω)=0
10V – 5V = 20mA * R_D
So 5V/20mA = R_D = 250Ω

(b) (15 pts) If i_D = 9 mA, V_{tn}=1 V what is v_S ? What is v_G? What is R_2?

If i_D=9mA, we know that V_S = 9mA * 250Ω by ohm's law, so

V_s = 2.25V

To know V_{GS}, we need to use the load line analysis figure. We already know I_D, so we need to determine what our V_{DS} and from that we can figure out V_{GS}.

V_D = 10V – 9mA*250W = 7.75V

So V_{DS} = 7.75V - 2.25V = 5.5V

So you can see on the plot above, that where I_{DS}=9mA and V_{DS}=5.5V cross, the gate-source voltage of the transistor, V_{GS}, is equal to 4V.

So V_{GS} = 4V

So the voltage of V_G is equal to V_{GS} + V_S = 6.25V

Since no current flows through the base, we can determine the R_2 thinking of R_2 and the 300kΩ resistor as a voltage divider.

6.25V = $\frac{R_2}{R_2 + 300k\Omega} 10V$; $R_2 = 500k\Omega$

(c) (15 pts) If i_D = 4 mA, V_{tn}=1 V what is v_S ? What is v_G? What is R_2?

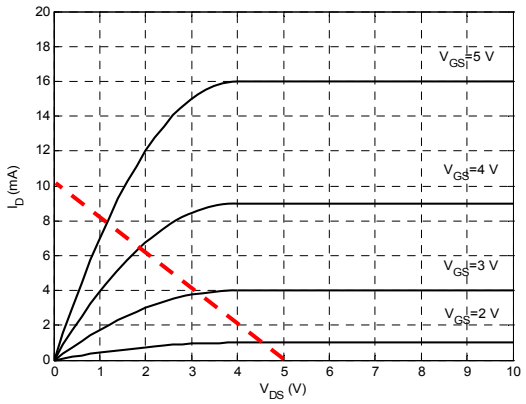
Just like before, if i_D=4mA, we know V_S = 4mA * 250ohm = 1V, V_D = 10V – 4mA*250ohm = 9V,

So V_{DS} = 9V-1V = 8V

So looking at the plot again, V_{GS} = 3V, so $V_G = V_{GS} + V_S$ = 4V

4V = $\frac{R_2}{R_2 + 300k\Omega} 10V$; $R_2 = 200k\Omega$

(d) (10 pts) Draw the new load line on the graph below when V_{DD}=5 V. What is the new i_D?



If the voltage changes to 5V, then the “open circuit” voltage is still 5V, and the “closed circuit” current is reduced by half since we cut the voltage in half. The slope of the line also has to stay the same since we didn’t change the resistance in our “equivalent” circuit.

I_{DS} will of course be reduced, but the actual value depends on the choice of R_2.

EECS 40, Spring 2006
Prof. Chang-Hasnain
Final Exam

May 19, 2006
Total Time Allotted: 180 minutes
Total Points: 200

1. This is a closed book exam. However, you are allowed to bring three pages (8.5" x 11"), double-sided notes
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. SHOW all the steps on the exam. Answers without steps will be given only a small percentage of credits. Partial credits will be given if you have proper steps but no final answers.
4. Draw BOXES around your final answers.
5. **Remember to put down units.** Points will be taken off for answers without units.
6. **NOTE: $\mu=10^{-6}$; $k=10^{3}$; $M=10^{6}$**

Last (Family) Name:_____

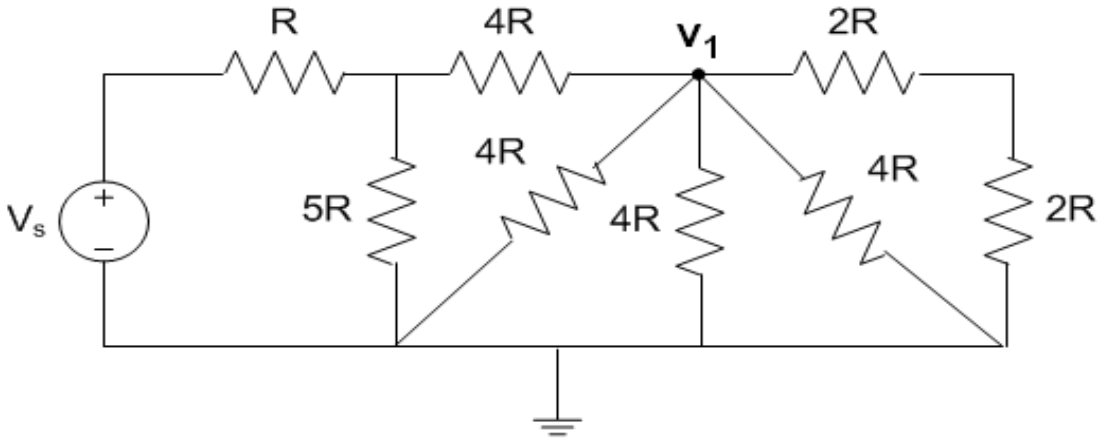
First Name: _____

Student ID: _____Lab Session: _____Dis. Session: _____

Signature: _____

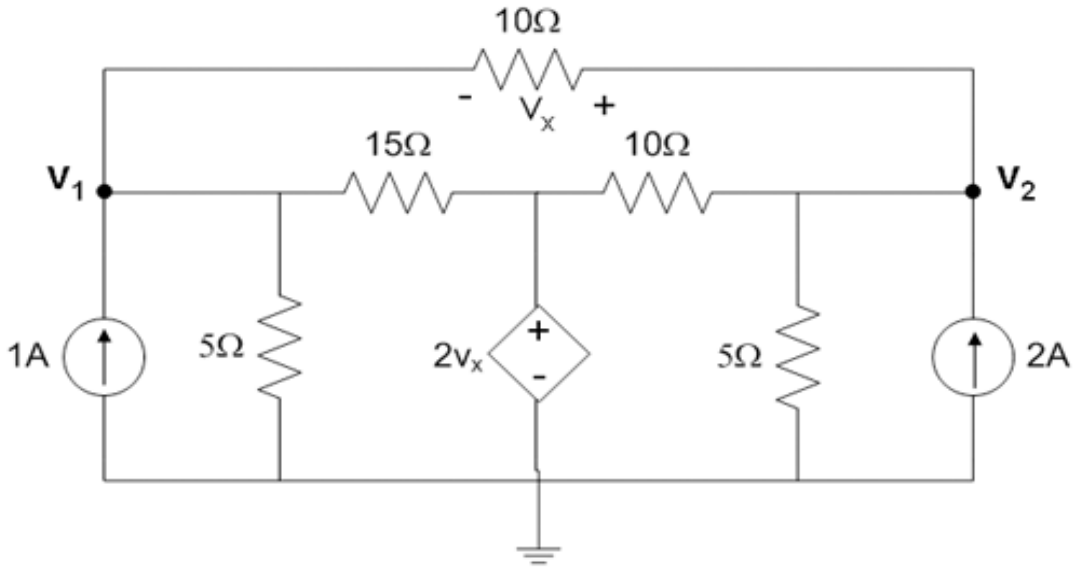
Score:	
Problem 1 (30 pts)	
Problem 2 (55 pts):	
Problem 3 (20 pts):	
Problem 4 (20 pts):	
Problem 5 (20 pts):	
Problem 6 (55 pts):	
Total	

1a. (10 pts) Solve for V_1 in terms of V_s and R



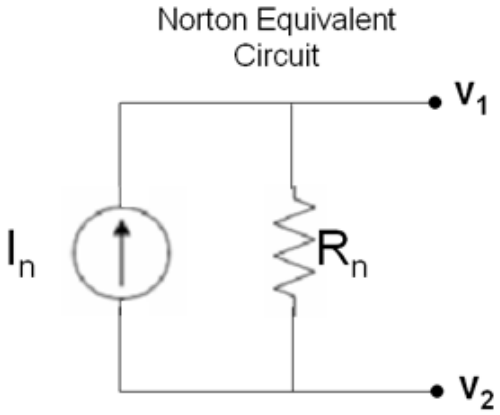
$v_1 =$

1b. (i) (10 pts) Solve for node voltages V_1 and V_2



V_1 =	V_2 =

1b (ii) (10 pts) Find the Norton equivalent current (I_N) and resistance (R_N) for the circuit above (i) between V_1 and V_2 as shown:



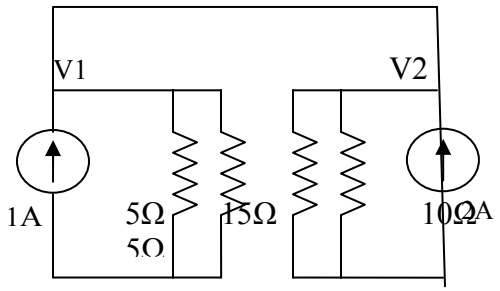
I_N =	R_N =

1

a) By combining the resistors, we can get a circuit that's a Vs, A resistor R and two five ohm resistor in parallel(i.e. 2.5 ohm).
So this is a voltage divider, we can say that V_2 across the 2.5 ohm resistor as
V2=Vs*(2.5)/(2.5+1)=Vs*(5/7)
Use another voltage divider across the 4R and the equivalent resistance of 4R//4R//4R//4R=R,
V1=V2*(1/5)
V1=Vs(5/7)(1/5)=**Vs/7 V**

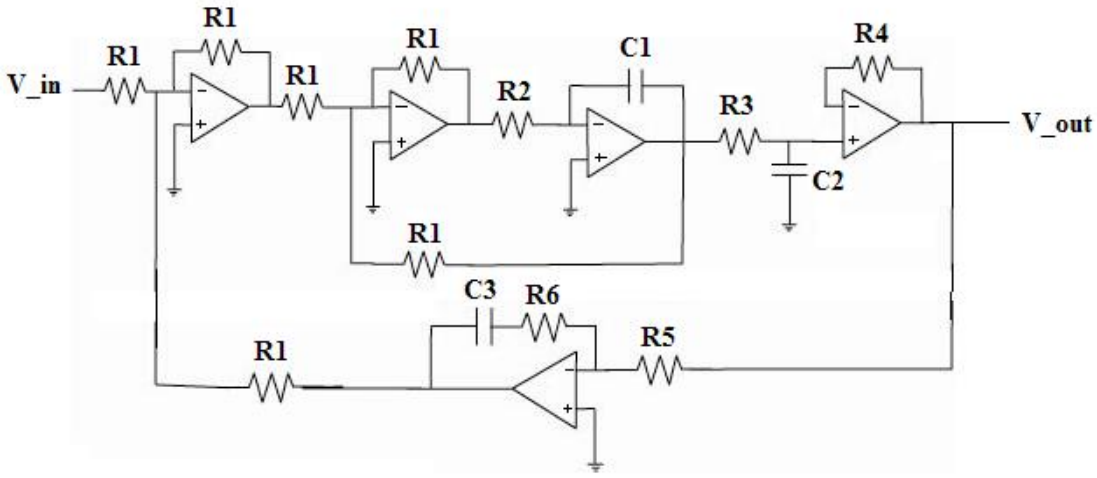
b) Write KCL at V1 and V2, and Vx=V2-V1:
At node V1:
1A=(V1-V2)/10+[V1-2(V2-V1)]/15+V1/5
⇨ 1A=V1*(1/10+1/15+2/15+1/5)+V2*(-1/10-2/15)
⇨ 1A=V1*(1/2)+V2*(-7/30)
At node V2:
2A=(V2-V1)/10+[V2-2(V2-V1)]/10+V2/5
⇨ 2A=V2*(1/10+1/10-2/10+1/5)+V1*(-1/10+2/10)
⇨ 2A=V2*(1/5)+V1*(1/10)
Solve for V1 and V2,
V1=200/37 V
V2=270/37 V

c) The open circuit Voltage Vth=V1-V2 and from part (b) this is V1-V2=200/37-270/37=-70/37
The short circuit current Isc is obtained by shorting V1 and V2, i.e V2-V1=0, and Vx=0.
Redraw the circuit after zeroing out the dependant voltage source, the circuit looks like the following:



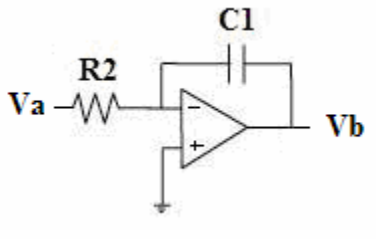
where: 5Ω//15Ω=15/4Ω, 10Ω//5Ω=10/3Ω
At node V1, 1A = V1/(15/4Ω)+Isc
At node V2, 2A=V2/(10/3Ω)-Isc
And V1=V2, sum the above two equations,
3A=V1/(15/4Ω) + V1/(10/3Ω)
V1=V2=90/17 V
Substitue V1 into the first equation
In=Isc=1A-V1/(15/4Ω) = -7/17 A
Rn=Vth/In=170/37Ω

2. (55 pts) Find the transfer function (from V_{in} to V_{out}) of the circuit given below. Note that V_{in} and V_{out} are both referenced to ground.

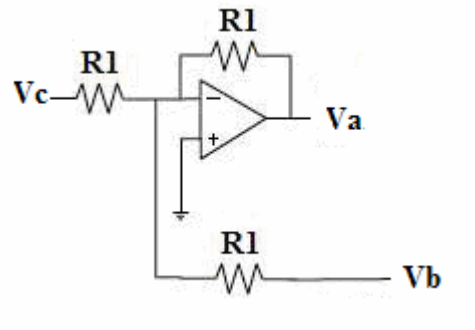


(For parts (a) through (f), write the relationships in terms of labeled values (like R_1, R_2, C_1, etc.)

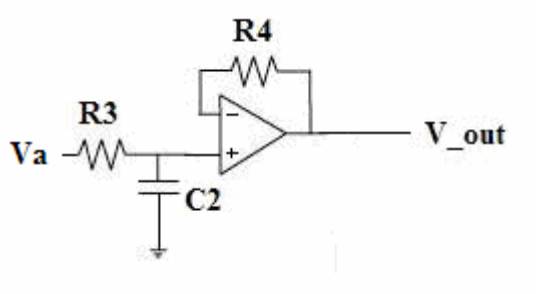
a) (10 pts) Use KCL to find the relationship between V_a and V_b in the subsection below:



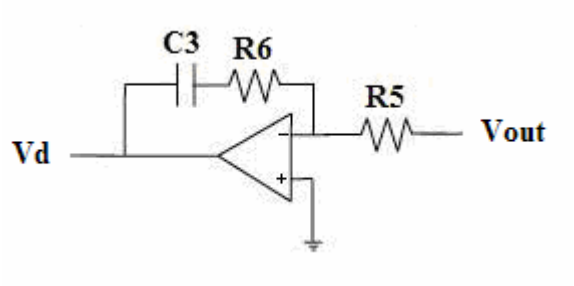
b) (10 pts) Use KCL to find the relationship between V_a, V_b, and V_c in the subsection below:



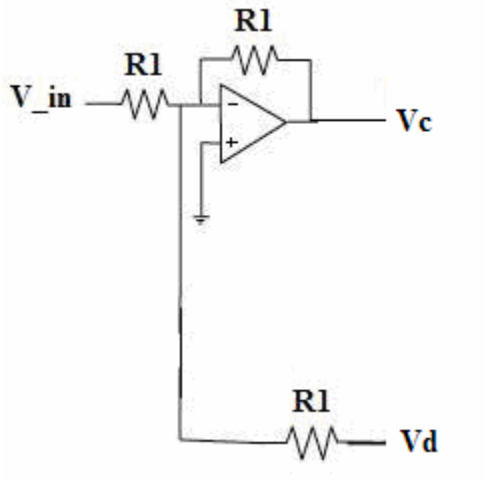
c) (10 pts) Using voltage divider, find the relationship between V_a and V_{out} in the subsection below:



d) (10 pts) Use KCL to find the relationship between V_d and V_{out} in the subsection below:



e) (5 pts) Use KCL to find the relationship between V_{in}, V_c, and V_d in the subsection below:



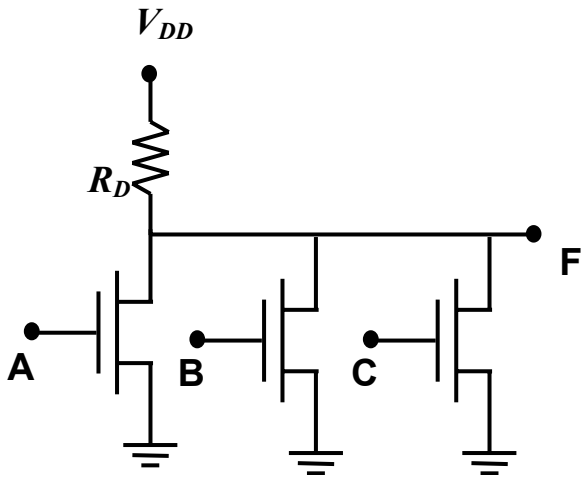
f) (10 pts) Combine the relationships from parts (a)-(e) to figure out the transfer function from V_{in} to V_{out}. You need not simplify your final solution. However, make sure to EXPLICITLY note when and where you use parts a,b,c,d,e. Make your work very clear!

a. Simple application of KCL, in conjunction with the summing point constraints (SPC) yields that $V_a/R_2 + V_b/(1/jwC_1) = 0$. This implies that $V_a = -(jw*R_2*C_1)V_b$.
   +5 for KCL
   +3 for SPC
   +2 for math (-1 incorrect sign)
b. Once again, using KCL and the SPC gives that $V_c/R_1 + V_b/R_1 + V_a/R_1 = 0$. This implies that $V_c = -V_a - V_b$.
   +5 for KCL
   +3 for SPC
   +2 for math (-1 incorrect sign)
c. The voltage divider equation, and the SPC immediately gives that $V_{out} = (1/jwC_2)/((1/jwC_2) + R_3)*V_a = 1/(1 + jw*C_2*R_3)*V_a$.
   +5 for Voltage Divider/KCL
   +3 for SPC
   +2 for math (-1 incorrect sign)
d. Using KCL and the SPC, we get $V_{out}/R_5 + V_d/((1/jwC_3) + R_6) = 0$. This implies that $V_d = -(1 + jw*C_3*R_6)/(jw*C_3*R_5)*V_{out}$.
   +5 for KCL
   +3 for SPC
   +2 for math (-1 incorrect sign)
e. This, is the same as b.
   +5 for doing the same thing as in (b) or noting that the problem is the same as (b)
   or:
   +2 for KCL
   +2 for SPC
   +1 for math
f. There are several ways to do this, including some quite clever ways. The most straightforward is to merely do a series of substitutions. Combining equations (a) and (b) gives $V_c = V_b*(jw*R_2*C_1 - 1)$. Next, using equation (c) gives $V_c = V\_out*(jw*R_2*C_1 - 1)*(jw*C_2*R_3 + 1)$.

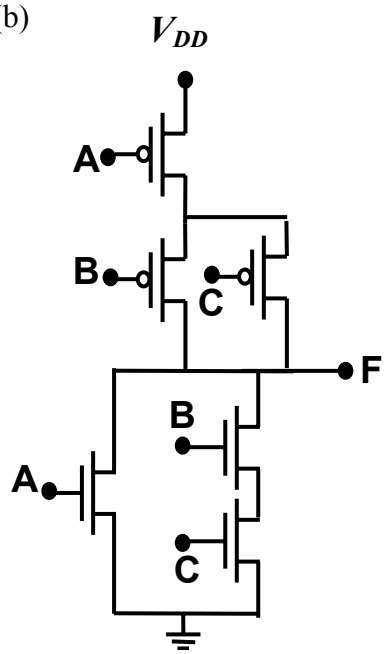
   Next, consider equations (d) and (e). Combining these two blocks gives $V_{in} = -V_c + (1 + jw*C_3*R_6)/(jw*C_3*R_5)*V_{out}$. From the relationship above, we can write that $V_{in} = V_{out}*(-(jw*R_2*C_1 - 1)*(jw*C_2*R_3 + 1) + (1 + jw*C_3*R_6)/(jw*C_3*R_5))$. Thus, our final answer is that $V_{out}/V_{in} = (-(jw*R_2*C_1 - 1)*(jw*C_2*R_3 + 1) + (1 + jw*C_3*R_6)/(jw*C_3*R_5))^(-1)$.
   +4 for the correct connection of the blocks
   +3 for math
   +3 for giving a final answer

3. (20 pts) For the following circuits (i) write the truth table (ii) write the logic function as either a sum of products or product of sums.

(a)



(b)



Problem 3
The truth tables and logic functions are as follows:

a) Note that when a high input is received at A, B, or C, the corresponding NMOS transistor turns on. When all transistors are off, no current can flow through the resistor, so F stays at the high voltage. When a transistor is on, it behaves almost as a short, so F goes to the low voltage.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	1	1	0
1	0	1	0
1	1	0	0
1	1	1	0

$F = \overline{A} \cdot \overline{B} \cdot \overline{C}$
The logic function is also known as NOR.

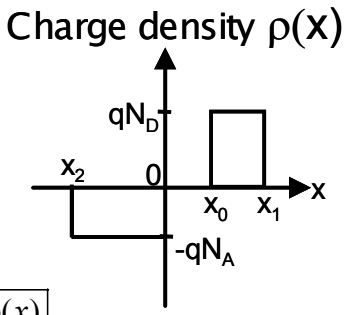
b) In this case, high inputs activate NMOS transistors and turn off PMOS transistors. Low inputs activate PMOS transistors and turn off NMOS transistors. The output follows a complete path either to the high voltage, or to ground, and assumes the corresponding voltage value, for any given input set.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
1	0	0	0
0	1	1	0
1	0	1	0
1	1	0	0
1	1	1	0

$F = \overline{A} \cdot \left(\overline{B} + \overline{C}\right)$
Note: we didn't require that the form of the expression be simplified completely. Any expression accurately describing the truth table was accepted for full credit.

4. (20 pts) You are given the space charge diagram on the right.

$$\rho(x) = qN_D, x_0 \le x \le x_1,$$
$$= -qN_A, x_2 \le x \le 0,$$
$$= 0, everywhere\ else$$
$$where\ N_D(x_1 - x_0) = -N_A x_2$$



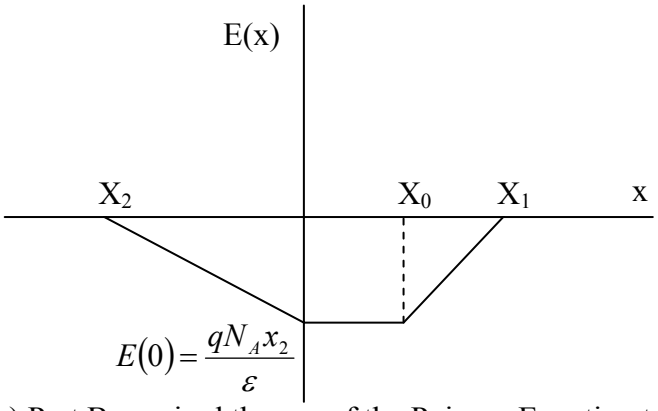
Hints: Gauss's Law $\boxed{\frac{dE}{dx} = \frac{\rho}{\varepsilon}}$ Poisson Equation $\boxed{E(x) = -\frac{d\phi(x)}{dx}}$

a) (10 pts) Plot electric field *E*(x) vs. distance x. Assuming the ε is the permittivity of the material Label your plot. Label the axes as well as important points (both x and *E*(x) values at important points).

b) (10 pts) Plot electrostatic potential V(x) vs. distance x. Label your plot. Label the axes as well as important points (both x and V(x) values at important points).

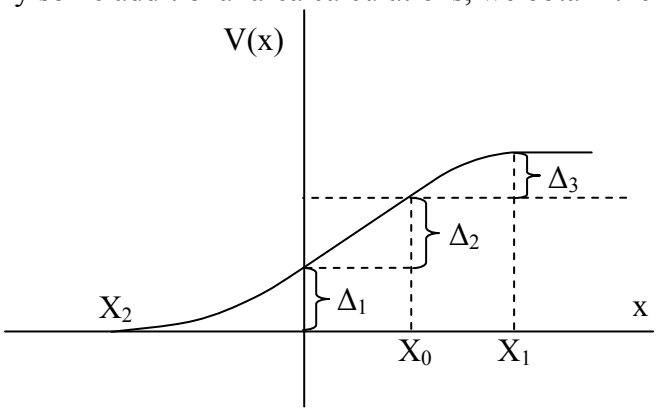
Problem 4

a) Part A required the use of Gauss' Law in order to determine the electric field. Given the provided charge density plot, we obtain the following plot of electric field. Note that because - $N_A x_2 = N_D(x_1 - x_0)$, we know that the integral over the charge density from x_2 to x_1 evaluates to zero, so $E(x_2) = E(x_1)$. By a simple area calculations, we obtain the key value in the plot below.



b) Part B required the use of the Poisson Equation to determine the electric potential.

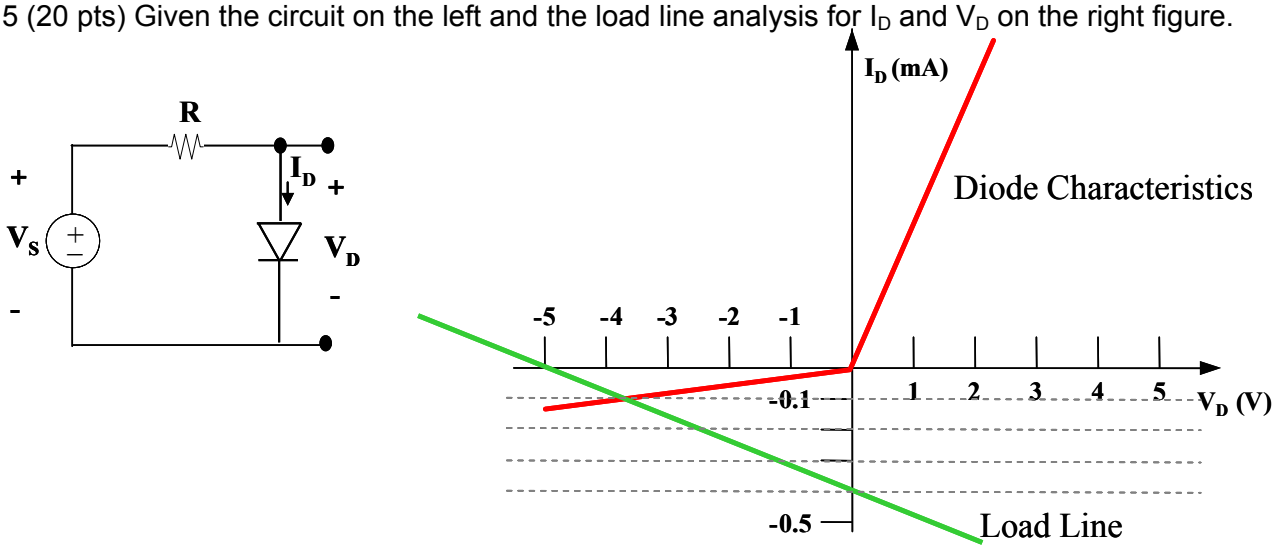
The result is that change in electric potential is given by the negative of the integral over the electric field graph. Because the graph for E(x) is piecewise linear, this is again doable by hand. By some additional area calculations, we obtain the values in the plot below.



As absolute voltage has no meaning, we focus only on the voltage differences outlined above. By geometric area calculations (A = l*w for rectangles, A = (1/2)b*h for triangles):

$$\Delta_1 = \frac{qN_A x_2^2}{2\varepsilon},\ \Delta_2 = \frac{qN_A(-x_0 x_2)}{\varepsilon},\ \Delta_3 = \frac{qN_A(x_1 - x_0)(-x_2)}{2\varepsilon}$$

5 (20 pts) Given the circuit on the left and the load line analysis for I_D and V_D on the right figure.



(a) (10 pts) Determine the values of V_S, R

(b) (10 pts) What are the solutions of V_D and I_D for this circuit?

Problem 5
This problem was an exercise in interpreting a load-line characteristic plot.

a) By inspection, the load line intersects the voltage axis at V = -5V. Given that the load line represents V_s and R, which are arranged in Thevenin circuit form, this intersection gives the open circuit voltage V_s. We can also observe the value of I_{sc} at -0.4mA. Then,

$$R = \frac{V_{oc}}{I_{sc}} = \frac{-5V}{-0.4mA} = \boxed{12.5k\Omega = R\ ,\ V_s = -5V}$$

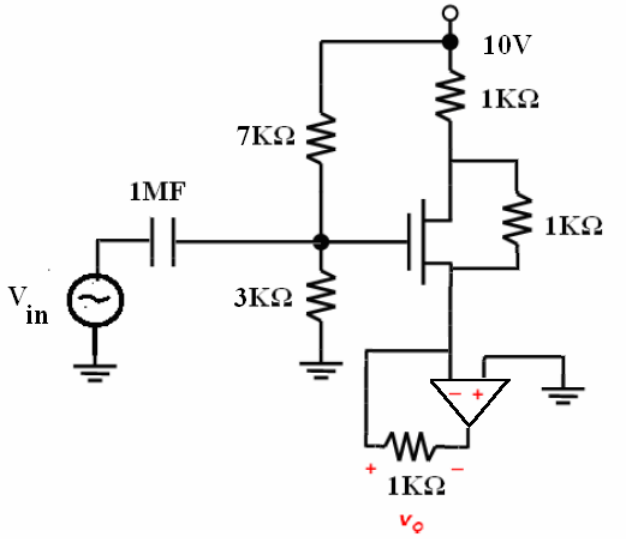
b) To determine I_D and V_D, we can take the coordinates of the intersection point between the IV characteristic of the diode and the load line. By KVL the voltages must match, and by KCL the currents must match.
By inspection, the current at this intersection is -0.1mA. Also, the voltage at the intersection is between -4V and -3V.
We can calculate this voltage explicitly, as follows:

$$V_s = I_D R + V_D$$

$$V_D = V_s - I_D R = -5V - \left(-0.1mA * 12.5k\Omega\right) = -3.75V$$

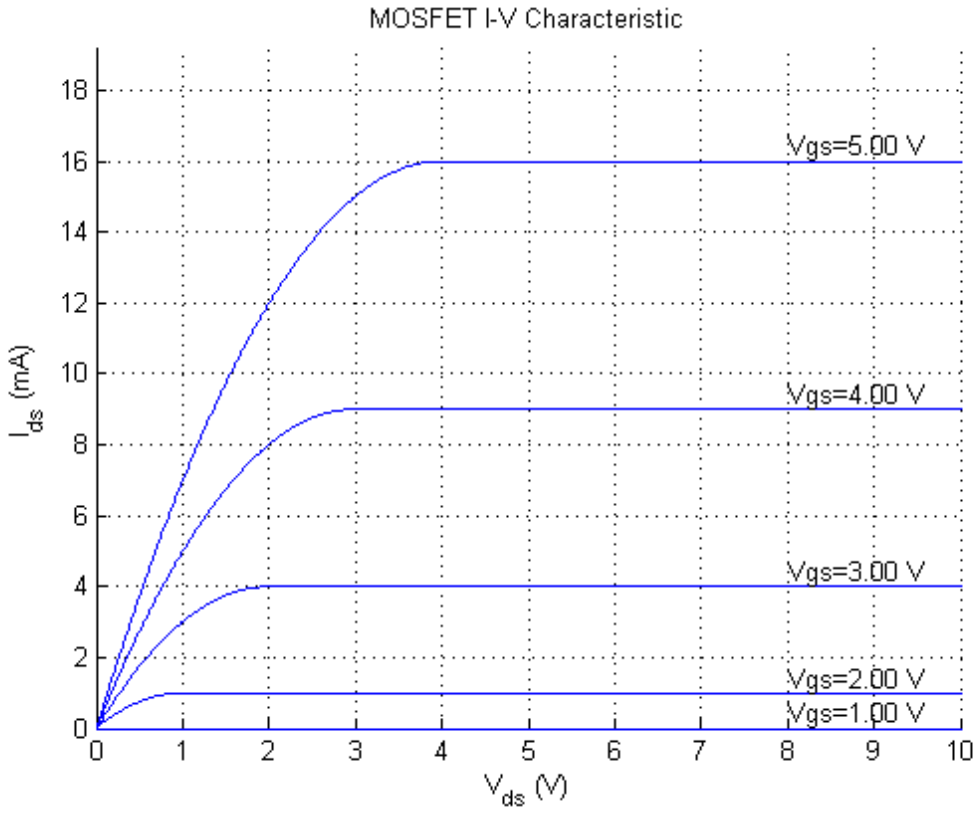
$$\boxed{V_D = -3.75V, I_D = -0.1mA}$$

6. (55 pts) Analyze the following NMOS circuit. K=1 mA/V^2 and V_{t0}=1V



a. (10 pts) Using KVL, write the equation of I_{DS} as a function of V_{DS}.

b. (10 pts) Draw the load line on the following diagram.

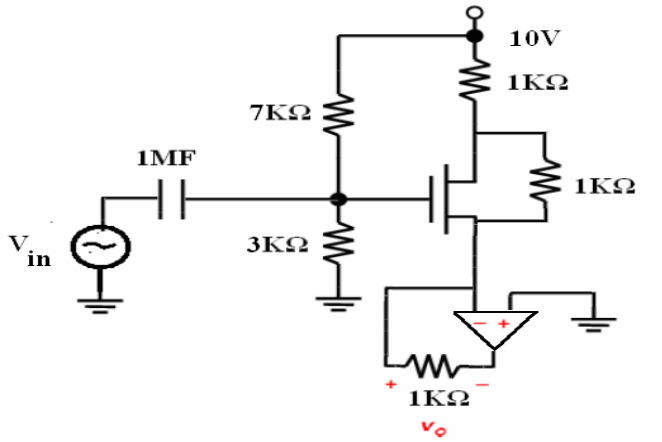


c. (10 pts) By using your load line plot or by using the equation for current through an NMOS, Find V_{GSQ}, I_{DSQ}, V_{DSQ}

d. (15 pts) Draw the small signal model

e. (10 pts) Find A_v, the small signal voltage gain

Problem 6



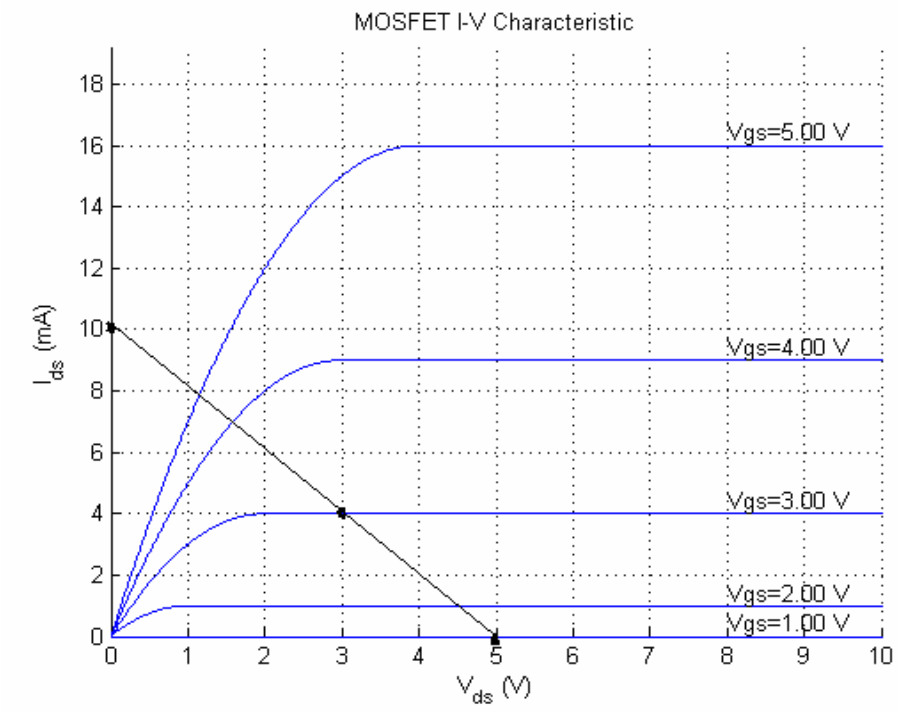
a. (10 pts) Using KVL, write the equation of Ids as a function of Vds.

Solution: V+=V-=0, therefore Vsource= 0

Setup KCL at the Vdrain node: (10V-Vds)/1kohm=Ids+ (Vds/1kohm)

Ids (mA) = (10V-2Vds)/1kohm

b.



At Ids=0, the Vds=5v, and at Vds=0, the Ids=10mA from part a.

c. By using your load line plot or by using the equation for current through a MOSFET, Find V_{GSQ}, I_{DSQ}, V_{DSQ}

Solution: The Q point is where the Vgs=3v, from voltage divider rule, we know

Vgs=10v (3/3+7) =3volts.

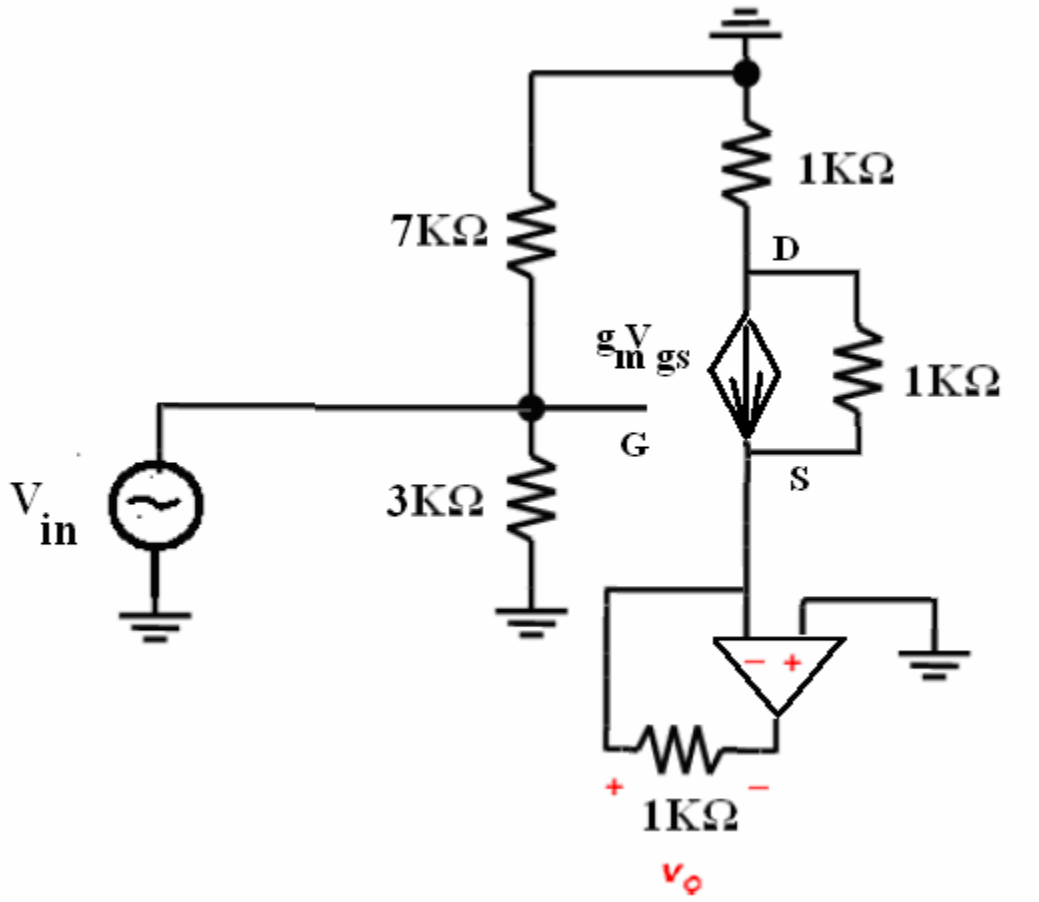
Vdsq=3v (can read of the plot)

Ids=4mA **by substituting the Vgs and Vds into** Ids(mA) = (10V-2Vds)/1kohm

or solve Ids=K(Vgs-Vt)^2=K(3-1)^2=4mA

d) To get the small signal model we ground the DC source, replace the capacitor by a short, and replace the MOSFET by a dependent current source.

Note: It was an extremely common mistake (>70%) for people to merge the S node and the ground node. While the op-amp does indeed force the S node to ground, it is still a distinct node! (In other words, if you write KCL at S, you get different equations than if you write it at node S. In other words again, the op-amp does not act like a wire. The book refers to this voltage copying behavior as a "virtual short")



e) Let the current through the output resistor be called I_o, with the positive direction from left to right (into the op-amp). Clearly $v_o=I_o * 1K$.

To find I_o, we just use some basic circuit analysis principles. First, we write KCL at node D, and get that $V_d/1K + V_{ds}/1K + g_m V_{gs}=0$. Since $V_{gs}=V_{in}$, and S=0V, we can rewrite KCL as: $V_d/1K+V_d/1K+4\text{ mS } V_{in}=0$, which gives us $V_d= -2V_{in}$.

We know that I_o will be the sum of the current out of the dependent source, and the current from D to S through the resistor. We get the current through the resistor using Ohm's law, and get that $I_{ds\_through\_resistor}=V_d/1K= -2V_{in}$ mA. Furthermore $I_{ds\_through\_current\_source}=4V_{in}$ mA. Thus, $I_o=I_{ds\_through\_resistor} + I_{ds\_through\_current\_source}= 4V_{in} – 2V_{in}$ mA = 2 V_{in} mA. Thus $v_o=2\ V_{in}$, so the gain is 2.

Sorry this problem was so difficult. I really didn't think (and still don't think) it's so bad, but

then again I have been teaching this class for a year. It's alright, though, only 4 or 5 people got the last part right, so nobody really suffered. - Josh

EECS 40, Spring 2005
Prof. Chang-Hasnain
Midterm #1

March 3, 2005
Total Time Allotted: 80 minutes

1. This is a closed book exam. However, you are allowed to bring one page (8.5" x 11"), double-sided notes
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. Numerical answers within a factor of 1.5 will not get points deducted, provided the steps are all correct and the errors are due to the lack of a calculator. (e.g. if the correct answer is 1, the acceptable range will be 0.67~1.5).
4. SHOW all the steps on the exam. Answers without steps will be given only a small percentage of credits. Partial credits will be given if you have proper steps but no final answers.
5. Write your answers in the spaces (lines, boxes or plots) provided.
6. Remember to put down units. Points will be taken off for answers without units.
7. **NOTE: nH=10^{-9} H; pF=10^{-12} F; GHz=10^{9} Hz; MHz=10^{6} Hz**

Last (Family) Name:_____

First Name: _____

Student ID: _____

Signature: _____

Score:	
Problem 1 (20 pts)	
Problem 2 (20 pts):	
Problem 3 (30 pts):	
Problem 4 (30 pts):	
Total 100 pts	

1: A voltage source with voltage V is connected to N identical resistors with resistance R.

(a) All of the resistors are connected in parallel, as in Figure 1a. What is the equivalent resistance R_{eq}? What is the total power consumed in the resistors?

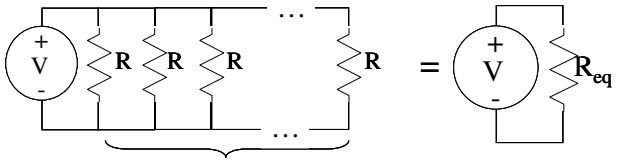


Fig. 1a

Solution:
The resistors are in parallel so:

$$\frac{1}{R_{eq}} = \sum_{n=1}^{N} \frac{1}{R} = \frac{N}{R}$$

$$\Rightarrow R_{eq} = \frac{R}{N}$$

Thus, the total power dissipated is:

$$P = \frac{V^2}{R_{eq}} = N\frac{V^2}{R}$$

Answer: $R_{eq} = R/N$

Power = NV^2/R

(b) All the resistors are all connected in series, as in Figure 1b. What is the equivalent resistance R_{eq}? What is the total power consumed in the resistors?

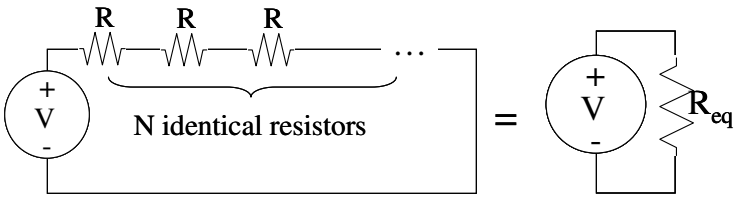


Fig. 1b

Solution:
The resistors are in series so:

$$R_{eq} = NR$$

Thus, the total power dissipated is:

$$P = \frac{V^2}{R_{eq}} = \frac{1}{N}\frac{V^2}{R}$$

Answer: R_{eq}= NR

Power = V^2/NR

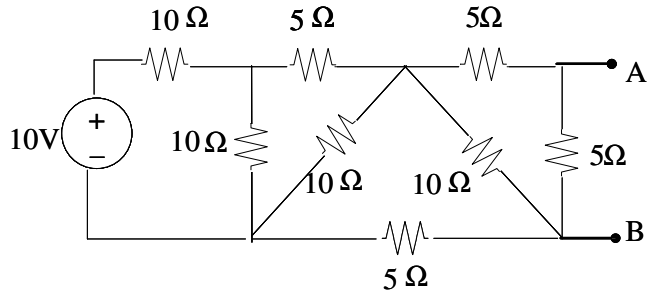
2. Equivalent circuit

(a) What is equivalent resistance R_{eq} for points A-B?

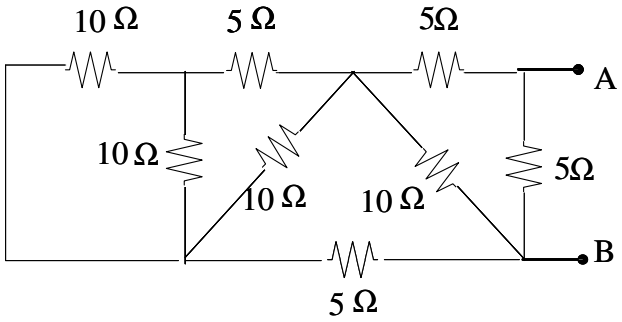
(b) What is the open circuit voltage across points A-B?

(c) What is the short circuit current through points A-B?

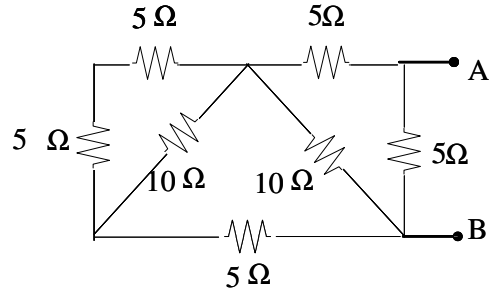
(d) Draw both Thevenin and Norton equivalent circuits.



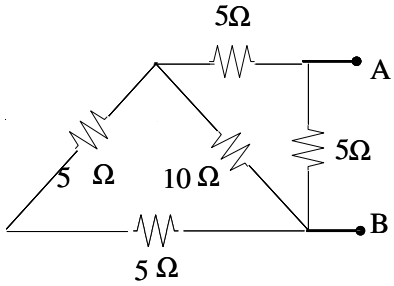
(a) To get the equivalent resistance, we short voltage source:



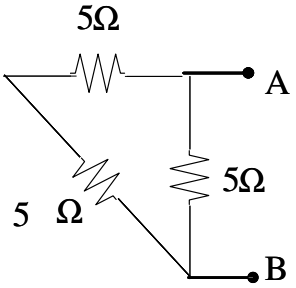
Two 10 Ω in parallel is equivalent to one resistor of 5 Ω. So the equivalent circuit is:



Two 5 Ω in series and then in parallel with 10 Ω. R=(5 + 5) || 10 = 5 Ω. So the equivalent circuit is:



Again two 5 Ω in series then in parallel with one 10 Ω resistor. R=(5 + 5) || 10 = 5Ω. So the equivalent circuit is:



Finally, two 5Ω in series then in parallel with another 5Ω.

$$R_{eq} = (5+5) \| 5 = 10/3\Omega$$

(b) Open circuit

We set nodes C, D, E as shown below besides nodes A and B.

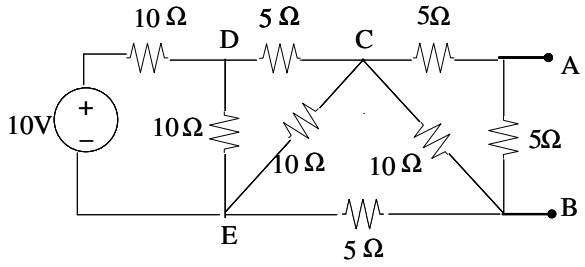


Figure 1

Now we try to find the equivalent resistance to the right of D and E.

Two 5Ω in series then in parallel with one 10Ω, R=(5 + 5) || 10 = 5Ω. We get:

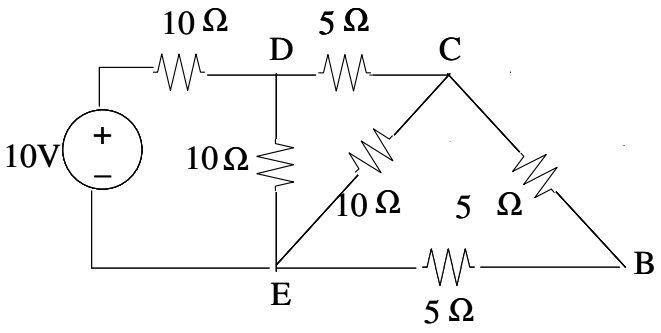


Figure 2

To further simplify that, two 5Ω in series then in parallel with 10Ω, R=(5 + 5) || 10 = 5Ω. We get:

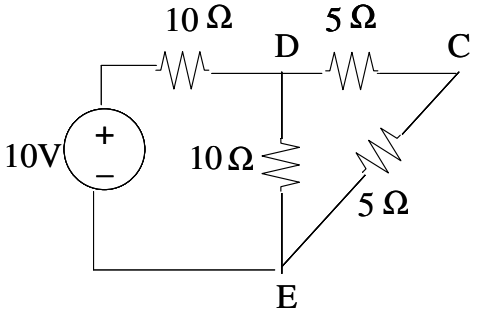
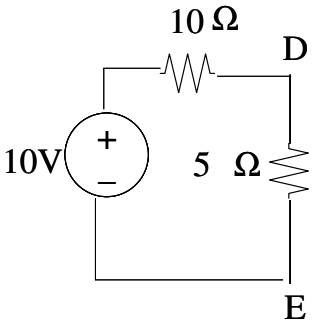


Figure 3

To further simplify, 5Ω in series then in parallel, R=(5 + 5) || 10 = 5Ω, we have:



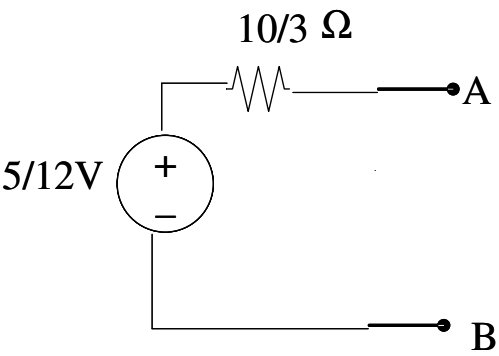
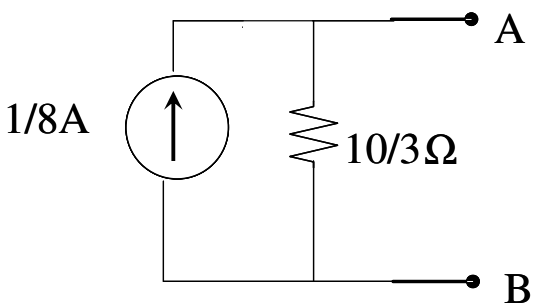
Then $V_{DE} = \frac{5}{10+5} \times 10 = \frac{10}{3}\text{V}$

From Figure 3, we know $V_{CE} = \frac{5}{5+5} \times V_{DE} = \frac{5}{3}\text{V}$

From Figure 2, we know $V_{CB} = \frac{5}{5+5} \times V_{CE} = \frac{5}{6}\text{V}$

Finally from Figure 1, we know $V_{oc} = V_{AB} = \frac{5}{5+5} \times V_{CB} = \frac{5}{12}\text{V}$

(c) $I_{sc} = \frac{V_{oc}}{R_{eq}} = \frac{5}{12} \times \frac{3}{10} = \frac{1}{8}\text{A}$

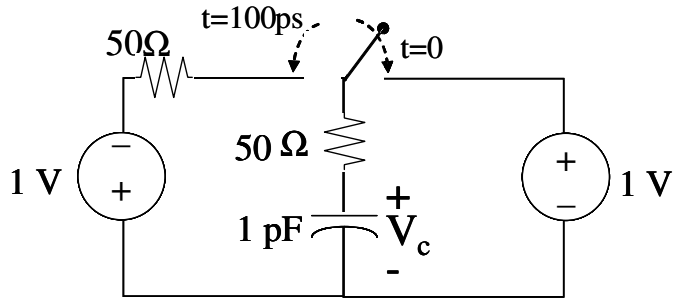
R_{eq}=10/3Ω	V_{oc}=5/12V	I_{sc}=1/8A
Thevenin equivalent: 	Norton equivalent: 	

3. Transient Analysis: 1st order circuit

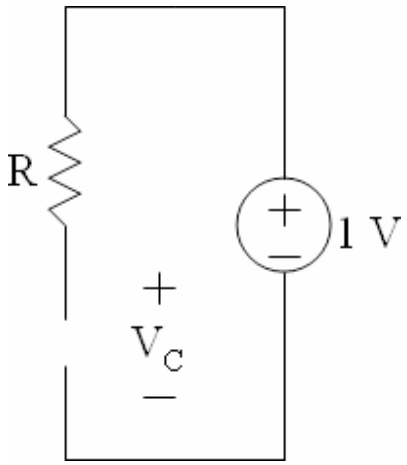
(a) At t<0, the switch is open and V_c= 0. At t=0, the switch is closed towards the right.
What is $V_c(t)$? (*Hint: You can leave terms of the form e^{-x} as they are*)

(b) At t=100 ps, the switch is closed towards the left and shall stay closed towards the left.
What is $V_c(t)$ when t>100 ps?

(c) Qualitatively draw $V_c(t)$ when t>0.

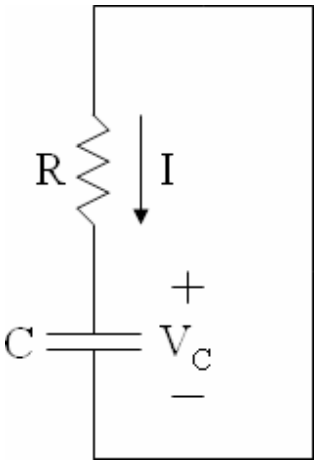


Solution:
(a) *Steady-state response*: At DC steady-state, the capacitor behaves like an open circuit so we can redraw the circuit like so:



No current flows in this circuit, so there is no voltage drop across the resistor and KVL says that the steady state voltage is 1 V.

Transient response: To see the natural response of the circuit, we turn off all power sources:



KVL:

$$-V_C(t) - RI(t) = 0$$

where

$$I = C\frac{dV_C(t)}{dt}$$
$$\Rightarrow \frac{dV_C(t)}{dt} + \frac{1}{RC}V_C(t) = 0$$

This first-order linear differential equation gives solutions of the form

$$V_C(t) = Ke^{-t/\tau}$$

Substituting into the homogeneous equation, we have:

$$-\frac{K}{\tau}e^{-t/\tau} + \frac{K}{RC}e^{-t/\tau} = \left(-\frac{1}{\tau} + \frac{1}{RC}\right)Ke^{-t/\tau} = 0$$
$$\Rightarrow \tau = RC = 50\text{ps}$$

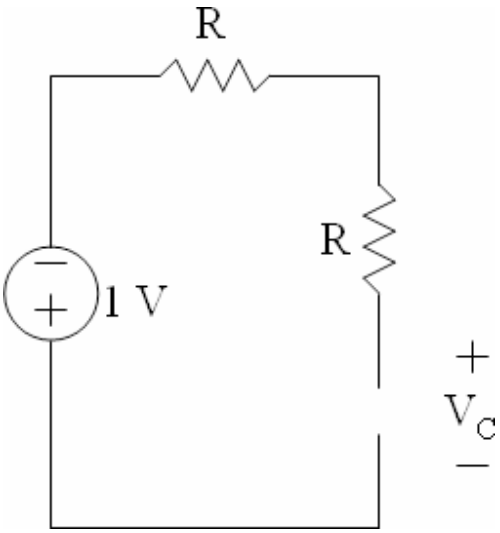
Total response: From the above, we have that the total response is in the form:

$$V_C(t) = 1 + Ke^{-t/50\text{ps}}$$

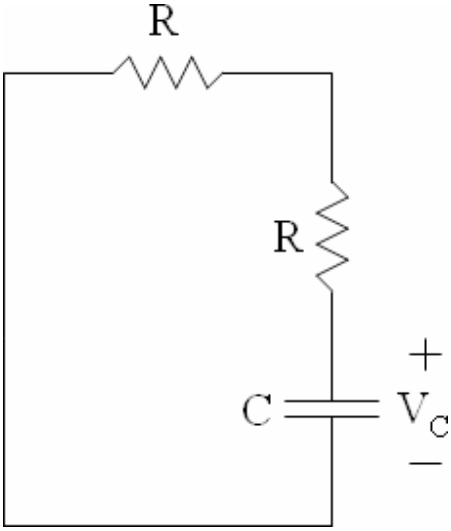
And since the voltage across a capacitor must be continuous, we have the initial condition:

$$V_C(0^+) = 1 + K = 0$$
$$\Rightarrow K = -1$$
$$\Rightarrow V_C(t) = 1 - e^{-t/50\text{ps}}\ \text{V}$$

(b) The analysis here is much the same as part (a). *Steady-state response*: V_C = -1 V.



Transient response:



$$V_C(t) = Ke^{-t/\tau}$$
$$\tau = (50\Omega + 50\Omega)(1\text{pF}) = 100\text{ps}$$

Total response:

$$V_C(t) = -1 + Le^{-t/100\text{ps}}$$

Note that this is equivalent to writing:

$$V_C(t) = -1 + Me^{-(t-100\text{ps})/100\text{ps}}$$

So now when we use part (a) to find initial conditions:

$$V_C(100^- \text{ps}) = 1 - e^{-100\text{ps}/50\text{ps}} = 1 - e^{-2}$$

$$V_C(100^+ \text{ps}) = -1 + Me^{-(100\text{ps}-100\text{ps})/100\text{ps}} = 1 - e^{-2}$$

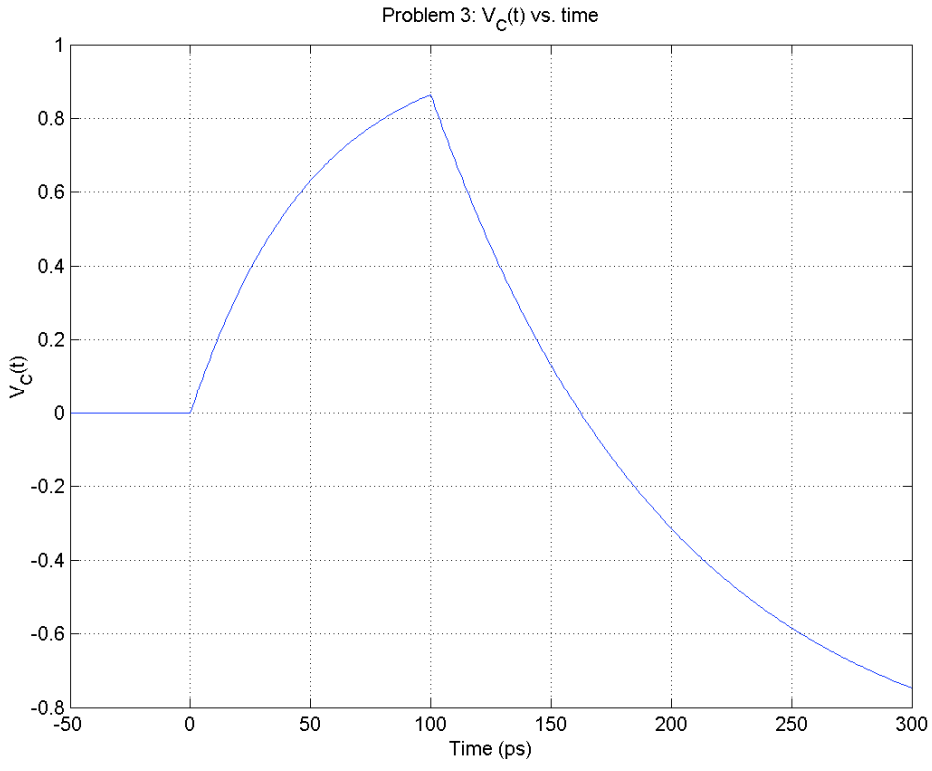
$$\Rightarrow M = 2 - e^{-2}$$

$$\Rightarrow V_C(t) = -1 + (2 - e^{-2})e^{-(t-100\text{ps})/100\text{ps}} \text{ V}$$

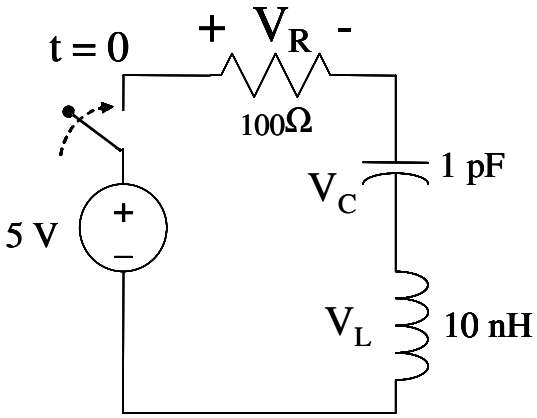
(c)

0<t<100 ps	t>100 ps
$V_c(t) = V_C(t) = 1 - e^{-t/50\text{ps}}$ V	$V_c(t) = V_C(t) = -1 + (2 - e^{-2})e^{-(t-100\text{ps})/100\text{ps}}$ V

Draw $V_c(t)$ vs t:



4. Transient Analysis: 2nd order circuit



At t=0, the switch is closed.

(a) What is the KVL equation of the circuit in terms of $V_c(t)$?

(b) Calculate ω_0 , α, and ζ. Is the circuit underdamped, critically damped or overdamped?

(c) What is the solution of $V_c(t)$?

(*Hint:* $\omega_n = \sqrt{\omega_0^{\,2} - \alpha^2} = \frac{\sqrt{3}}{2} \times 10^{10}$ rad/s)

(a) $V_L + V_R + V_c = 5$

$$\because i = C\frac{dV_c}{dt}, \qquad V_L = L\frac{di}{dt} = LC\frac{d^2V_c}{dt^2}, \qquad V_R = R \times i = RC\frac{dV_c}{dt}$$

$$\therefore LC\frac{d^2V_c}{dt^2} + RC\frac{dV_c}{dt} + V_c = 5$$

or $$\frac{d^2V_c}{dt^2} + \frac{R}{L}\frac{dV_c}{dt} + \frac{V_c}{LC} = \frac{5}{LC}$$

So $$\frac{d^2V_C}{dt^2} + 10^{10}\frac{dV_c}{dt} + 10^{20}V_c = 5 \times 10^{20}$$

(b) $\omega_0 = \frac{1}{\sqrt{LC}} = 10^{10}$ rad/s

$$\alpha = \frac{R}{2L} = 5 \times 10^9$$

$$\zeta = \frac{\alpha}{\omega_0} = \frac{1}{2}$$ underdamped case

(c) Since it's underdamped, the solution has the following form:

$$V_c = K_1 e^{-\alpha t}\cos\omega_n t + K_2 e^{-\alpha t}\sin\omega_n t + 5$$

Initial condition: there is no charge on the capacitor $V_c(0) = 0$

So $V_c = K_1 + 5 = 0 \Rightarrow K_1 = -5$

Initial condition: there is no current in the circuit $i(0) = C\left.\frac{dV_c}{dt}\right|_{t=0} = 0$

So $i(0) = -\alpha K_1 + \omega_n K_2 = 0 \Rightarrow K_2 = \frac{\alpha K_1}{\omega_n} = -\frac{5}{\sqrt{3}} = -\frac{5\sqrt{3}}{3}$

$$V_c = -5e^{-5\times10^9 t}\cos\frac{\sqrt{3}}{2}\times10^{10}t - \frac{5\sqrt{3}}{3}e^{-5\times10^9 t}\sin\frac{\sqrt{3}}{2}\times10^{10}t + 5$$

KVL in terms of $V_c(t)$: $\frac{d^2V_c}{dt^2} + 10^{10}\frac{dV_c}{dt} + 10^{20}V_c = 5\times10^{20}$			
$\omega_0 =$ 10^{10}rad/s	$\alpha =$ $5*10^9$	$\zeta =$ 1/2	Damping case: underdamped
$V_c(t)$: $V_c = -5e^{-5\times10^9 t}\cos\frac{\sqrt{3}}{2}\times10^{10}t - \frac{5\sqrt{3}}{3}e^{-5\times10^9 t}\sin\frac{\sqrt{3}}{2}\times10^{10}t + 5$			

EECS 40, Spring 2005
Prof. Chang-Hasnain
Midterm #2

April 14, 2005
Total Time Allotted: 80 minutes

1. This is a closed book exam. However, you are allowed to bring one page (8.5" x 11"), double-sided notes
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. Numerical answers within a factor of 1.5 will not get points deducted, provided the steps are all correct and the errors are due to the lack of a calculator. (e.g. if the correct answer is 1, the acceptable range will be 0.67~1.5).
4. SHOW all the steps on the exam. Answers without steps will be given only a small percentage of credits. Partial credits will be given if you have proper steps but no final answers.
5. Write your answers in the spaces (lines, boxes or plots) provided.
6. Remember to put down units. Points will be taken off for answers without units.
7. Mobility chart is provided for your reference.

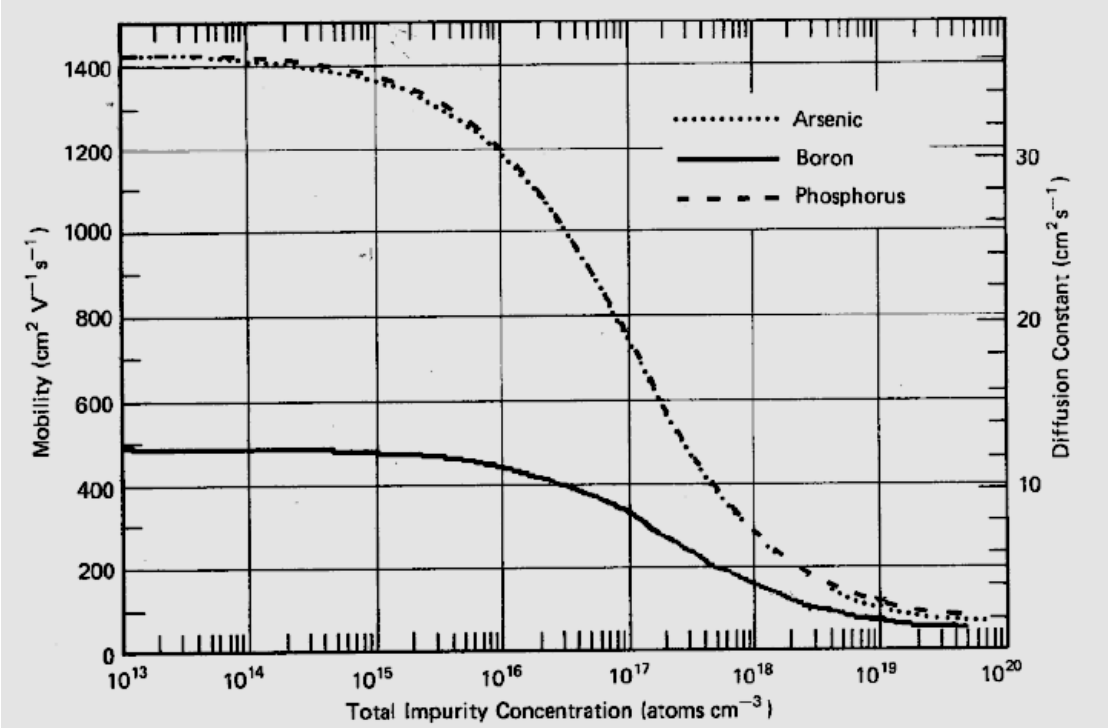
Last (Family) Name:_____

First Name: _____

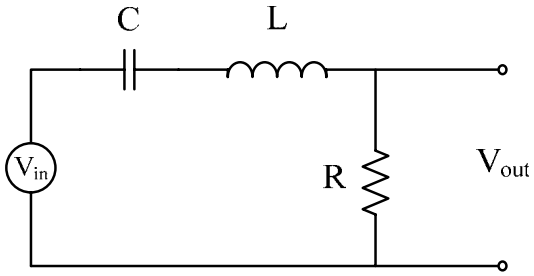
Student ID: _____

Signature: _____

Score:	
Problem 1 (25 pts)	
Problem 2 (25 pts):	
Problem 3 (20 pts):	
Problem 4 (30 pts)	
Total 100 pts	


Arsenic
Boron
Phosphorus
Mobility ($cm^2 V^{-1} s^{-1}$)
Diffusion Constant ($cm^2 s^{-1}$)
Total Impurity Concentration (atoms cm^{-3})
1400
1200
1000
800
600
400
200
0
30
20
10
10^{13}
10^{14}
10^{15}
10^{16}
10^{17}
10^{18}
10^{19}
10^{20}

1. [25 pts] RLC circuit in series. Given: $R = 1 + \frac{1}{\sqrt{10}}\Omega$, $C = 1$ F, and $L = \frac{1}{\sqrt{10}}$ H.



Part a. This is a simple voltage divider:

$$\mathbf{V}_{out} = \mathbf{V}_{in} \frac{\mathbf{Z}_R}{\mathbf{Z}_R + \mathbf{Z}_L + \mathbf{Z}_C}$$

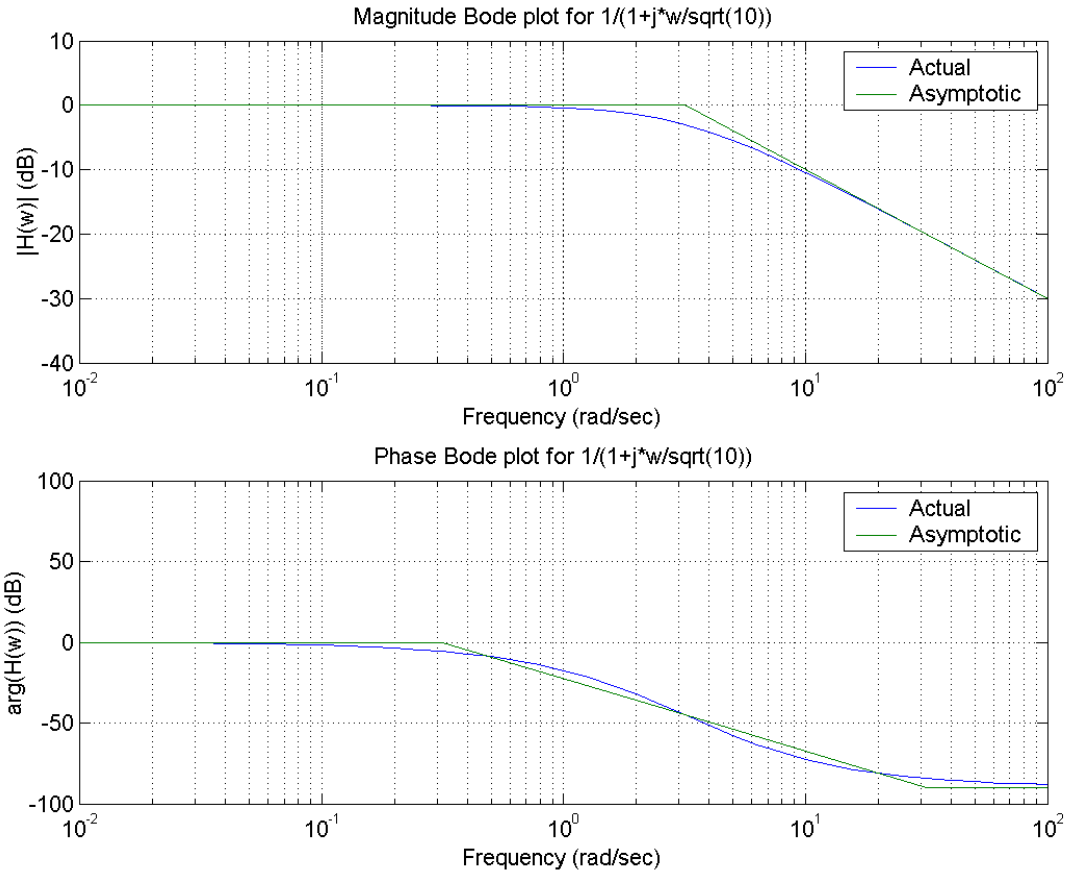
where

$$\mathbf{Z}_R = R$$
$$\mathbf{Z}_L = j\omega L$$
$$\mathbf{Z}_C = \frac{1}{j\omega C}$$

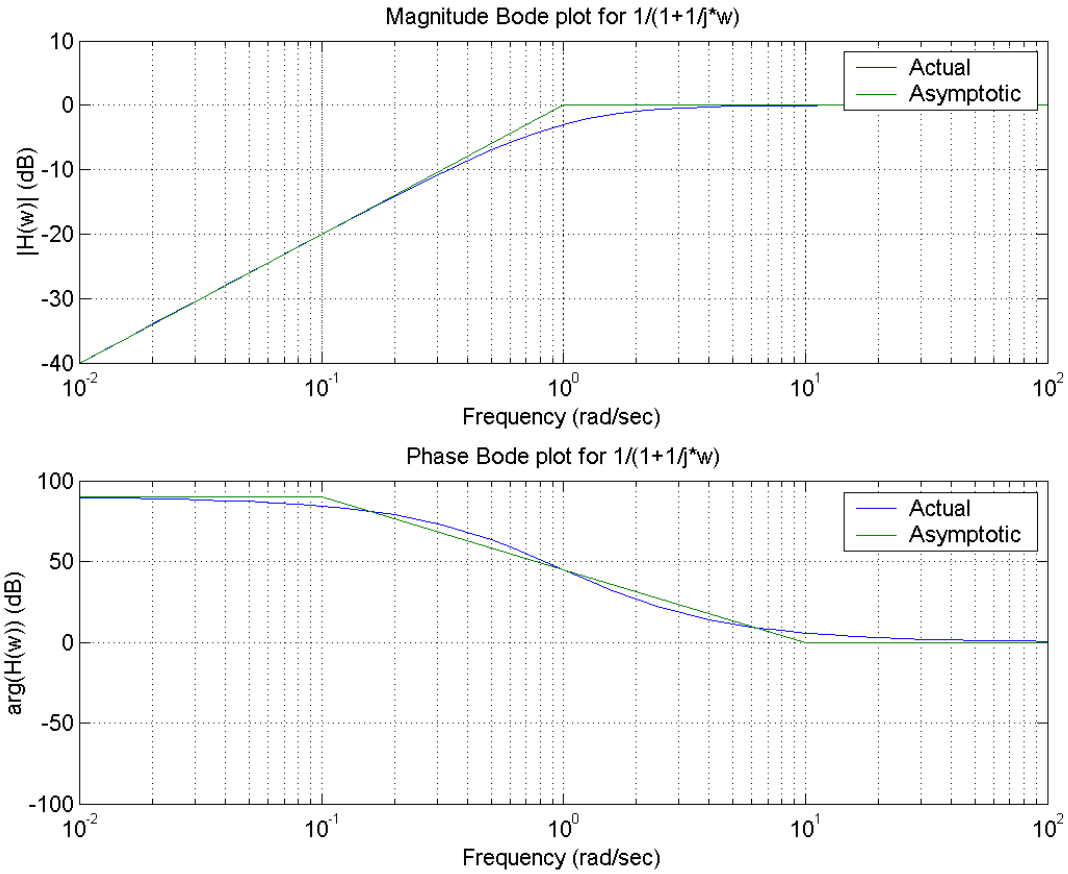
$$H(\omega) = \frac{\mathbf{V}_{out}}{\mathbf{V}_{in}}$$
$$= \frac{R}{R + j\omega L + \frac{1}{j\omega C}}$$
$$= \frac{1 + \frac{1}{\sqrt{10}}}{\frac{j\omega}{\sqrt{10}} + \left(1 + \frac{1}{\sqrt{10}}\right) + \frac{1}{j\omega}}$$
$$= \boxed{\frac{1 + \frac{1}{\sqrt{10}}}{\left(\frac{j\omega}{\sqrt{10}} + 1\right)\left(1 + \frac{1}{j\omega}\right)}}$$

Part b. We can analyze this transfer by breaking it down into first order parts.

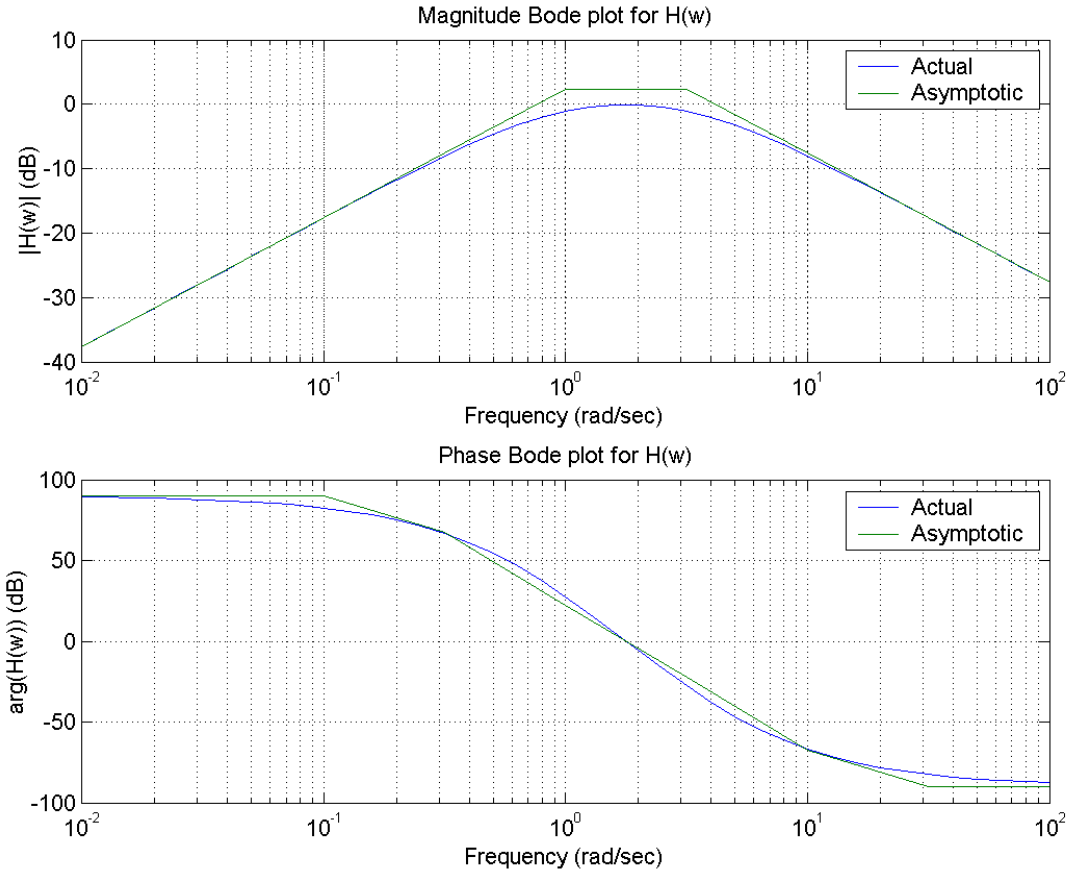
$$\frac{1}{1 + \frac{j\omega}{\sqrt{10}}}:$$


Magnitude Bode plot for 1/(1+j*w/sqrt(10))
|H(w)| (dB)
Frequency (rad/sec)
Actual
Asymptotic
Phase Bode plot for 1/(1+j*w/sqrt(10))
arg(H(w)) (dB)
Frequency (rad/sec)
Actual
Asymptotic

$\frac{1}{1+\frac{1}{j\omega}}$:



$H(\omega)$: We are given that $\log_{10}\left(1+1/\sqrt{10}\right)\approx 0.12$, thus $20\log_{10}\left(1+1/\sqrt{10}\right)\approx 2.4$ dB, which actually is accurate out to the 2nd significant digit. So we can superposition the above two plots and shift the magnitude plot up by 2.4 dB.



Part c. By superposition, we can treat each frequency separately. For ω = 1 rad/sec:

$$H(1) = \frac{1+\frac{1}{\sqrt{10}}}{\left(1+\frac{j}{\sqrt{10}}\right)\left(1+\frac{1}{j}\right)} \approx \frac{1.3\angle 0^\circ}{\left(1\angle 18^\circ\right)\left(1.4\angle -45^\circ\right)}$$

$$|H(1)| \approx \frac{1.3}{1.4} \approx 0.9$$

$$\angle H(1) \approx 0^\circ - 18^\circ - (-45^\circ) = 27^\circ$$

For ω = 10 rad/sec:

$$H(1)=\frac{1+\frac{1}{\sqrt{10}}}{\left(1+j\sqrt{10}\right)\left(1+\frac{1}{j10}\right)}\approx\frac{1.3\angle 0^\circ}{(3.3\angle 72^\bullet)(1\angle -6^\circ)}$$

$$|H(1)|=\frac{1.3}{3.3}=0.4$$

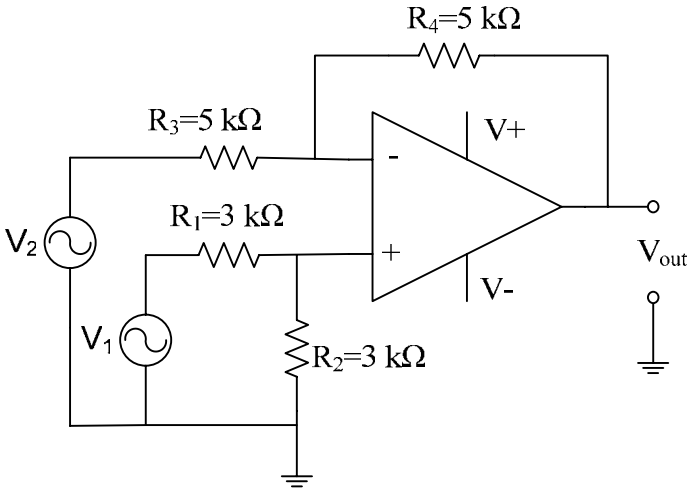
$$\angle H(1)=0^\circ-72^\circ-(-6^\circ)=-66^\circ$$

$$\begin{aligned}\mathbf{V}_{out}&=H(1)\cdot 2\cos t+H(10)\cdot 3\sin 10t\\&=(0.9\angle 27^\circ)\cdot 2\cos t+(0.4\angle -66^\circ)\cdot 3\cos(10t-90^\circ)\\&=1.8\cos(t+27^\circ)+1.2\cos(10t-156^\circ)\end{aligned}$$

The actual answer is:

$$\mathbf{V}_{out}=\boxed{1.775\cos(t+27.45^\circ)+1.185\cos(10t-156.7^\circ)}$$

2. [25 pts] The op-amp is configured as shown in the figure.



(a) Express V_{out} in terms of V_1 and V_2. [5 pts]

Use superposition.

Short V_2 first.

Then we have $V_+ = \frac{3}{3+3}V_1 = \frac{1}{2}V_1$, then $V_- = \frac{5}{5+5}V_{out} = \frac{1}{2}V_{out} = V_+ = \frac{1}{2}V_1$

So we have $V_{out} = V_1$

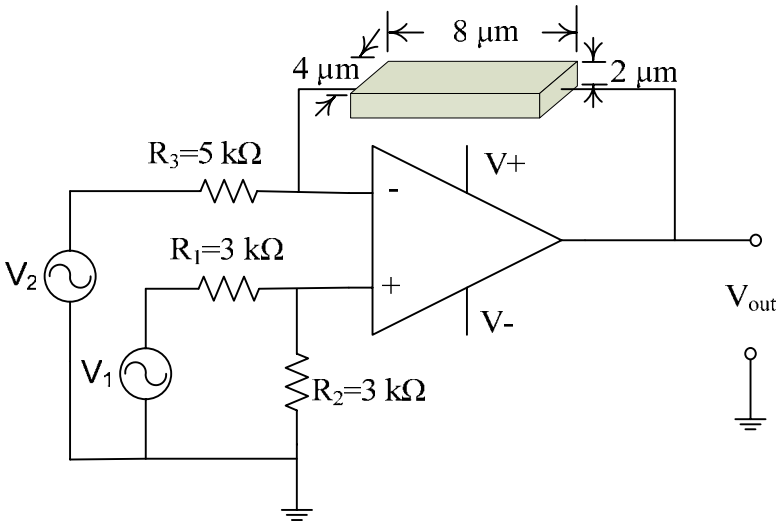
Then we short V_1.

We have $V_+ = V_- = 0$ and $\frac{V_2}{5k} = -\frac{V_{out}}{5k} \Rightarrow V_{out} = -V_2$

Now we superpose the above two results:

$$V_{out} = V_1 - V_2$$

(b) Now resistor R_4 is changed to a piece of Silicon whose dimensions are L=8 μm, T=2 μm, and W=4 μm as labeled in the figure. The Silicon is doped with Boron at a concentration of 3×10^{16} cm^{-3}. Express V_{out} in terms of V_1 and V_2 again. [10 pts]



We need to find the resistance of the Silicon first.

Resistivity is: $\rho = \dfrac{1}{qn\mu_n + qp\mu_p}$

Since boron is acceptors, we have $p \cong N_A = 3\times10^{16}\,cm^{-3}$ and $n = \dfrac{n_i^{\,2}}{p} \cong 3\times10^{3}\,cm^{-3}$.

Since the electron density is much smaller than the hole density, we approximate resistivity as:

$$\rho = \frac{1}{qp\mu_p}$$

Since $N_A + N_D = 3\times10^{16}\,cm^{-3}$, from the mobility chart, we get $\mu_p = 420cm^2/V/s$.

So $\rho = \dfrac{1}{1.6\times10^{-19}\times3\times10^{16}\times420} = \dfrac{1}{2.016} \cong 0.5\Omega cm$

Resistance is: $R = \rho\dfrac{L}{WT} = 0.5\dfrac{8}{4\times2\times10^{-4}} = 5\,\text{k}\Omega$

So the same as (a),

$$V_{out} = V_1 - V_2$$

(c) If we add 5×10^{16} cm^{-3} Phosphorus into the Silicon, what is V_{out} now? [10 pts]

Since phosphorus is a donor, now we have $N_A = 3\times10^{16}\,cm^{-3}$ and $N_D = 5\times10^{16}\,cm^{-3}$.

$N_D - N_A = 2\times10^{16}\,cm^{-3} >> 0$, so $N_D >> N_A$, the material is N-type now. And we have

$n = N_D - N_A = 2\times10^{16}\,cm^{-3}$, $p = \frac{n_i^{\,2}}{n} = 5\times10^{3}\,cm^{-3}$.

Now resistivity can be approximated as $\rho = \frac{1}{qn\mu_n}$

Since $N_A + N_D = 8\times10^{16}\,cm^{-3}$, from the mobility chart, we get $\mu_n = 800cm^2/V/s$

So $\rho = \frac{1}{1.6\times10^{-19}\times2\times10^{16}\times800} = \frac{1}{2.56} \cong 0.4\Omega cm$

Resistance is: $R = \rho\frac{L}{WT} = 0.4\frac{8}{4\times2\times10^{-4}} = 4\,\mathrm{k}\Omega$

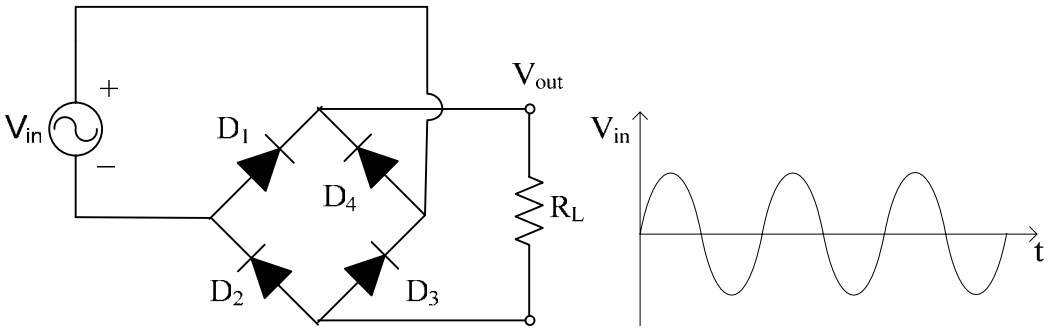
So for V_1, we have $V_- = \frac{5}{5+4}V_{out} = \frac{1}{2}V_1$, so $V_{out} = 0.9V_1$

For V_2, we have $\frac{V_2}{5k} = -\frac{V_{out}}{4k}$, so $V_{out} = -0.8V_2$

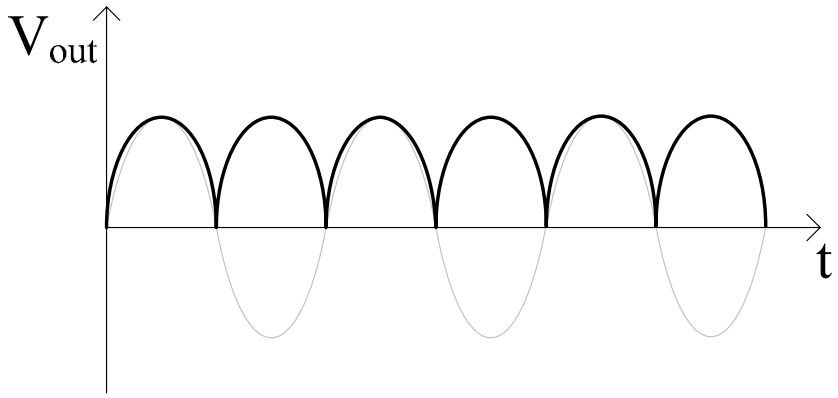
Finally,

$$V_{out} = 0.9V_1 - 0.8V_2$$

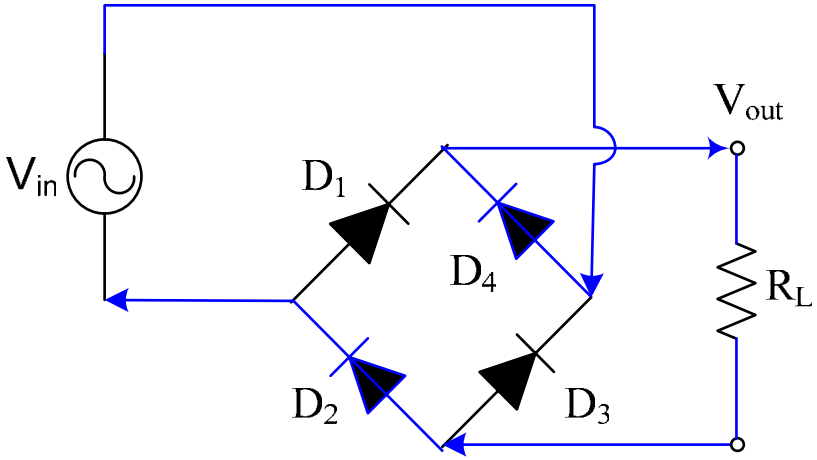
3. [25 pts] Diode rectifier. The input voltage is shown below. Assume all the diodes are ideal and with threshold voltage V_T=0V.



(a) Please draw the output voltage on the load resistor and give explanations. (The input is given as a reference.) [8 pts]

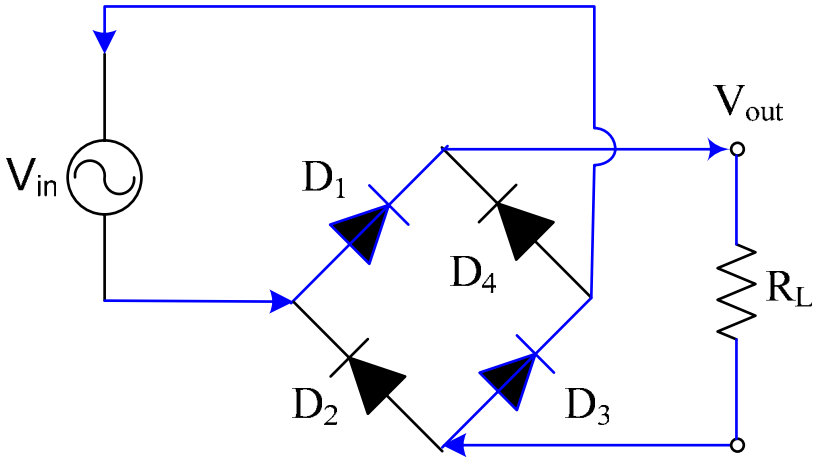


For the V_{in} positive half cycle, the current path is:



D_2 and D_4 are on while D_1 and D_3 are off. So V_{out} on the load resistor is V_{in} positive half cycle.

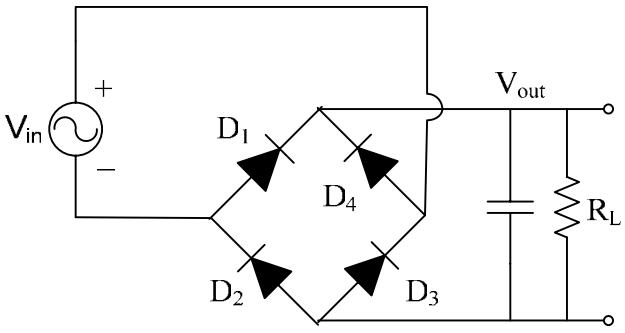
For the Vin negative half cycle, the current path is:

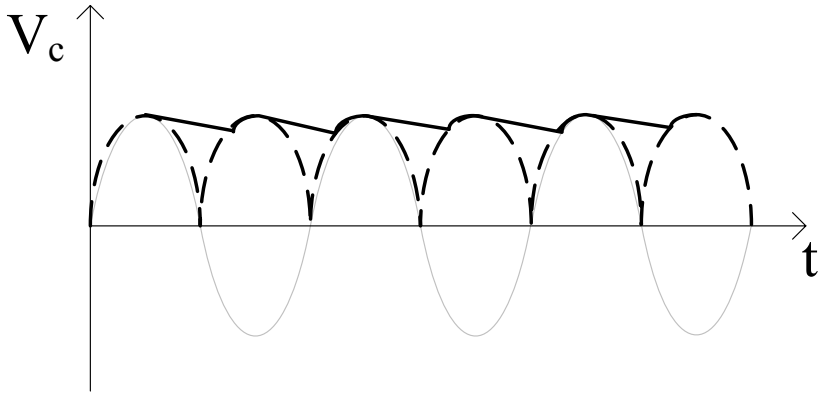


D_1 and D_3 are on while D_2 and D_4 are off. However, the current goes through the resistor in the same direction. So V_{out} on the load resistor for the negative half cycle is the same as it was for the positive half cycle.

So we get V_{out} looks like $|\sin \omega t|$. (Flip the negative half cycle.)

(b) If we put a large capacitor in stead of the resistor at the output as shown below, what is the voltage of the capacitor? Please draw the output you got in (a) as well for a reference and give explanations. [8 pts]





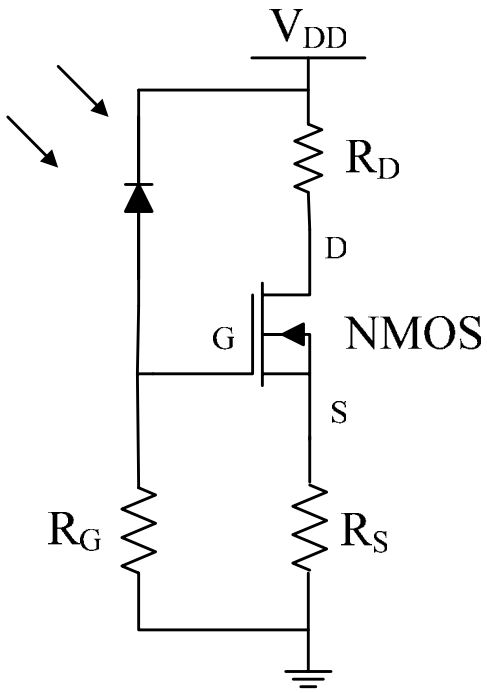
Consider the steady state.

The capacitor is charged up to the peak value when the input signal reaches its maximum. Then the input signal starts to drop, thus the capacitor is discharging. Since it's a large capacitor, it is being discharged slowly. By the time the absolute value of the input voltage is higher than it is on the capacitor, it's being charged again, which makes V_c to the peak value again.

(c) Which one do you think is more efficient in getting DC power, (a) or (b)? Why? [4 pts]

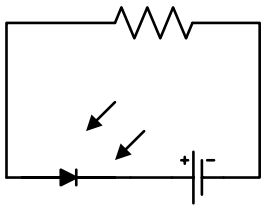
(b) is more efficient, since the average power is higher. Or area below the output is larger.

4. [30 pts] A photodetector (reverse biased photodiode) is connect to an NMOSFET as shown in the figure. We know V_{DD}=5 V, R_G=10 kΩ, R_D=50 Ω and R_S=200 Ω.



(a) The photodetector I-V characteristics are known as shown in the I_p-V_p plot below. When it is dark, it follows the top curve, while when it is under a certain amount of light, it shifts down. Now given that the light intensity is exactly the amount that makes the photodiode follow the bottom curve, please draw the load line of the photodiode on the I_p-V_p plot below, label its operating point and give the V_{pQ}, I_{pQ} values of the operating point. [10 pts]

The current loop of the photodetector is

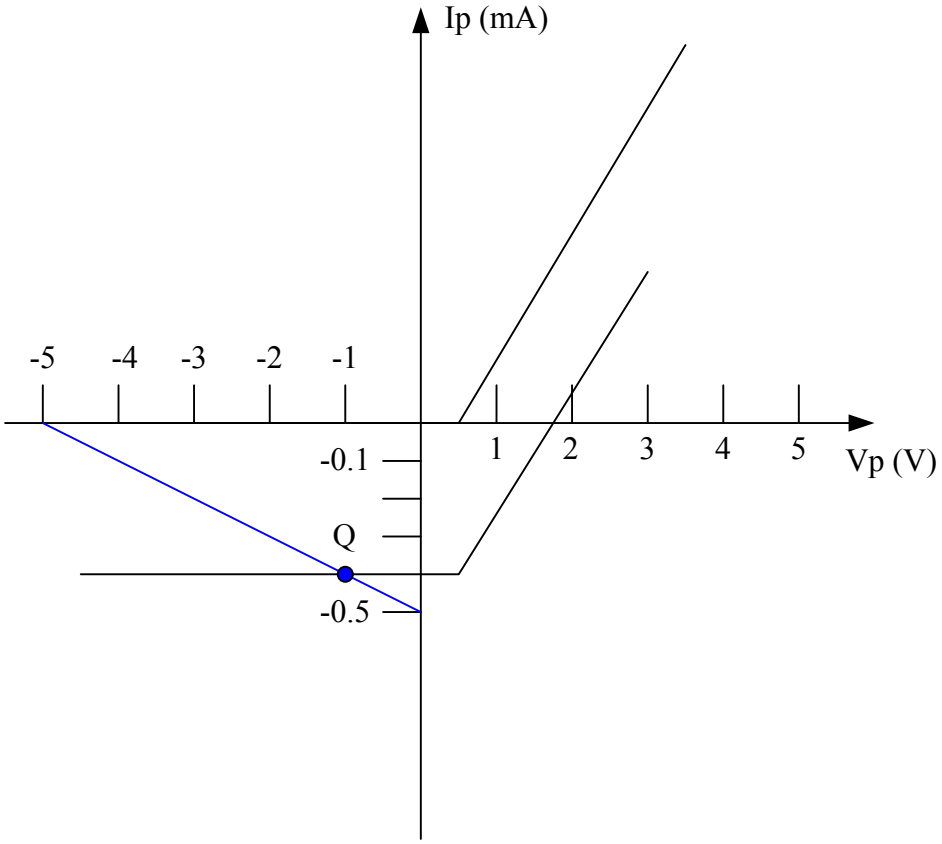


So the load line equation is: $V_{DD} = -V_p - I_p R_G$. Note that we put negative sign before V_p and

I_p, because the photodiode is reverse biased. Put the values of V_{DD} and R_G in, we get $5 = -V_p - I_p 10k$ and we draw this on the plot.

Since we know from the characteristics that the photocurrent now is -0.4 mA under reverse bias, so I_p= -0.4 mA and from the load line equation, we know immediately that V_p= -1V.

V_{pQ}= -1V	I_{pQ}= -0.4mA



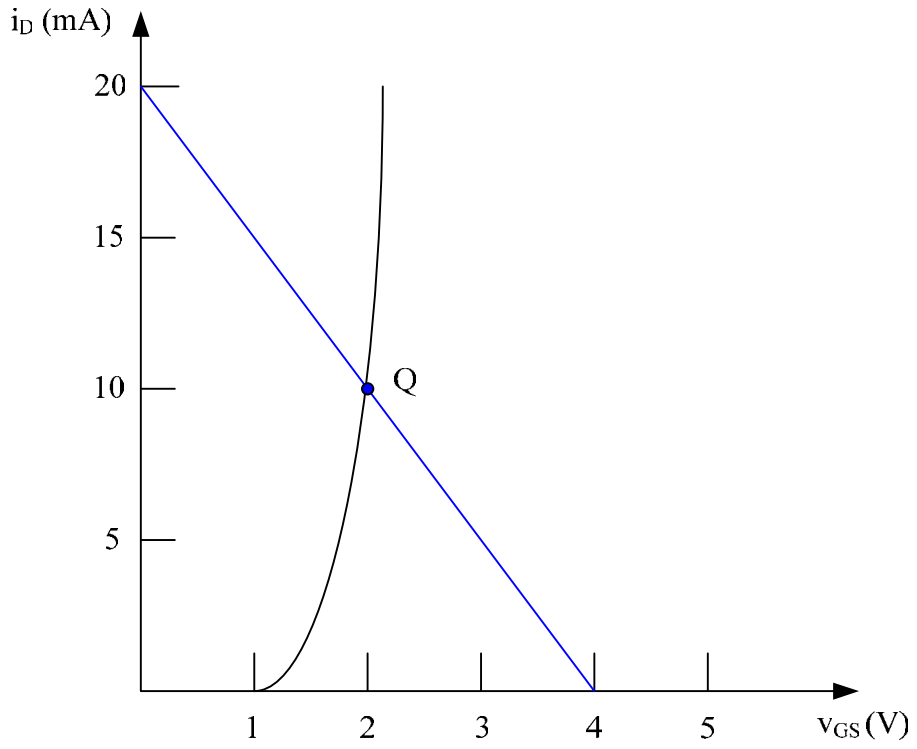
(b) Given the v_{GS}-i_D characteristics of the MOSFET which is shown in the v_{GS}-i_D plot below, please draw the load line on this plot, label the operating point Q of the MOSFET and give v_{GSQ} and i_{DQ} values of the operating point. [10 pts]

From the circuit configuration, we apply the KVL at gate and source and get the load line equation

$$v_{GS} = R_G I_p - i_D R_S = 10k \times 0.4m - i_D 200 = 4 - 200 i_D \Rightarrow v_{GS} = 4 - 200 i_D$$

We draw this on the v_{GS}-i_D plot. And from the MOSFET characteristics, we read the values of the operating point.

V_{GSQ}= 2 V	i_{DQ}= 10 mA



(c) Given the v_{DS}-i_D characteristics of the MOSFET which is shown in the v_{DS}-i_D plot below, please draw the load line on this plot, label the operating point Q of the MOSFET and give v_{DSQ} value of the operating point. [10 pts]

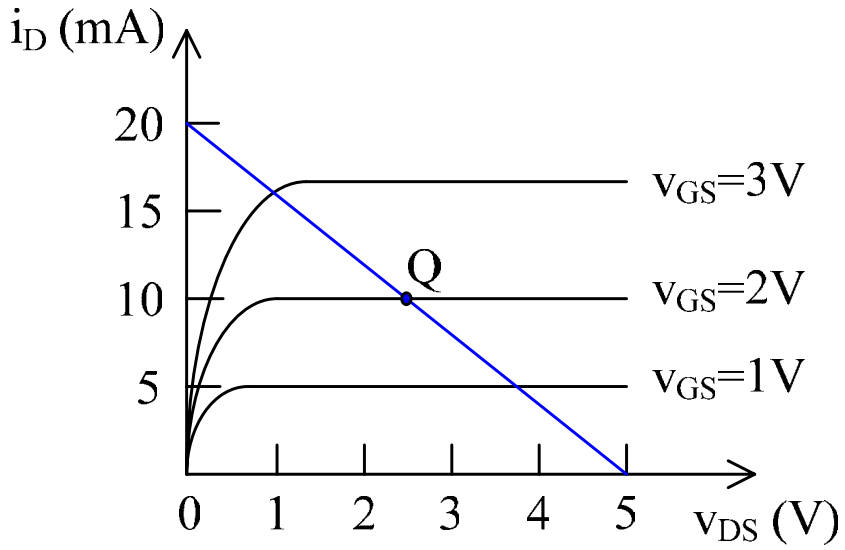
Apply KVL from VDD through drain and source to the ground.

We get the load line equation $V_{DD} = i_D R_D + v_{DS} + i_D R_s = i_D(200+50) + v_{DS}$

$v_{DS} = V_{DD} - 250 i_D = 5 - 250 i_D$

We draw this line on the plot below. Since the VGS is 2 V, the Q point will be on the middle curve. Since we know from question (b) that i_D is 10 mA, so v_{DS}=2.5 V

V_{DSQ}= 2.5 V



EECS 40, Spring 2005
Prof. Chang-Hasnain
Final Exam Solutions

Friday, May 13, 2005
12:30-3:30 pm
Total Time Allotted: 180 minutes

1. This is a closed book exam. However, you are allowed to bring THREE page (8.5" x 11"), double-sided notes
2. No electronic devices, i.e. calculators, cell phones, computers, etc.
3. Numerical answers within a factor of 1.5 will not get points deducted, provided the steps are all correct and the errors are due to the lack of a calculator. (e.g. if the correct answer is 1, the acceptable range will be 0.67~1.5).
4. SHOW all the steps on the exam. Answers without steps will be given only a small percentage of credits. Partial credits will be given if you have proper steps but no final answers.
5. Write your answers in the spaces (lines, boxes or plots) provided.
6. Remember to put down units. Points will be taken off for answers without units.
7. FYI: nH=10^{-9} H; pF=10^{-12} F; GHz=10^{9} Hz; MHz=10^{6} Hz

Last (Family) Name:_____

First Name: _____

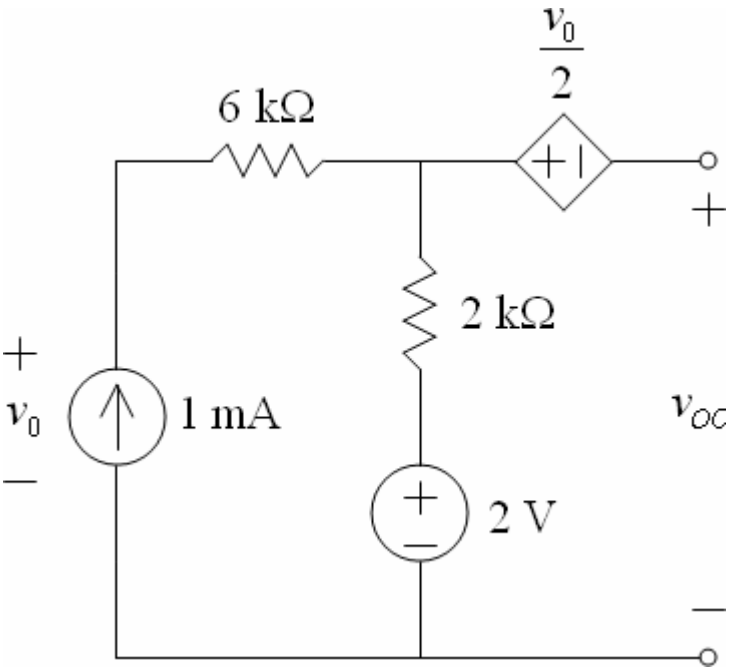
Student ID: _____

Signature: _____

Score:	
Problem 1 (20 pts)	
Problem 2 (60 pts):	
Problem 3 (40 pts):	
Problem 4 (40 pts):	
Problem 5 (40 pts):	
Total 200 pts	

1: [20 pt] Equivalent Circuit

Find R_{eq}, I_{sc}, and V_{oc} at the terminals indicated and draw the Thevenin equivalent circuit. (All answers should be numeric and not contain V_0)



Set current i_1 going through 6k to the right, i_2 going through 2k down.

Open circuit to calculate V_{oc}

$$i_1 = 1\,\text{mA}$$

$$V_0 = 6000i_1 + 2000i_1 + 2 = 6 + 4 = 10\,\text{V}$$

$$V_{oc} = 2 + 2000i_1 - \frac{v_0}{2} = 2 + 2 - 5 = -1\,\text{V}$$

Short circuit to calculate I_{sc}

$$i_1 - i_2 = 6 - i_2 = I_{sc}$$

$$v_0 = 6000i_1 + 2000i_2 + 2$$

$$\frac{v_0}{2} = 2 + 2000i_2$$

$v_0 = 12\,\text{V}$ and $i_2 = 2\,\text{mA}$

$$I_{sc} = -1\,\text{mA}$$

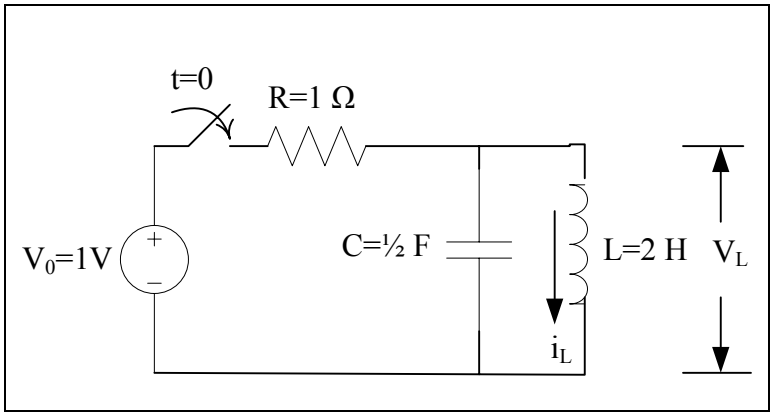
$$R_{eq} = \frac{V_{oc}}{I_{sc}} = 1\,\text{k}\Omega$$

R_{eq}= 1 kOhm	V_{oc}= -1 V	I_{sc}= -1 mA
Thevenin equivalent:		

2. [60 pt] 2nd order circuit

Part I: Transient Analysis: For t<0, the switch is open and had been open for long. There is no charge on the capacitor. At t=0, the switch is closed.

(a) [6 pt] What are the initial conditions for V_L and i_L?



Since there was no charge when t<0 and the switch was open, there was no current and voltage on the inductor. Thus $V_L(0)=I_L(0)=0$.

$V_L(0)=0$	$i_L(0)=0$

(b) [10 pt] KVL equation of the circuit in terms of $i_L(t)$?

KVL: $V_0 = i_R R + V_L$

$$i_R = i_L + i_C$$

$$V_L = L\frac{di_L}{dt},\ i_C = C\frac{dV_L}{dt} = CL\frac{d^2 i_L}{dt^2}$$

$$\therefore i_R = i_L + CL\frac{d^2 i_L}{dt^2}$$

$$V_0 = i_L R + LCR\frac{d^2 i_L}{dt^2} + L\frac{di_L}{dt}$$

$$\frac{d^2 i_L}{dt^2} + \frac{1}{RC}\frac{di_L}{dt} + \frac{1}{LC}i_L = \frac{V_0}{LCR}$$

With the numbers given:

$$\frac{d^2 i_L}{dt^2} + 2\frac{di_L}{dt} + i_L = V_0$$

KVL in terms of $i_L(t)$: $\frac{d^2 i_L}{dt^2} + \frac{1}{RC}\frac{di_L}{dt} + \frac{1}{LC}i_L = \frac{V_0}{LCR}$ or $\frac{d^2 i_L}{dt^2} + 2\frac{di_L}{dt} + i_L = V_0$

(c) [12 pt] If V_0=1 V, R=1 Ω, C=1/2 F, and L=2 H, calculate ω_0 , α, and ζ. Is the circuit underdamped, critically damped or overdamped?

From the KVL equation gotten in (b)

$$2\alpha = \frac{1}{RC} \Rightarrow \alpha = \frac{1}{2RC} = 1$$

$$\omega_0{}^2 = \frac{1}{LC} \Rightarrow \omega_0 = \frac{1}{\sqrt{LC}} = 1$$

$$\zeta = \frac{\alpha}{\omega_0} = 1$$

So it's critically damped.

$\omega_0 = 1$	$\alpha = 1$	$\zeta = 1$	Damping case: Critically damped

(c) [12 pt] What is the solution of $V_L(t)$?

Solve $i_L(t)$ first since the second order differential equation is in term of $i_L(t)$.

Particular solution:

$i_{Lp} = 1$ from inspection.

Complementary solution for critically damped case:

$$i_{Lc}(t) = K_1 e^{s_1 t} + K_2 t e^{s_1 t}$$

So the solution is:

$$i_L(t) = K_1 e^{s_1 t} + K_2 t e^{s_1 t} + 1$$

From the initial conditions gotten in (a),

$$i_L(0) = K_1 + 1 = 0 \Rightarrow K_1 = -1$$

$$V_L(0) = L\left.\frac{di_L}{dt}\right|_{t=0} = -s_1 e^{s_1 t} + K_2 t s_1 e^{s_1 t} + K_2 e^{s_1 t}\Big|_{t=0} = -s_1 + K_2 = 0 \Rightarrow K_2 = s_1$$

$$s_1 = -\alpha = -1$$

$$\therefore K_2 = -1$$

$$\therefore i_L(t) = -e^{-t} - te^{-t} + 1$$

$$V_L(t) = L\frac{di_L}{dt} = 2\left(e^{-t} - e^{-t} + te^{-t}\right) = 2te^{-t}$$

$V_L(t)$: $2te^{-t}$ (V)

Part II: Steady State Frequency Analysis: Use complex impedance to analyze the circuit.

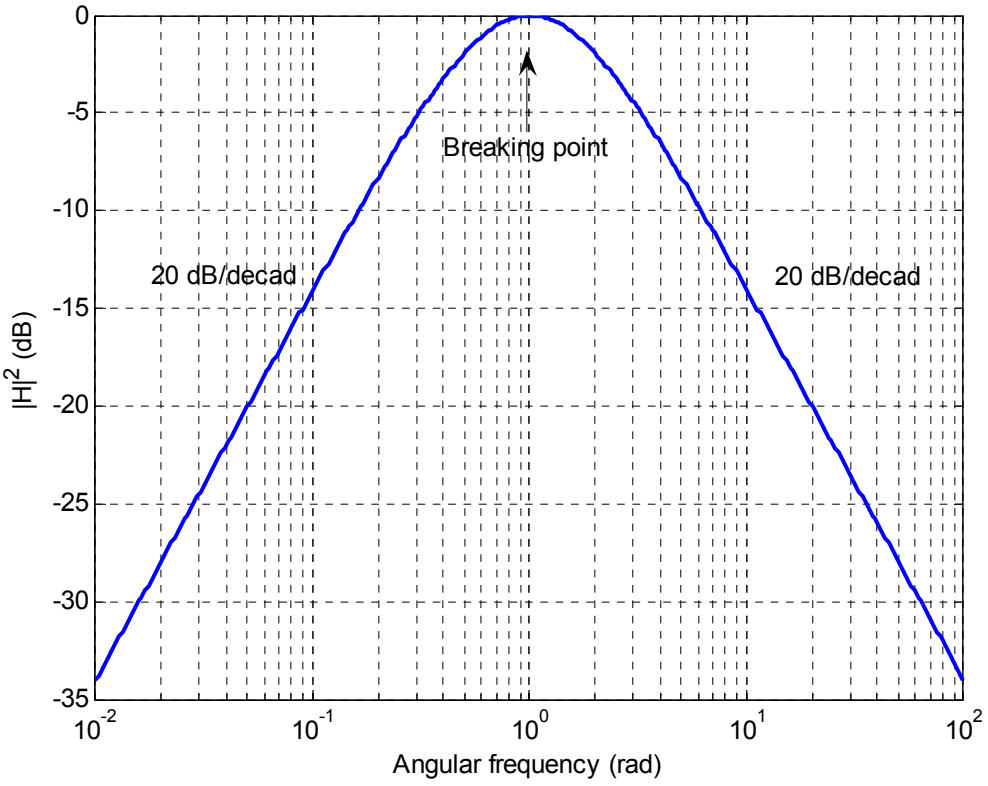
(e) [10 pt] What is the transfer function $H(\omega)=\frac{V_L}{V_0}$ of this circuit if V_0 is a sinusoidal source?

$$H(\omega)=\frac{\frac{L/C}{\frac{1}{j\omega C}+j\omega L}}{\frac{L/C}{\frac{1}{j\omega C}+j\omega L}+R}=\frac{j\omega L}{R+j\omega L-\omega^2 LCR}=\frac{2j\omega}{1+2j\omega-\omega^2}=2\frac{1}{j\omega+1}\cdot\frac{j\omega}{j\omega+1}$$

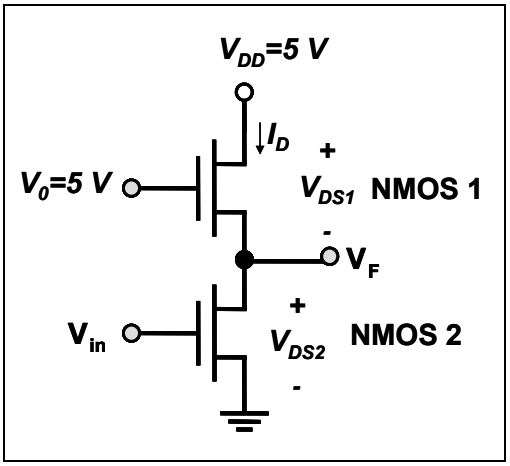
$$H(\omega)=\frac{j\omega L}{R+j\omega L-\omega^2 LCR}=\frac{2j\omega}{1+2j\omega-\omega^2}=2\frac{1}{j\omega+1}\cdot\frac{j\omega}{j\omega+1}$$

(f) [10 pt] Draw magnitude Bode plot of the transfer function. Please label all the important features (slopes, break points etc.) and axes. (*Hint: Draw it versus angular frequency*)

Magnitude Bode plot:



3. [40 pt] NMOS Circuit DC Analysis



Let $V_0=V_{DD}=5V$. Two **identical** NMOS put in series, with parameters are KP = 50 uA/V^2, V_t=1V, L=1 um, W=40um. The I_D vs. V_{DS} curves for various V_{GS} values are shown below.

(a) [10 pt] What values of V_{in} can make NMOS2 **NOT** be in the cutoff region?

Based on the fact $V_0=V_{DD}$, what mode(s) (cut-off, saturation or triode) can NMOS1 be in when NMOS2 is **NOT** in the cutoff region?

When $V_{in} > V_{t2,}$ NMOS2 is no longer in cutoff region. So $V_{in} > 1$ V.

Based on the fact that $V_0=V_{DD}$

$$V_{GS1} = V_0 - V_F = 5 - V_F$$
$$V_{DS1} = V_{DD} - V_F = 5 - V_F$$
$$\therefore V_{DS1} = V_{GS1} > V_{GS1} - V_t$$

So when NMOS2 is on, NMOS1 is always in saturation mode.

Range(s) of V_{in} where NMOS2 is on:	Mode(s) of NMOS1:
V_{in}>1 V	Saturation

(b) [5 pt] Write down I_D as a function of gate-source voltage of NMOS1 when NMOS2 is on.

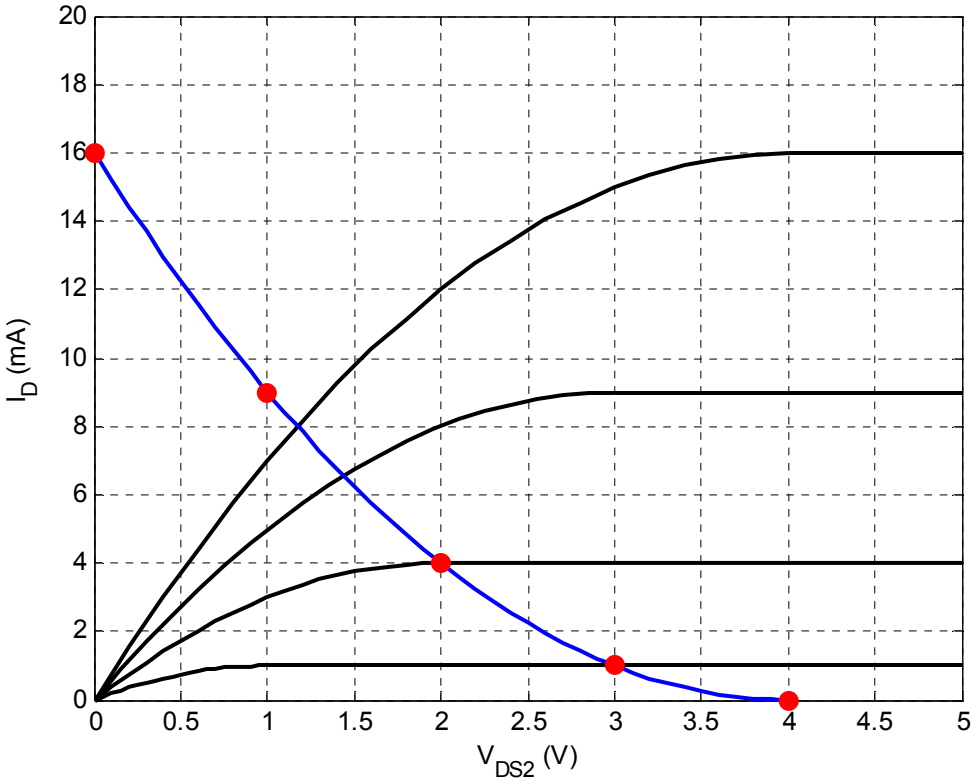
Since two NMOSFETs are in series, they share the same current. ID is the saturation current of NMOS1.

$$I_D = \frac{KP}{2}\frac{W}{L}\left(V_{GS1} - V_t\right)^2 = \frac{KP}{2}\frac{W}{L}\left(V_0 - V_F - V_t\right)^2 = \left(4 - V_F\right)^2$$

$I_D = \left(4 - V_F\right)^2$

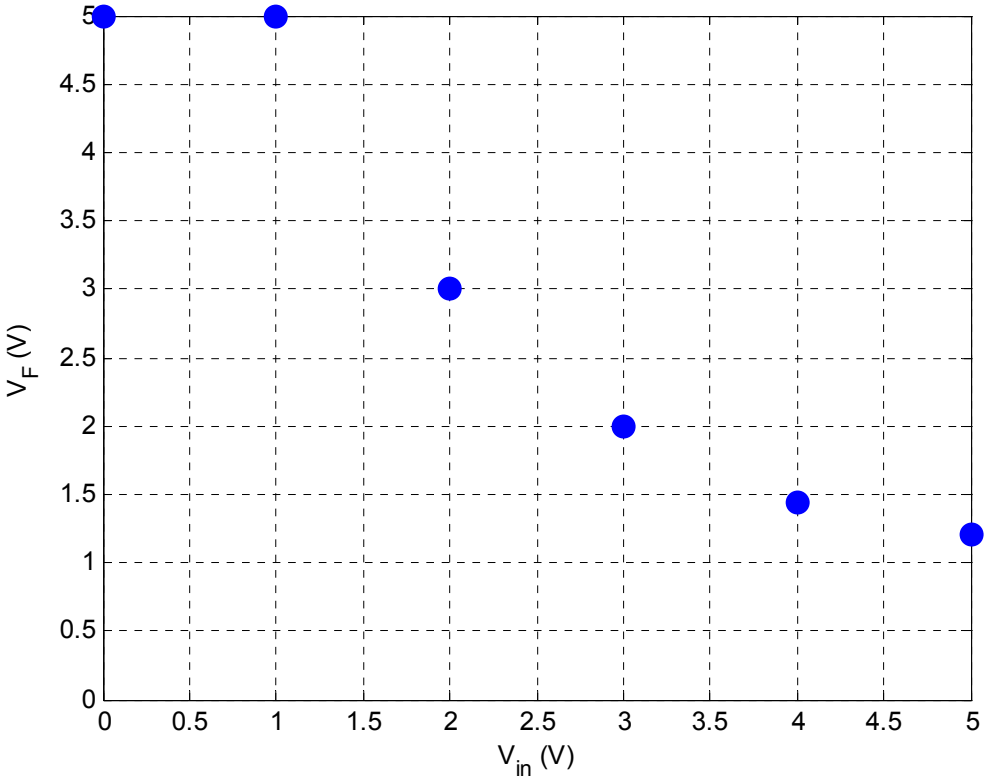
(c)[10 pt] Sketch I_D (that you got in (b)) vs. V_F onto the figure below, which is the I_D vs V_{DS} for NMOS2. Label key points with values. (*Hint: Take V_F=0,1,2,3,4 V, then sketch)*

V_F (V)	0	1	2	3	4
I_D (mA)	16	9	4	1	0



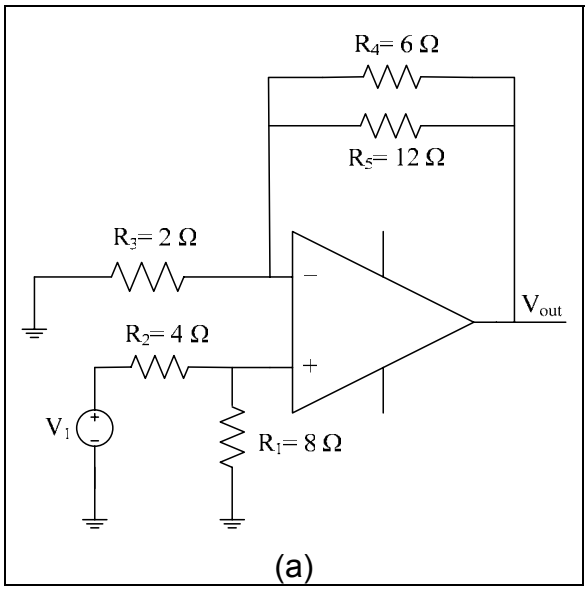
(d) [15 pt] Sketch V_F vs V_{in} for V_{in} ranging from 0 to 5V. Label V_F Values for V_{in}=0, 1, 2, 3, 4, 5 V.

V_{in} (V)	0	1	2	3	4	5
V_F (V)	5	5	3	2	1.44	1.2



4. [40 pt] Op-Amp

(a) [15 pt] Please express V_{out} in terms of V_1 as shown in Figure (a).



$$V_+ = V_- = \frac{R_1}{R_1 + R_2} V_1 = \frac{8}{4+8} V_1 = \frac{2}{3} V_1$$

$$R_4 // R_5 = \frac{1}{\frac{1}{6} + \frac{1}{12}} = 4\Omega$$

$$\therefore \frac{R_3}{R_3 + R_4 // R_5} V_{out} = V_- = \frac{2}{3} V_1$$

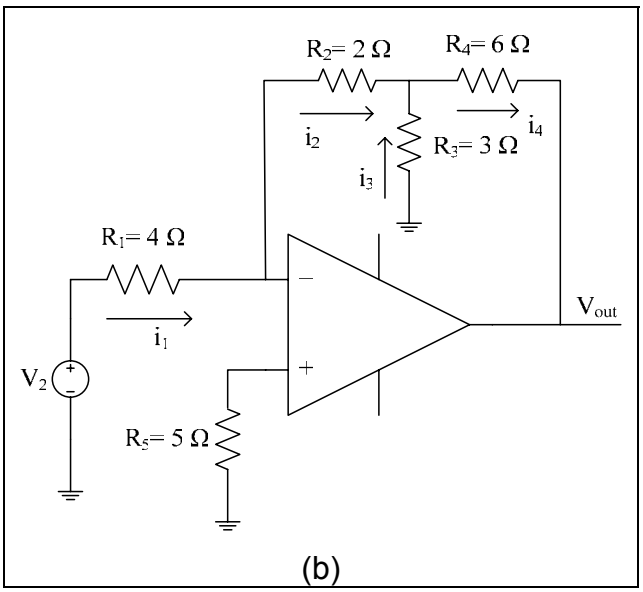
$$\frac{2}{2+4} V_{out} = \frac{2}{3} V_1$$

$$\frac{1}{3} V_{out} = \frac{2}{3} V_1$$

$$V_{out} = 2V_1$$

$V_{out}= 2V_1$

(b) [15 pt] Please express V_{out} in terms of V_2 as shown in Figure (b).

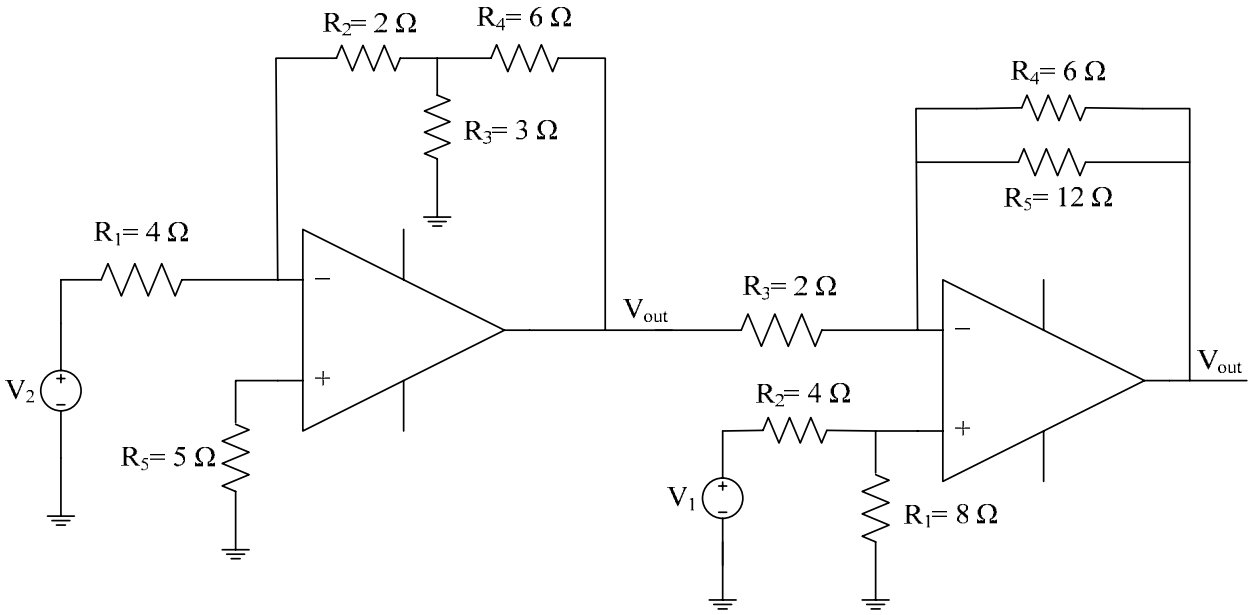


(b)

$$V_+ = V_- = 0$$
$$V_1 = i_1 R_1$$
$$i_1 = i_2$$
$$i_4 = i_2 + i_3$$
$$i_2 R_2 = i_3 R_3$$
$$V_{out} = -i_2 R_2 - i_4 R_4$$
$$= -i_1 R_2 - (i_2 + i_3) R_4$$
$$= -\frac{V_1}{R_1} R_2 - \left(i_1 + \frac{R_2}{R_3} i_1 \right) R_4$$
$$= -\frac{V_1}{R_1} R_2 - \left(1 + \frac{R_2}{R_3} \right) \frac{V_1}{R_1} R_4$$
$$= -\frac{2}{4} V_1 - \left(1 + \frac{2}{3} \right) \frac{V_1}{4} 6$$
$$= -3V_1$$

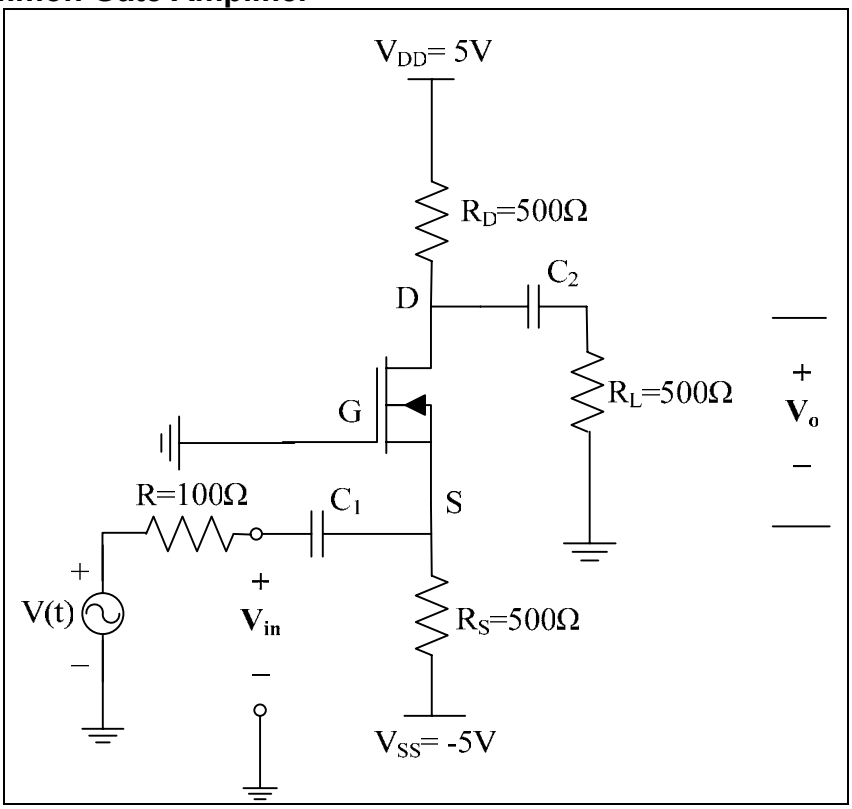
V_{out}= -3V_1

(c) [10 pt] Please draw a structure using (a) and (b) only to realize the operation $2V_1+6V_2$. Please do not change the resistor network configuration of (a) and (b) and do not add any other components.



Just connect the output of the inverting op-amp to R_3 of the non-inverting op-amp.

5: [40 pt] Common Gate Amplifier



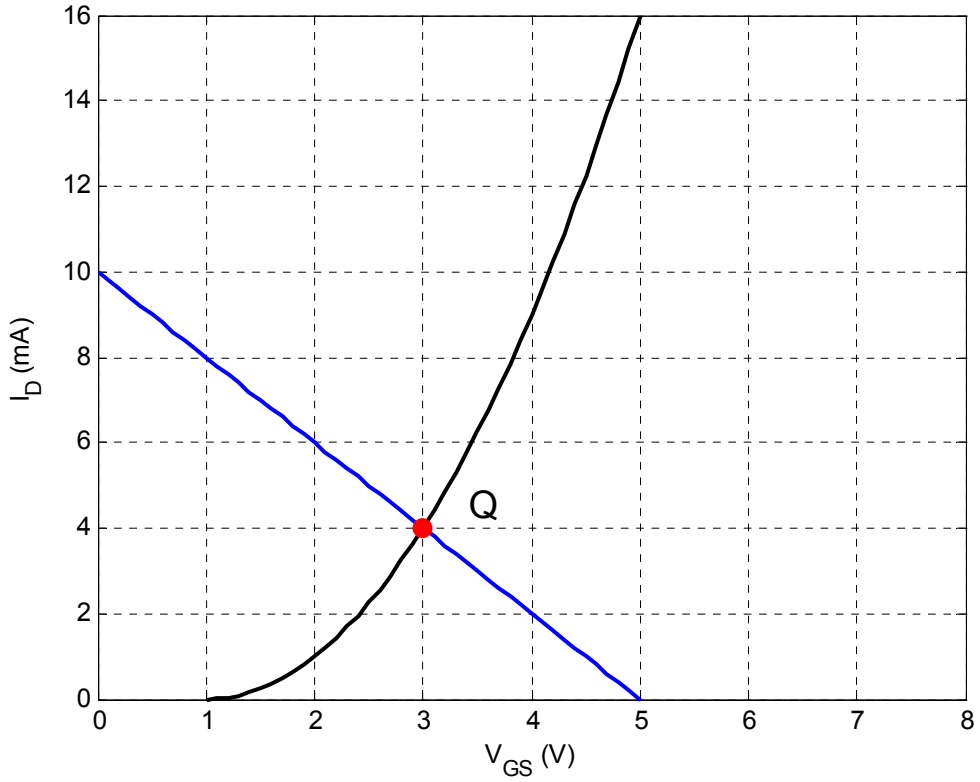
Consider an NMOS with KP = 50 uA/V^2, V_t=1V, L=1 um, W=40um. R_S =R_D = R_L=500 Ω

(a) [10 pt] Q point analysis: What are $V_{GSQ,}$ I_{DQ} and V_{DSQ}? Please derive load line equations and draw load lines on the following graphs.

Apply KVL on the loop GS-Vss

$$V_{GS} + R_S I_D + V_{SS} = 0$$
$$V_{GS} = 5 - 500 I_D$$

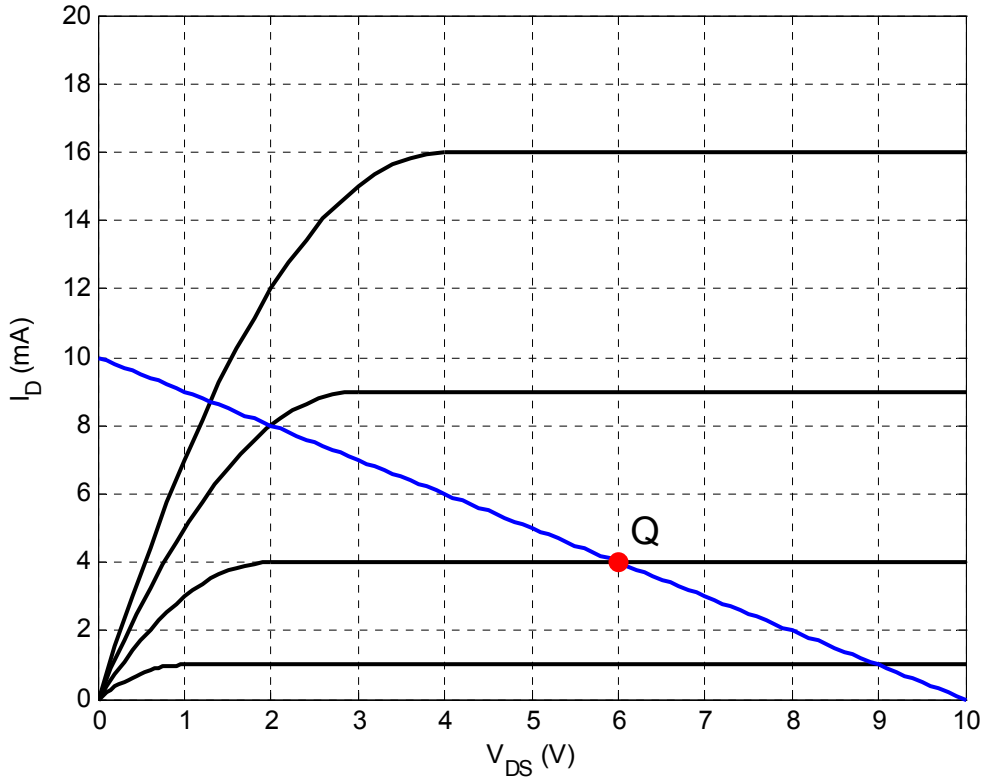
Draw this load line on the following figure.



Apply KVL to the loop from V_{DD} to Vss.

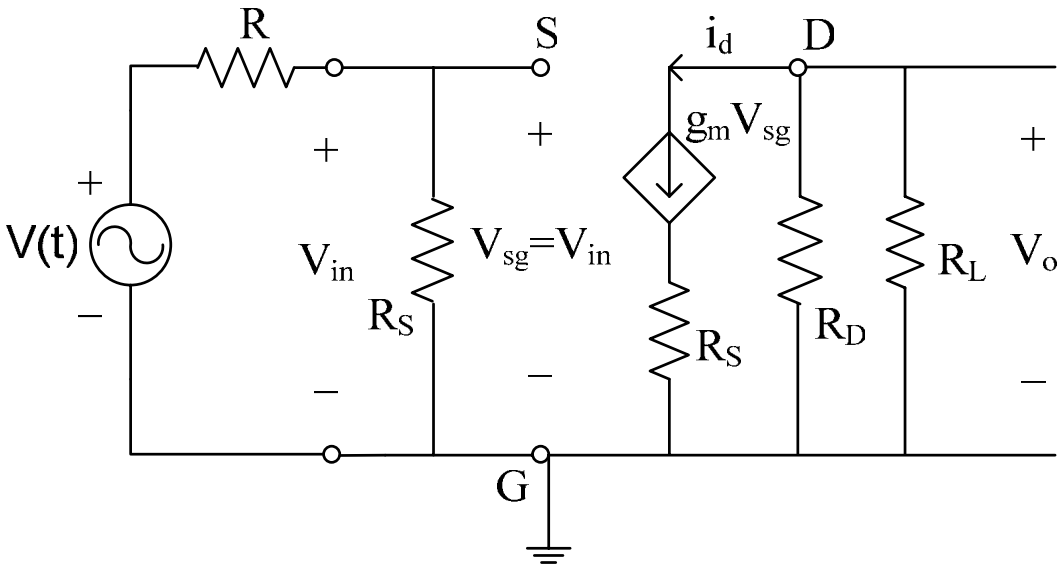
$$V_{DD} - V_{SS} = I_D(R_D + R_S) + V_{DS}$$
$$10 = I_D 1000 + V_{DS}$$

Plot this load line on the following figure.



V_{GSQ}= 3 V	I_{DQ}= 4 mA	V_{DSQ}= 6 V

(b) [10 pt]Small signal analysis: Draw the small signal model. Indicate all relevant value(s).



(c) [10 pt] Calculate small signal voltage gain A_v. (*Hint:* $\sqrt{0.1} \approx 0.32$)

$$g_m = \sqrt{2KP}\sqrt{W/L}\sqrt{I_{DQ}} = \sqrt{2\times 50\times 10^{-3}\times 40\times 4\times 10^{-3}} = 0.128$$

$$R_{//} = R_D \,//\, R_L = 250\Omega$$

$$V_0 = -(g_m V_{sg})R_{//} = -(g_m V_{in})R_{//}$$

$$A_v = \frac{V_0}{V_{in}} = -g_m R_{//} = -0.128\times 250 = -32$$

A_V= - 32

(d) [10 pts] Calculate input impedance R_{in} and output impedance R_o.

From the small signal model. It's obvious to find
$R_{in}=R_S$ and $R_o=R_D$

$R_{in}= R_S$	$R_o=R_D$