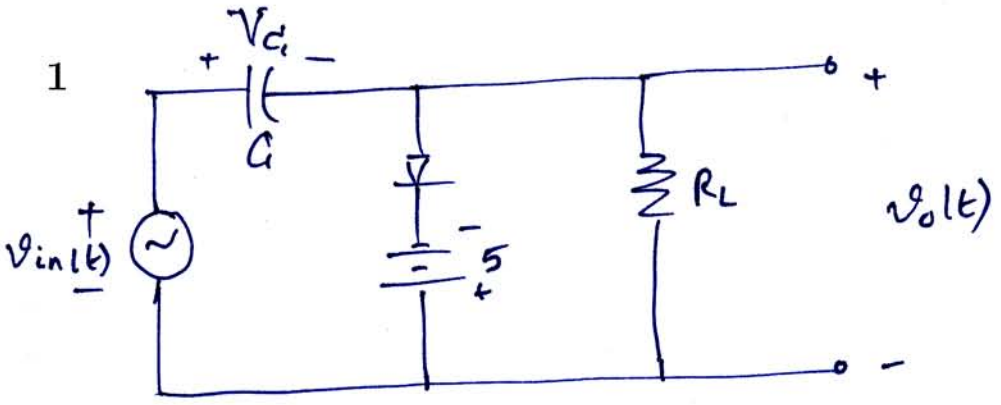
1

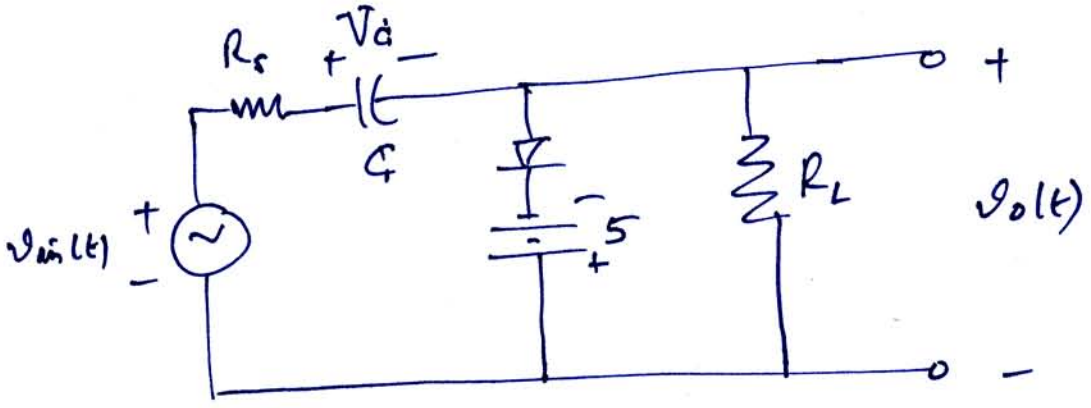


This is the circuit drawn in the book (Figure 10.33). The diode is assumed to be ideal.

2

We should really have a small resistance in series with the input voltage to avoid potential inconsistencies, which could arise because the model assumes: (1) the input voltage source can be chosen as we wish; and (2) the voltage across the capacitor cannot suddenly jump (if the diode is conducting these two requirements could contradict each other).

Here is the redrawn circuit. The series resistance R_s will be assumed to be extremely small, and will be neglected for the rest of the discussion.



3

We first analyze the circuit with $v_{in}(t) = V_m \sin(\omega t)$. Note that $V_m \geq 0$ in this case. We assume that

$$R_L C >> \frac{2\pi}{\omega}.$$

We think of the circuit started at time $-\infty$ (way back in the past) with the capacitor uncharged. Now, the diode short-circuits whenever the voltage across it attempts to go positive. At such times the capacitor will charge up. When the voltage we attempt to put across the diode goes negative, the diode become an open circuit. During such times the built-up charge on the capacitor hardly leaks out, because of the assumed condition $R_L C >> \frac{2\pi}{\omega}$. The capacitor will therefore charge up to a level which is barely sufficient to make the diode almost always be in an open circuit condition (i.e. such that the diode short-circuits for a duration that is very short and just enough to compensate for the charge lost from the capacitor during a cycle). This means that we can think of the capacitor as having charged up to a dc level V_C satisfying

$$V_m = V_C + (-5),$$

i.e. $V_C = V_m + 5$. This means that

$$v_o(t) = v_{in}(t) - V_C = v_{in}(t) - V_m - 5.$$

Thus the output voltage is a level-shifted version of the input voltage, retaining its shape, so that the upper peak has become clamped to -5 volts. See Figure 10.34 (b) of the text.

4

Next we analyze the circuit with $v_{in}(t) = V_d + V_a \sin(\omega t)$. comprised of a dc-level V_d and an ac-component $V_a \sin(\omega t)$. Let $V_m = V_d + V_a$ denote the peak input voltage. Note that V_m can have any sign in this case. We assume that

$$R_L C >> \frac{2\pi}{\omega}.$$

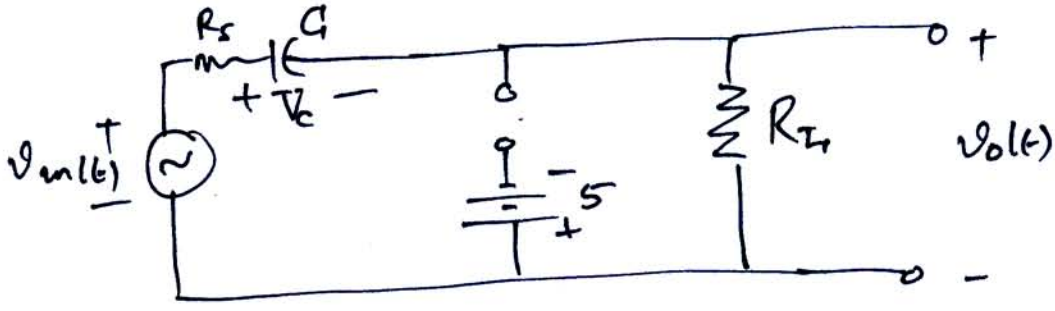
As before, we think of the circuit started at time $-\infty$ (way back in the past) with the capacitor uncharged.

If $V_m > -5$, the analysis proceeds exactly as in the preceding case. The capacitor can be viewed as having charged up to the level $V_C = V_m + 5$ (note that this is a positive voltage) which is the level that is barely enough to keep the diode an open circuit through almost the entire cycle, becoming a short circuit for just long enough at the peak of the cycle to compensate for the charge lost from the capacitor during a cycle (which is very little, because $R_L C >> \frac{2\pi}{\omega}$). Once again, the output voltage is

$$v_o(t) = v_{in}(t) - V_C = v_{in}(t) - V_m - 5,$$

and we see that the circuit acts to level-shift the input voltage to clamp its top level at -5 V.

If $V_m < -5$, the analysis is more subtle. At first sight it may seem that the diode is never going to be a short circuit. Suppose we start with this hypothesis. Then we are analyzing the circuit:



This is a linear circuit, that can be handled by superposition. We think of the input as being the sum of a dc part V_d and an ac part $V_a \sin(\omega t)$, The capacitor can be thought of as a short for ac, so we would conclude that $V_C = V_d$. This would mean that the diode supports a positive biased drop of 5V across it, which is absurd. Thus the assumption that the diode is always an open circuit is absurd (note: there is a big difference between *always* an open circuit and *almost always* an open circuit!).

We can understand this situation by noting that, starting way back in the past with the capacitor initially uncharged, the diode will be an open circuit and current will flow in the rest of the circuit to charge the capacitor to a

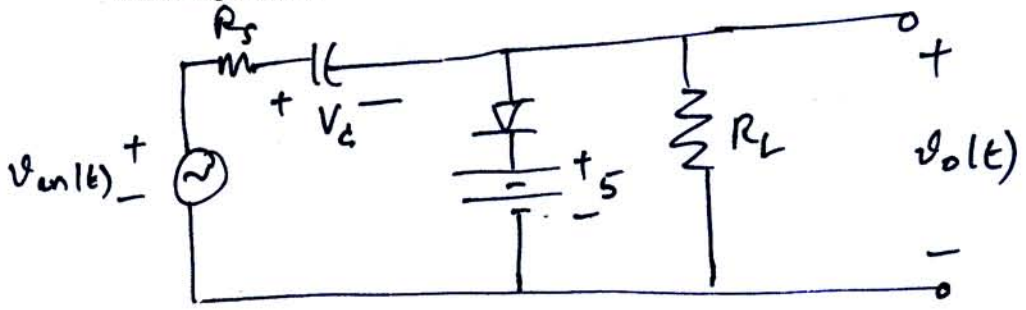
negative voltage. This will occur up to the point where the diode barely short-circuits at the peak of each cycle. Once again, the formula this gives is $V_C = V_m + 5$ (note now that this is negative!) and once again we get

$$v_o(t) = v_{in}(t) - V_C = v_{in}(t) - V_m - 5,$$

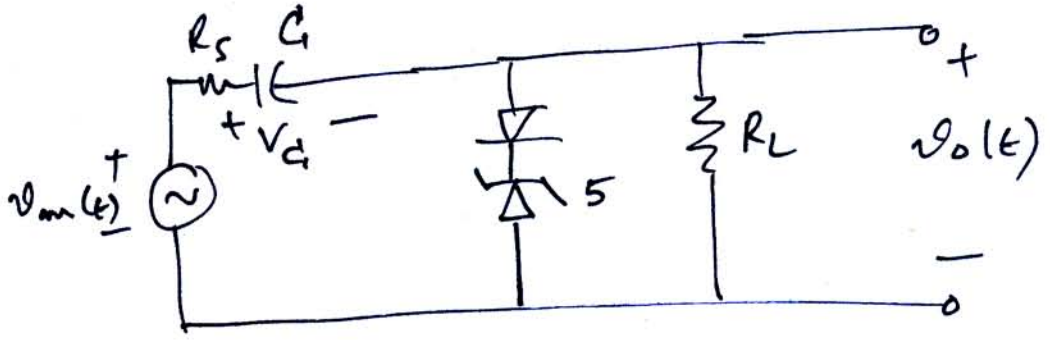
so this circuit works as a clamp circuit in this case also.

5

We next attempt design a clamp circuit that level-shifts the input voltage to give an output clamped at a peak of 5V. The first thing to try would be the following circuit:



This is exactly like the circuit of Figure 10.33 of the text, except that the DC voltage source has been flipped. Note that we could also have attempted to realize this by instead using a Zener diode with a breakdown voltage of 5V as in the following circuit:



We will call the former circuit the VS circuit and the latter circuit the ZD circuit. The entire discussion below applies to either circuit.

6

We first analyze the VS circuit and the ZD circuit with $v_{in}(t) = V_m \sin(\omega t)$. Note that $V_m \geq 0$ in this case. We assume that

$$R_L C >> \frac{2\pi}{\omega}.$$

We think of the circuit started at time $-\infty$ (way back in the past) with the capacitor uncharged.

Assume first that $V_m > 5$. Then the analysis proceeds exactly as in Section 3. The diode short-circuits whenever the voltage across it attempts to go positive (in either circuit). At such times the capacitor will charge up. When the voltage we attempt to put across the diode goes negative, the diode become an open circuit. During such times the built up charge on the capacitor hardly leaks out, because of the assumed condition $R_L C >> \frac{2\pi}{\omega}$. The capacitor will therefore charge up to a level which is barely sufficient to make the diode almost always be in an open-circuit condition. This means that we can think of the capacitor as having charged up to a dc level V_C satisfying

$$V_m = V_C + 5,$$

i.e. $V_C = V_m - 5$. This means that

$$v_o(t) = v_{in}(t) - V_C = v_{in}(t) - V_m + 5.$$

Thus the output voltage is a level-shifted version of the input voltage, retaining its shape, so that the upper peak has become clamped to 5V.

However, if we have $V_m < 5$ we have a problem! This is because there is no mechanism for the capacitor to charge. We will have the diode *always* an open circuit (in both the VS circuit and the ZD circuit), with $V_C = 0$ and $v_o(t) = v_{in}(t)$. In fact, even if the capacitor was initialized with some charge at $-\infty$, this charge will eventually leak out and the steady state situation

will be the one just described. Thus, in this situation (i.e. when $V_m < 5$) this circuit (either the VS circuit or the ZD circuit) *does not* act as a clamp circuit. This situation is illustrated in Figure 10.34 (c) of the text. In the phraseology of your book (see pp. 493 -494) what is going on is that "the desired clamp voltage causes the diode to be reverse biased". In making this statement he is comparing 5 to V_m and this situation occurs when $5 > V_m$. Note that in the analysis of Section 3 with $V_d = 0$, we could never have $-5 > V_m$, because $V_m > 0$.

7

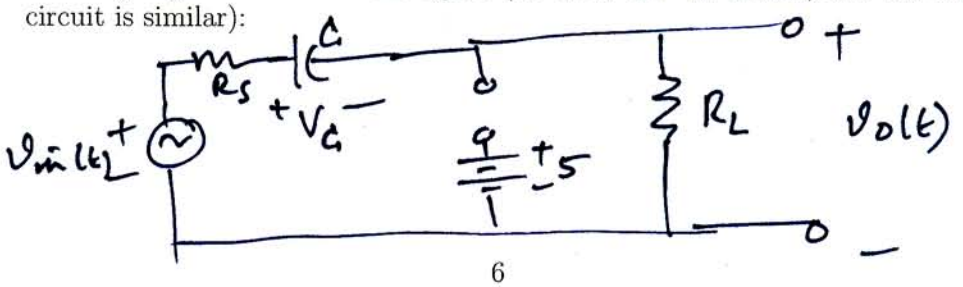
We next analyze the VS circuit and the ZD circuit with $v_{in}(t) = V_d + V_a \sin(\omega t)$. Let $V_m = V_d + V_a$ denote the peak input voltage. Note that V_m can have any sign in this case. We assume that

$$R_L C >> \frac{2\pi}{\omega}.$$

We think of the circuit started at time $-\infty$ (way back in the past) with the capacitor uncharged.

If $V_m > 5$ the analysis proceed exactly as before (in either the VS circuit or the ZD circuit). The capacitor charges up to a dc level $V_C = V_m - 5$ (note that this is positive). This means that $v_o(t) = v_{in}(t) - V_m + 5$. Thus the output voltage is a level-shifted version of the input voltage, retaining its shape, so that the upper peak has become clamped to 5V.

If $V_m < 5$ the analysis is more subtle. It may seem that the diode will *always* be an open circuit. Let us assume that this is true. Then we will be analyzing the circuit in the figure (we drew the VS circuit, but the ZD circuit is similar):



This is a linear circuit, which can be analyzed using superposition. The input voltage is thought of as having the dc part V_d and the ac part $V_a \sin(\omega t)$. We can think of the capacitor as a short circuit for ac. Under the assumption on the diode, we will then have $V_C = V_d$ in steady state. This would mean that the voltage across the diode in steady state is $V_a \sin(\omega t) - 5$. This would be okay if $V_a < 5$, but it would be absurd if $V_a \geq 5$. Thus we get two subcases, described below.

Subcase 1: Given $V_m < 5$, if we also have $V_a < 5$, then we will have $V_C = V_d$, the diode will always be an open circuit, and we will have

$$v_o(t) = v_{in}(t) - V_C = V_a \sin(\omega t).$$

Note that (either the VS or the ZD) circuit *does not* act as a clamp circuit in this subcase.

Subcase 2: Given $V_m < 5$, if we have $V_a \geq 5$, the capacitor will charge up to the voltage required to barely make the diode a short circuit for a brief period during a cycle, i.e we will have $V_C = V_m - 5$ (note that this is now negative) and $v_o(t) = v_{in}(t) - V_m + 5$. Thus the output voltage is a level-shifted version of the input voltage, retaining its shape, so that the upper peak has become clamped to 5V.

We now appreciate that the statement in your book, "the desired clamp voltage causes the diode to be reverse biased", should be interpreted as comparing 5 to V_a (note that V_m equals V_a in the case $V_d = 0$). When $5 > V_a$ we are in the bad case. Note that in the analysis of Section 3 we could never have $-5 > V_a$, irrespective of what V_d is, because $V_a > 0$, so we could never be in a bad case.

The upshot is that the VS circuit and ZD circuit do not always function as desired (when we want to clamp the input voltage to a postive upper level). In the next lecture we will see how to fix this.

8

Returning to the discussion of the case $V_m > 5$ in the second paragraph of Section 7, you should now realize that this analysis is incomplete, and in fact wrong! As stated in that paragraph, if $V_m > 5$ the capacitor initially charges up to the positive dc level $V_m - 5$. Let us write this as $V_C^0 = V_m - 5$, since we are not yet sure that this is going to be the eventual value of V_C. There are now two subcases.

Subcase where $V_d < V_m - 5$: Note that this is equivalent to $V_a > 5$. Consider

$$v_{in}(t) - V_C^0 = V_d + V_a \sin(\omega t) - (V_d + V_a - 5) = 5 - V_a + V_a \sin(\omega t).$$

You can think of this as the voltage being presented across the diode branch when the capacitor has charged up to V_C^0. Note that this voltage has a *negative* dc part (because $V_a > 5$). This implies that the diode cannot stay always cut off. To see this, we analyze the linear circuit corresponding to the diode branch always cut off as we did in the preceding section. In that circuit the remaining negative dc component $5 - V_a$ would like to eventually drop entirely across the capacitor. Thus it will try to make V_C even more negative, thus constantly trying to lift the voltage across the diode branch above 5, which is prevented by the diode becoming a short for brief periods around the peak of each cycle. Thus in this case we indeed have $v_o(t) = v_{in}(t) - V_m + 5$ and the circuit works as desired. Also we can write V_C for V_C^0 in this case, because this is indeed the (approximate) steady state value of the capacitor voltage.

Subcase where $V_d > V_m - 5$: Note that this is equivalent to $V_a < 5$. As in the preceding subcase, consider

$$v_{in}(t) - V_C^0 = V_d + V_a \sin(\omega t) - (V_d + V_a - 5) = 5 - V_a + V_a \sin(\omega t),$$

which can be thought of as the voltage being presented across the diode branch when the capacitor has charged up to V_C^0. Note that this voltage has a *positive* dc part (because $V_a > 5$). This implies that *the diode will be always cut off*. To see this, we analyze the linear circuit corresponding to the diode branch always cut off as we did in the preceding section. In that

circuit the remaining positive dc component $5 - V_a$ would like to eventually drop entirely across the capacitor *and it is able to do that*. Thus we will eventually have $V_C = V_C^0 + 5 - V_a = V_d$. In steady state, we then have

$$v_o(t) = v_{in}(t) - V_C = V_a \sin(\omega t).$$

Thus the circuit does not function as desired in this case.

We see that, as mentioned at the end of Section 7, whether the circuit works or not *always* depends on how 5 compares to V_a, irrespective of what V_m is. In the next lecture we will see how to fix the remaining problem with this circuit.