EE40
Lecture 4
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1/30/08

Reading: Chap. 2

Parallel, Series, Voltage and Current Dividers

Circuit Nodes and Loops

- A ***node*** is a point where two or more circuit elements are connected.
- A ***loop*** is formed by tracing a closed path in a circuit through selected basic circuit elements without passing through any intermediate node more than once

Kirchhoff's Laws

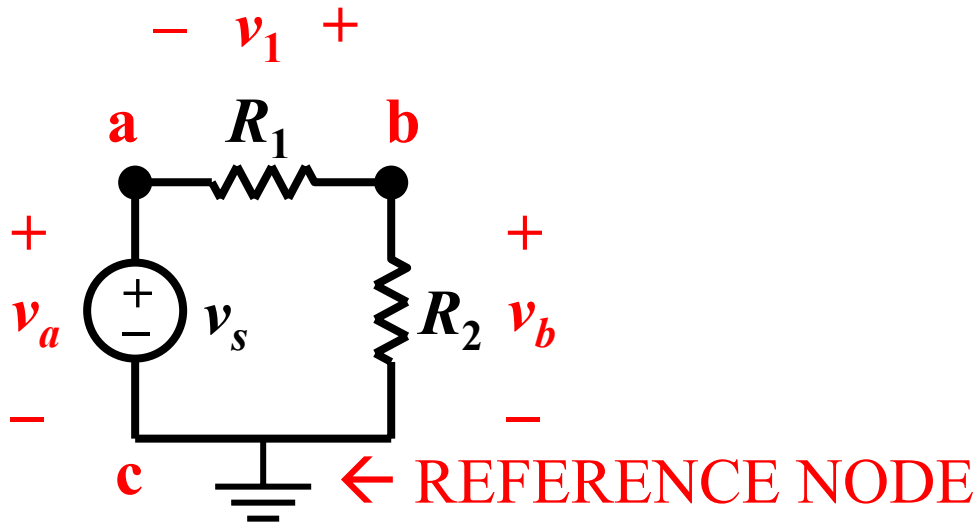
- **Kirchhoff's Current Law (KCL):**
  - The algebraic sum of all the **currents** entering any **node** in a circuit equals zero.
- **Kirchhoff's Voltage Law (KVL):**
  - The algebraic sum of all the **voltages** around any **loop** in a circuit equals zero.

Gustav Robert Kirchhoff
1824-1887

Notation: Node and Branch Voltages

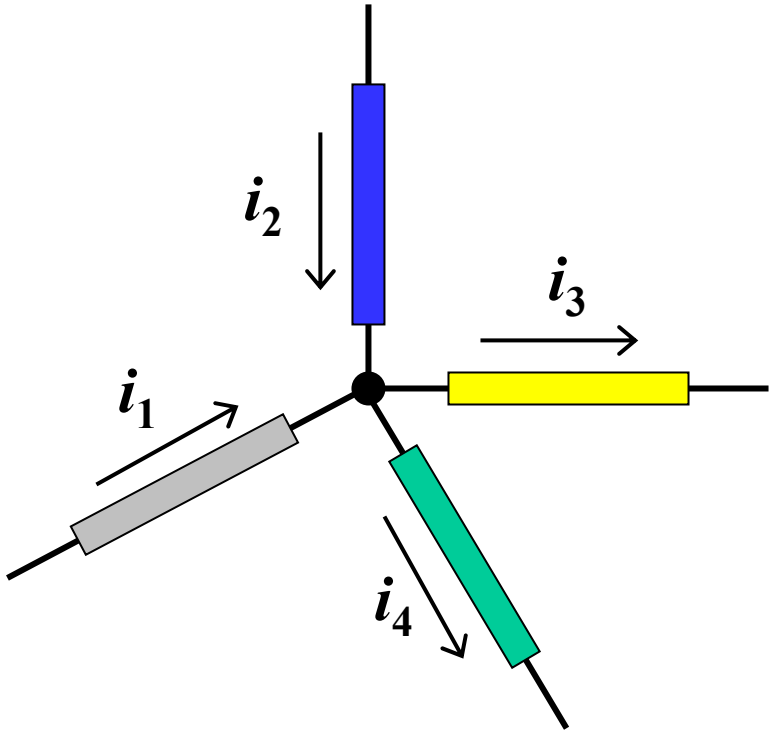
- Use one node as the reference (the "common" or "ground" node) – label it with a symbol
- The voltage drop from node **x** to the reference node is called the **node voltage v_x**.
- The voltage across a circuit element is defined as the difference between the node voltages at its terminals

Example:



Using Kirchhoff's Current Law (KCL)

Consider a node connecting several branches:



- Use **reference directions** to determine whether currents are "entering" or "leaving" the node – with no concern about actual current directions

Formulations of Kirchhoff's Current Law

(Conservation of charge)

Formulation 1:

Sum of currents entering node
= sum of currents leaving node

Formulation 2:

Algebraic sum of currents entering node = 0

- Currents leaving are included with a minus sign.

Formulation 3:

Algebraic sum of currents leaving node = 0

- Currents entering are included with a minus sign.

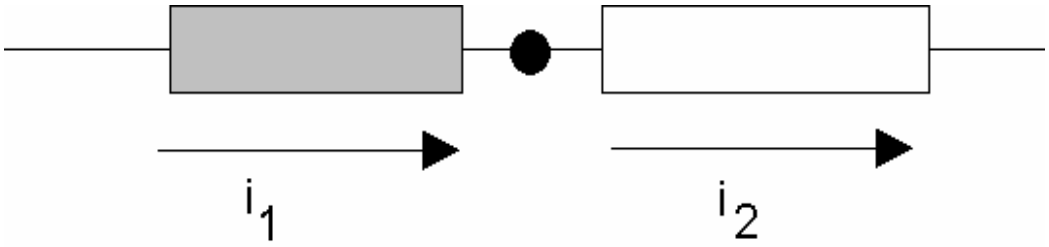
An Underlying Assumption of KCL

- All ways by which charge can enter or leave the node have been included in the circuit model.

  In integrated circuits there are leakage currents. These will need to be modeled into the circuit model for KCL to be applicable.

A Major Implication of KCL

- KCL tells us that **all of the elements in a single branch carry the same current**.
- We say these elements are connected ***in series***.



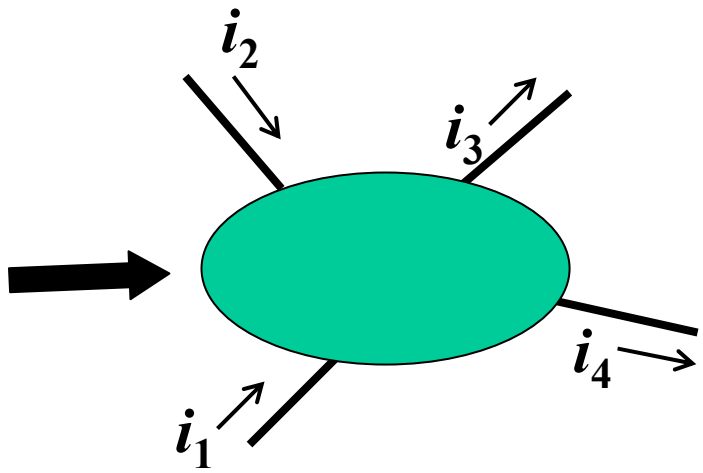
Current entering node = Current leaving node

$$i_1 = i_2$$

Generalization of KCL

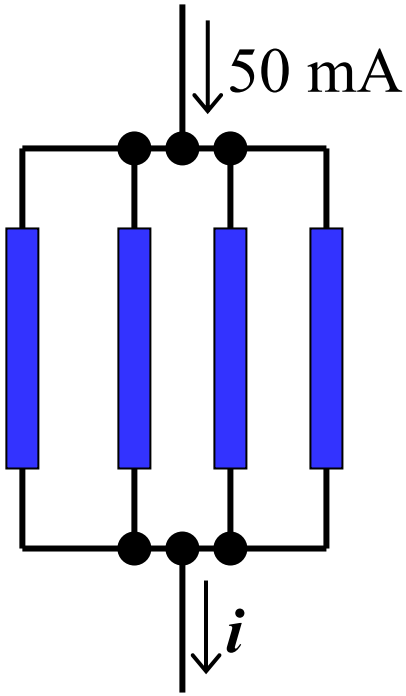
- The sum of currents entering/leaving any subset of nodes is zero. The current through any circuit element that connects from one node in this subset to another node in this subset need not be considered because it both adds and subtracts automatically.

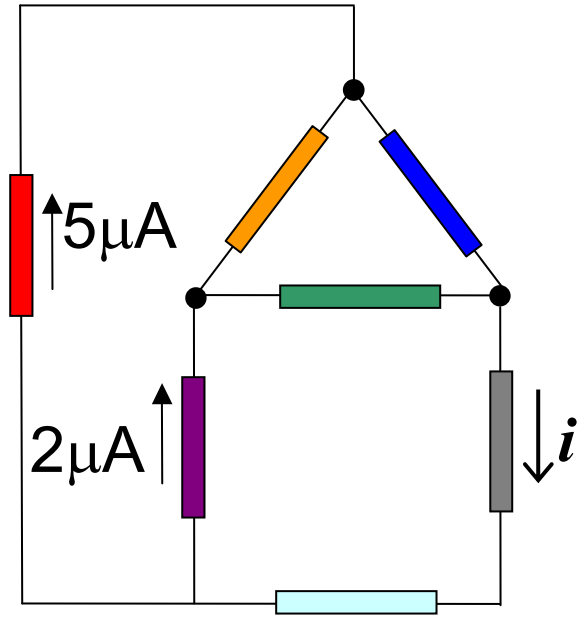
This could be a big chunk of a circuit, *i.e.* a "black box"



The links involved in writing this KCL equation go between the chosen subset of nodes and its complementary subset. Such a collection of links is called a cutset.

Generalized KCL Examples

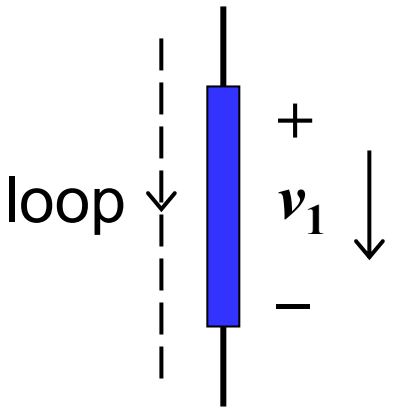




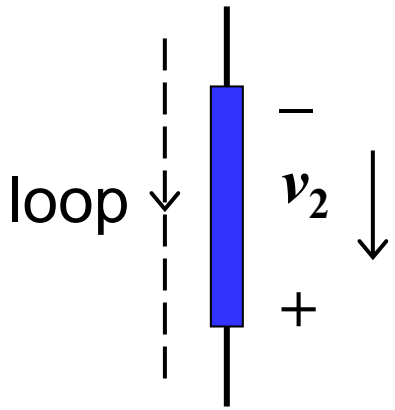
In each figure what is *i* ?

Using Kirchhoff's Voltage Law (KVL)

Consider a branch which forms part of a loop:



Moving from + to -
We add V_1



Moving from - to +
We subtract V_2

- Use **reference polarities** to determine whether a voltage is dropped
- No concern about actual voltage polarities

Formulations of Kirchhoff's Voltage Law

(Conservation of energy)

Formulation 1:

Sum of voltage drops around loop
= sum of voltage rises around loop

Formulation 2:

Algebraic sum of voltage drops around loop = 0

- Voltage rises are included with a minus sign.

(Handy trick: Look at the first sign you encounter on each element when tracing the loop.)

Formulation 3:

Algebraic sum of voltage rises around loop = 0

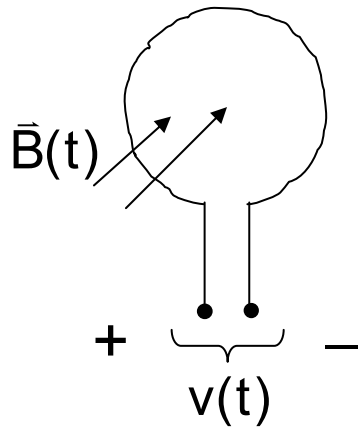
- Voltage drops are included with a minus sign.

An Underlying Assumption of KVL

- No time-varying magnetic flux through the loop

  Otherwise, there would be an induced voltage (Faraday's Law)

- Note: Antennas are designed to "pick up" electromagnetic waves; "regular circuits" often do so undesirably.



Avoid these loops!

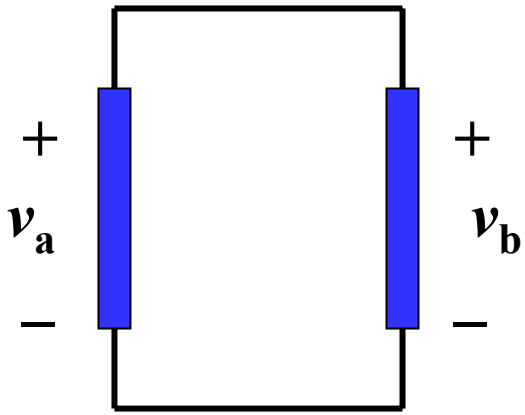
How do we deal with antennas (EECS 117A)?

Include a voltage source as the circuit representation of the induced voltage or "noise".

(Use a lumped model rather than a distributed (wave) model.)

A Major Implication of KVL

- KVL tells us that **any set of elements which are connected at both ends carry the same voltage**.
- We say these elements are connected **in parallel**.



Applying KVL in the clockwise direction, starting at the top:

$$v_b - v_a = 0 \quad \rightarrow \quad v_b = v_a$$