A) common gate configuration.

Consider the following connection:

\[ V_{DD} \]
\[ R_D \]
\[ - \]
\[ N_i \]
\[ V_i \]
\[ N_o \]

\[ \]

A.1) Considering \( V_T = 2.8 \text{V} \), \( K = 0.82 \)

\( (\text{where} \quad I_{D_{\text{sat}}} = \frac{K}{2} (V_{GS} - V_T)) \), \( V_{DD} = 9 \text{V} \)

find a combination of \( V_i, R_D \)

such that the transistor is

in saturation region

A.2) Using the small signal model

for the transistor final: \( A_V = \frac{V_o}{V_i} \), \( R_i \) the input resistance and \( R_o \) the output resistance.
A.3) Based on the values that you found in A.1, what should be the input range in order for the analysis in A.2 to make sense?

A.4) Based on the values found in A.1 what is the maximum output range? (by output range I mean \( V_{\text{max}} - V_{\text{min}} \))

What is the maximum input range?

A.5) Extra question) How would you set \( R_0 \) and \( V_1 \) in order to maximize the output range while having \( A_0 = 10 \)?
(c) Cascade configuration

\[ \begin{align*}
{\text{C.1) Assuming } V_{as1}, V_{as2}, R \text{ and } V_{dd} \text{ such that the two transistors are in saturation find:} } \\
\text{I) } A_n &= \frac{N_o}{N_i} \\
\text{II) } R_i \\
\text{III) } R_o
\end{align*} \]

(C.2 Extra) Can you find \( V_{as1}, V_{as2}, R \) such that both \( M_1 \) and \( M_2 \) are in saturation?

(Case \( V_i = 2.9 \), \( K = 0.82 \), \( V_{dd} = 12V \))
B.1) Consider the circuit

$S_1$ is a switch that closes at $t=0$, so basically $V_i$ is a step function with amplitude equal to $V_{dd}$.

I) Describe, qualitatively, how the circuit works. (What happens for $t>0$).

II) Write equations for $V_o$. Since the transistor will be in different regions (cutoff, saturation, triode) you are supposed to write three expressions for $V_o$.

III) Compute $t_1$ and $t_2$ where $t_1$ is the time when the transistor enters the saturation region and $t_2$ when it enters the triode region.
B.2) Consider now this circuit:

As in problem B.1, \( S_1 \) switches on for \( t = 0 \).

I) Describe qualitatively what happens for \( t > 0 \).

II) Write expressions for \( V_o \).

III) Compute \( t_1 \) and \( t_2 \), whose meaning is the same as B.1. III.

[For both circuits: there are no numbers, so I'm not expecting answers in terms of numbers. It is very important that you try to comment on the results that you find.]