2. Let $V_{GSP}$ be the gate-source voltage over the PMOS transistor. Then $V_{GSP} = V_{in} - V_{out}$. In the case where $V_{in} = V_{DD}$, $V_{GSP} = V_{DD} - V_{out} > 0 > V_{th}$ so the PMOS transistor is in cutoff and the output voltage is $V_{out} = V_{DD} - V_{T}$. Similarly, when $V_{in} = 0$, the output voltage is $V_{out} = V_{t}$, so the function of a circuit is a buffer. The proper way to design this is to cascade two CMOS inverters since $\sim (\sim A) \equiv A$.

3. $D = \frac{\ln(Y)}{A} = -\frac{\ln(0.93)}{22 \text{ mm}^2} = 0.003298$ defects per square millimeter at the current technology node. If we assume that $D$ stays relatively constant we get that the area of the die at 98% yield is $A = -\frac{\ln(Y)}{D} \approx 6.125 \text{ mm}^2$. To project the number of years that this growth will take, Moore’s law tells us that the number of transistors fabricated on a fixed area doubles every 2 years, which gives us roughly a factor of 4 years.