Take Home Half of Mini-Midterm 3 (80 pts)
Due at the beginning of class Wednesday (August 11th 2010)

ALL WORK SHOULD BE DONE INDIVIDUALLY
You should spend a maximum of 5 hours on this take home midterm
See lecture slides and emails for a list of allowed resources
Extra sections of the book (the WWW parts) are here:

For all problems, you have access to the following parts:

1. Resistor with resistance $R$ between 1Ω and $10^7$Ω
2. Capacitor with capacitance between 1nF and 1mF
3. Inductors with inductance between 1μH and 1H
4. PMOS and NMOS MOSFET
   a. $R_{on}$ between 10Ω and 10,000Ω
   b. $V_t$ between $-5V$ and $5V$
   c. $C_{gs} = 10^{-12}F$
   d. Obey SRC model perfectly
5. Ideal op-Amp with infinite input resistance and zero output resistance
   a. Don’t forget that op-amps are FOUR port devices. Don’t forget to include your two supplies on your diagrams
6. Any supply voltage between -110 and 110V with any frequency between 0 and 10MHz
7. Diode that perfectly obeys the voltage source model with $V_c$ between 0.3V and 2.2V. Diodes may not consume more than 1 watt
8. Physical switch (can be opened or closed)
9. Diode that perfectly obeys Shockley equation with $I_o$ between $10^{-12}$ and $10^{-16}$ and $n$ between 1 and 2 of your choice (assume $V_T = 0.026V$). May not consume more than 1 watt. I didn’t use any of these in my solutions.
10. Photodiode with perfectly obeys Shockley equation with $I_{optical}$ of up to 5mA (your choice). I also didn’t use any of these.

Current sources and ideal dependent sources are not allowed!

If anything is unclear, email or text me. If there’s no time to receive an answer from me, or you don’t hear from me for some reason, then write down your assumptions and solve.
1. [34 pts] Filter Design [this one is arguably the most time consuming]:

In this problem, you will design a 4 terminal device with two input terminals which accepts a sinusoidal input voltage $V_{in}(t) = A \cos(\omega t + \theta)$ and outputs a new sinusoidal output voltage $V_{out}(t)$.

For this problem:

1. Neatly draw your circuit, listing all parts and values.
2. [3 pts] Find $H(j\omega)$ for your system.
3. Plot the magnitude and phase Bode plots
   a. [5 pts] Your magnitude plot should be on a dB scale
   b. [1 pt] Your phase plot should be on a semilog scale
4. Calculate $|H(j\omega)|$ for $\omega = 500, 5000, 7500, 10000, \text{ and } 100,000$. Your answers should be:
   a. [2 pts] $|H(j500)| \leq 0.1$
   b. [2 pts] $|H(j5000)| \geq 0.70$
   c. [2 pts] $0.9 \leq |H(j7500)| \leq 1.1$
   d. [2 pts] $|H(j10,000)| \geq 0.70$
   e. [2 pts] $|H(j100,000)| \leq 0.1$
5. [2 pts] If your transfer function changes if you add a 5Ω load, then calculate $|H(j\omega)|$ for $\omega = 500, 5000, 7500, 10000, \text{ and } 100,000$ for a 5Ω load. If it doesn’t change with a load, free 2 pts

1. The device must be able to correctly handle any input voltage between $-5V$ and $5V$
2. The input source must not provide more than 1W of real power on average.
3. $|H(j7500)|$ should be between 0.9 and 1.1
4. All frequencies between $\omega = 5000 \text{ rad/sec}$ and $\omega = 10000 \text{ rad/sec}$ should be attenuated (reduced in magnitude) by less than 30%
5. All frequencies less than $\omega = 500 \text{ rad/sec}$ should be attenuated by at least 90% (i.e. magnitude should be at most $1/10^{th}$)
6. All frequencies greater than $\omega = 100,000 \text{ rad/sec}$ should be attenuated by at least 90%
7. The device should meet the above specifications for any resistive load greater than 5Ω.
6. **[2 pts]** Explain briefly how you came up with your circuit and list any references which played a significant part in your design. If it is just “I got a template from the book”, that is ok

The remaining 12 points will be based on correctness. If you meet all the given test cases above, you will probably get these 12 points.

Hint: For problem 1, my drawing of my circuit used one resistor, one capacitor, one inductor, two op-amps as voltage buffers and an AC source which represented the input.
2. [0 pts] Tone Generator Design – There is no tone generator design problem.

3. [25 pts] Adder Design

In this problem, you will design a digital 2-bit adder. It takes as inputs \(a_1, a_2, b_1,\) and \(b_2.\) It outputs \(c_1, c_2,\) and \(c_3.\) The voltages will be 5V for 1, and 0V for 0.

The idea here is that \(a_1\) and \(a_2\) together represent an integer which we’ll call \(A.\) The mapping is as follows:

<table>
<thead>
<tr>
<th>(a_1)</th>
<th>(a_2)</th>
<th>Integer represented: (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

The same mapping holds true for \(b_1, b_2,\) giving integer \(B.\)

Similarly, \(C\) will be an integer represented by 3 binary values \(c_1, c_2, c_3,\) giving the table below:

<table>
<thead>
<tr>
<th>(c_1)</th>
<th>(c_2)</th>
<th>(c_3)</th>
<th>Integer represented: (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
</tbody>
</table>

Our goal is to build part of a CMOS circuit which implements a 2-bit adder.

For example, If we give our device an input of \(a_1 = 5V, a_2 = 0V\) and \(b_1 = 0V, b_2 = 5V,\) this means we’re telling our device we want to know the sum of \(A\) (which is 2), and \(B\) (which is 1). Thus, the output should give us \(C=3,\) or equivalently \(c_1 = 0V, c_2 = 5V, c_3=5V.\) This sort of thing is exactly what your computer is doing all the time, and you can learn all about this in CS61C or CS150.
Fully developing the logic functions which give the correct \( c_1, c_2, \) and \( c_3 \) is beyond the scope of this course, so we’ll focus instead on the hardware design for this circuit. In this problem, all gates have capacitances are \( 10^{-12} \) F.

1. **[1 pt]** Using the tables above, explain why \( c_3 = a_2 \overline{b_2} + \overline{a_2} b_2 \). Include a 4 row truth table giving \( c_3 \) as a function of \( a_2 \) and \( b_2 \) as part of your answer.

2. **[3 pts for network, 1.5 points for each \( V_{\ell} \)]** If you use the equation as it is written in part 1, you will need 14 transistors, which is suboptimal. It is possible to show that
   \[
   c_3 = (\overline{a_2} + b_2)(a_2 + \overline{b_2})
   \]
   In other words, this is another way of writing the equation from part 1, it takes less hardware to implement if you use the design procedure from class. Neatly draw a static CMOS network which implements this function. This should take 12 total transistors (4 of which will be used for inverting \( a_2 \) and \( b_2 \)). Select \( V_{\ell} \) for the NMOS and PMOS transistors such that the circuit considers any value below 1V as 0 and any value above 3.5V as 1. Do not pick \( R_{on} \) yet.

3. **[0 pts]** We can also find \( c_2 = (a_1 + b_1 + k_2)(a_1 + \overline{b_1} + k_2)(\overline{a_1} + b_1 + k_2)(\overline{a_1} + \overline{b_1} + k_2) \), where \( k_2 = a_2 b_2 \). Finding this efficiently is beyond the scope of the course. Finding this efficiently is beyond the scope of the course. In an older version of this exam, where I didn’t make a dumb algebra mistake, there were a reasonable number of transistors here, and it wasn’t so bad. Don’t implement this unless you are really bored with life itself.

4. **[0 pts]** Lastly it can be shown that \( c_1 = (\overline{a_1} + b_1)(\overline{a_1} + \overline{k_1})(\overline{b_1} + k_1) \), where \( k_1 = a_1 b_1 + a_1 k_2 + b_1 k_2 \). Again, a major pain to implement.

5. **[3 pts]** Imagine that all inputs have been low for a long time. Then suddenly \( a_1 \) and \( b_1 \) instantly increase to 5V, while \( a_2 \) and \( b_1 \) remain 0V [for CS61C folks, this represents, for example, the output of a decoder stage right after a clock cycle of our instruction which wants to add two immediate values, namely 2 and 1].

Thus, \( A \) now represents the number 2 and \( B \) represents the number 1. In response, your design from part 2 should give the least significant digit of \( C=3 \), or in other words, \( c_3 \) should be 1, since \( c_1 = 0, c_2 = 1, c_3 = 1 \).

Verify that if \( a_1 = 5V, a_2 = 0V, b_1 = 0V, \) and \( b_2 = 5V, \) your circuit gives that \( c_3 = 5V \).

6. **[4 pts]** Let \( V_{\overline{a_2}}(t) \) be the output of the inverter which inverts \( a_2 \). What is \( V_{\overline{a_2}}(t) \) in terms of \( R_{on} \)?

   Give the rising AND falling case, assuming the voltage starts at the opposite end (so if falling, it starts at 5V, and if rising, it starts at 0V). Keep in mind that this inverter drives multiple gate capacitances (in my implementation, it drove two gate capacitances), so \( C \) will not be simply \( 10^{-12} F \). Note that \( \overline{a_2} \) is not used by the equations which calculate \( c_2, k_2, c_1, \) or \( k_1, \) so all gate capacitance will appear entirely in the part of the design you drew for part 2.

7. **[5 pts]** Using your answer from part 6, select an \( R_{on} \) (same for NMOS and PMOS) such that the inverter takes:
   a. At most 1\( \mu s \) to rise from 0V to 3.5V AND
   b. At most 1\( \mu s \) to fall from 5V to 1V
8. [1 pts] Let $V_{b_2}(t)$ be the output of the inverter which inverts $b_2$. If we use the same $R_{on}$ values from part 7, what is $V_{b_2}(t)$? Give the rising AND falling case, assuming the voltage starts at the opposite end (so if falling, it starts at 5V, and if rising, it starts at 0V) Keep in mind that this inverter drives multiple gate capacitances, and does not appear in the equations $c_2$, $k_2$, $c_1$, or $k_1$, so all capacitance is entirely in the part of the design you drew for part 2.

9. [4 pts] Now let’s see how the circuit reacts to the input combination from part 5. Assume that $V_C$ is driving a 1pF $(10^{-12} F)$ load. Let $V_{c_3}(t)$ be the output of the gate you built for part 2. Find $V_{c_3}(t)$ (you will need your answers to part 6 and 7 and 8).

10. [1 pt] How much time does it take for $c_3$ to reach 3V?

11. [0 pt] This was a power problem but it is beyond rescuing. Suffice it to say the calculation of $C=1+2$ is roughly $10^{-10} J$.

12. [Bonus 0.1 pt] Humans use about 100W (based on 2000 food calories per day), and can calculate $1+2$ on the order of something like 10 ms. How much energy does a human use when computing $1+2$? (Note: humans are simultaneously doing many many other things, so the comparison is unfair, and my estimate of the calculation time is obviously a very rough estimate. For large numbers the comparison is much better, since we can actually clock the time it takes you to add those numbers).

4. [21 pts] Voltage Regulator

For this problem, you’ll make a device which takes a voltage input $V_{in}$. If $1.1 V < V_{in} < 5 V$, then $V_{out}$ will be 1V. If $V_{in} < 1 V$, your device has no defined behavior.

In this problem you CAN NOT USE voltage supplies other than the given $V_{in}$. In other words your device must be completely passive (cannot provide power)!

Detailed specifications are as follows:

1. If $1.1 V \leq V_{in} \leq 5 V$, then $V_{out} = 1 V$ within 10%
2. If $0 V \leq V_{in} \leq 1.1 V$, $V_{out}$ may be any voltage
3. Your circuit should work correctly for any load $R_L$ greater than 100Ω
Hint: If your design utilizes a diode, make sure you didn’t violate the power constraints of the diode. No diodes don’t count as voltage supplies, because they cannot supply power (because current always flows into their plus end).

1. Neatly draw your circuit, listing all parts and values.
2. [2 pts] Calculate $V_{out}$ when $V_{in} = 1.1V$ and $R_L = 100\Omega$, output should be within 10% of 1
3. [2 pts] Calculate $V_{out}$ when $V_{in} = 5V$ and $R_L = 100\Omega$, output should be within 10% of 1
4. [2 pts] Calculate $V_{out}$ when $V_{in} = 1.1V$ and $R_L = 10^7\Omega$, output should be within 10% of 1
5. [2 pts] Calculate $V_{out}$ when $V_{in} = 5V$ and $R_L = 10^7\Omega$, output should be within 10% of 1
6. [2 pts] Calculate $V_{out}$ when $V_{in} = 0.5V$ and $R_L = 100$, output can be anything
7. [2 pts] Explain briefly how you came up with your circuit and list any references which played a significant part in your design. If it is just “I got a template from the book”, that is ok.

The remaining 9 points will be based on correctness including power constraints on any diode or diodes that might be inside your circuit. Remember, no sources allowed inside your box.
Regulator Bonus (2 pts total) [Two level voltage regulator]: Draw a device that meets the following specification: and if $V_{in} < -1V$ and $V_{out} = -1V$, and repeat steps 1 through 6 for the previous voltage regulator.

1. If $1.1V < V_{in} < 5V$, then $V_{out} = 1V$
2. If $V_{in} < -1.1V$, then $V_{out} = -1V$
3. If $-1.1V < V_{in} < 1.1V$, $V_{out}$ may be any voltage
4. Your circuit should work correctly for any load $R_L$ greater than 100Ω
Diode Design Bonus (2 pts total):

You want a diode which has maximum reverse bias current $10^{-15} A$. Luckily, you have been given an ancient tablet which gives an approximation for the saturation current as $I_s = qA\left(\frac{n_i^2}{N_d} + \frac{n_i^2}{N_a}\right)$, where:

1. $q$ is the charge of an electron $1.6022 \times 10^{-19} C$
2. $A$ is the cross sectional area of the p-n junction in $cm^2$
3. $n_i^2$ is the square of the intrinsic carrier concentration. $n_i^2 = 10^{20}$ carriers/cm$^3$
4. $N_d$ is the concentration of acceptor atoms on the p side (in atoms/cm$^3$)
5. $N_a$ is the concentration of donor atoms on the n side (in atoms/cm$^3$)
6. $p=2000$ is a proportionality constant (in $cm^2/s$)
7. 4.4 is a dimensionless constant representing the fact that electrons have an easier time moving around inside the material compared to holes*.

In this problem, we will design a diode so that the theoretical current of the diode reaches 1A when the diode is forward biased with a voltage of 1V.

1. (0.5 pts) Assuming $n = 1$, calculate $I_s$ such that current is 1A when $V_p$ is 0.7V. Assume $V_T = 0.026V$
2. (0.5 pts) Assuming we have a cross sectional area of $A = 0.01 cm^2 \ (1mm \times 1mm)$, select $N_d$ and $N_a$ meeting the specifications below:
   a. $I_s \approx$ your answer from part 1
   b. $N_d < 10^{16}$ atoms/cm$^3$
   c. $N_a < 10^{16}$ atoms/cm$^3$
3. (0.5 pts) What element might we use for our donor dopant? For our acceptor dopant? Why do we use these dopants?
4. (0.5 pts) How does doping affect the height of the barrier separating the p and n regions? Does it increase or decrease as our dopant concentrations increase?

*: The somewhat intuitive reason for this is that holes are in the valence band and electrons are in the conduction band.