EECS 42 – Introduction to Electronics for Computer Science

Fall 2001, Dept. EECS, UC Berkeley
Prof. A. R. Neureuther 510 Cory 642-4590
Course Web Site http://www-inst.eecs.berkeley.edu/~ee42/

Midterm Wed. Nov. 7th
Last name A-K in 2040 Valley LSB, L-Z in 10 Evans
Review Session #1: 1-2 PM Sat. Nov 3rd 241 Cory
Review Session #2: 5-6 PM Tue. Nov 6th, 241 Cory

Topical Coverage Second Midterm
Schwarz and Oldham Material followed by skills

Chapter 2: all except 2.4 Loop Analysis, 2.6 and 2.7, light on 2.5
Node analysis of circuits with up to 8 branches
Voltage and current dividers

Chapter 3: all
Equivalent circuits: Thevenin and Norton
Nonlinear loads and load lines

Chapter 4: all but only ideal op-amps
Dependent sources, gain, input and output impedance
Ideal Op-Amps
Generalization to Comparators

Chapter 5: all light on 5.3 and very limited inductor circuits.

Chapter 8.1: Only 8.1
EE 40/42 simple solution method and application to switching and pulses
KCL to get differential equation for capacitor voltage and inductor current

Chapter 10: no flip-flops
Gates and logic functions
Generalization: Timing diagrams

Lectures 15-18, pp. 522-524, 604-611 Logic with state dependent devices
Device I vs. V curves and load line method
Simple inverter and voltage transfer function
Complementary Pull-Up and Pull-Down networks (CMOS)
Dynamic (Transient) Switched Resistor Model and 0.69RC delay

Likely Exam Emphasis
Analysis of vanilla circuits with dependent sources
Ideal Op-Amps
Analysis of circuits using dependent sources to improve characteristics
Logic Functions and Timing Diagrams
Static and dynamic analysis of logic gates - Using the $I$ vs. $V$ device model for static analysis and the switched resistor model for transient analysis.