a. \( F = (\overline{A} \cdot B) \)

b. Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>( \overline{A} )</th>
<th>B</th>
<th>( \overline{B} )</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
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</tbody>
</table>

c. \( C_g = \text{Cox} \times \text{gate electrode area} = \text{Cox} \cdot W \cdot L \)

\( \text{Cox} = 2.3 \, \text{fF/\( \mu \text{m}^2 \)} \)

Use \( W \)s and \( L \)s as on diagram in notes of 29.04.02 (see second page), i.e.,

- PMOS: 12 \( \mu \text{m} \) and 1.5 \( \mu \text{m} \)
- NMOS: 6 \( \mu \text{m} \) and 10.5 \( \mu \text{m} \)

Let \( R_p = \frac{1}{\text{gm}} \), \( R_n = 4 \, k\Omega \)
Find $C_{GP} = 23\,\text{fF} \times 12 \times 1.5 = 41.4\,\text{fF}$

$C_{GN} = 2.3\,\text{fF} \times 6 \times 1.5 = 20.7\,\text{fF}$

2. What is fanout of the inverter (1)?
3. What gate capacitance does the inverter drive?

$C_{GP} + C_{GN} = 41.4 + 20.7 = 62.1\,\text{fF}$

f. In NAND gate what is the source resistance when $F$ goes from 1 to 0?

$R = 2R_N = 8\,\text{k}\Omega$

g. In NAND gate what is the resistance when $F$ goes from 0 to 1?

Max of only one PMOS is shunt changes state $\rightarrow 4\,\text{k}\Omega$

h. In terms of $R_P$ and $R_N$, and what is the time delay in the inverter?

$T_{iu} = R (C_{GP} + C_{GN}) = 4\,\text{k}\Omega \times (62.1\,\text{fF}) = 248\,\text{ps}$

Gate delay $= 0.69R = 17\,\text{ps}$

i. If the load capacitance $C_L = 100\,\text{fF}$, what is the maximum delay in the NAND gate?

$T_{max} = R_{max} \times C_L = 8\,\text{k}\Omega \times 100\,\text{fF} = 800\,\text{ps}$

j. What values on $R_0 = 800\,\text{ps} \rightarrow T_{iu} = \frac{552\,\text{ps}}{T_{iu}}$
L. If A goes from a 0 to a 1, much energy is stored in the gate capacitance of the inverter. Which one (PMOS or NMOS)?

How much energy (assuming V<sub>DD</sub> = 5V)

\[ U = \frac{1}{2} CV^2 = \frac{1}{2} (20.7 \text{fF} \times 25) \]

\[ = 2.6 \times 10^{-13} \text{ J} \]

M. If charge occurs once each clock cycle in a 500 MHz processor, how much power is expended?

\[ P = U \times f = 2.6 \times 10^{-13} \times 5 \times 10^8 \]

\[ = 129 \mu \text{W} \]

N. If there are 60 watts:

\[ 60 \text{ watts} \rightarrow \frac{60}{129 \times 10} = 464,000 \text{ gates} \]