Lecture 11: October 8, 2001

Physical Limitations of Logic Circuits
A) Synthesis Recap
B) General Limitations for Digital
C) Gate Delay Causes and Model
D) Timing Example: XOR for EE 43
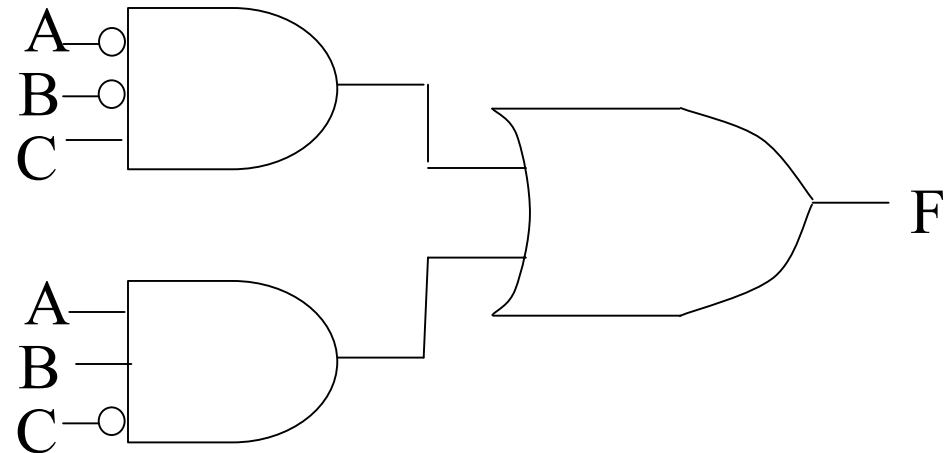### E) Timing Example: Logic Function

The following slides were derived from those prepared by Professor Oldham For EE 40 in Fall 01

Reading:
Schwarz and Oldham 11.3-11.4 pp. 403-422

How to Combine Gate to Produce a Desired Logic Function?
(More basic Logical Synthesis)

Example:

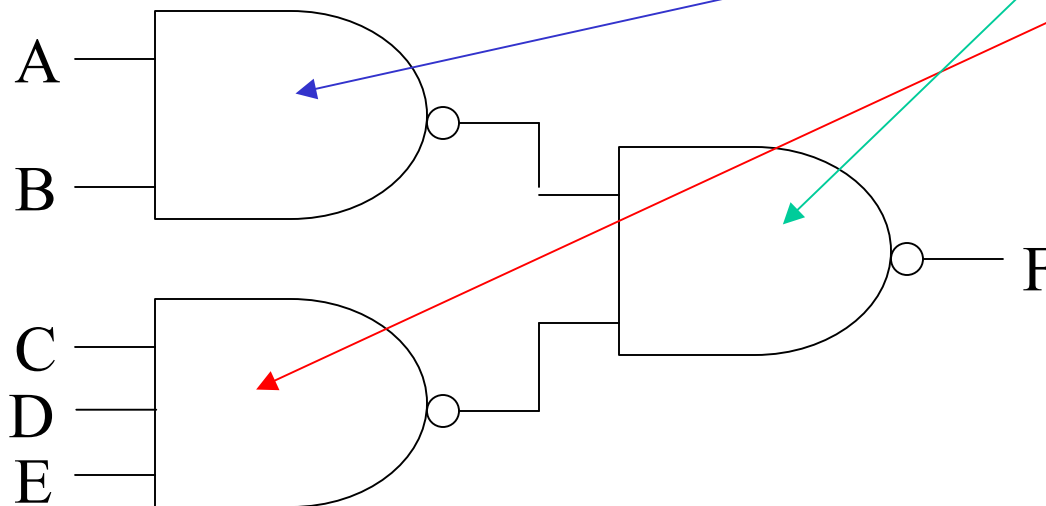| A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$$F=\overline{A}\,\overline{B}C +AB\overline{C}$$

Logical Synthesis
Guided by DeMorgan's Theorem

DeMorgan's Theorem :

$$A + B + C = \overline{\left[\overline{A}\ \overline{B}\ \overline{C}\right]} \quad \text{or} \quad \overline{A} + \overline{B} + \overline{C} = \overline{\left[A\ B\ C\right]}$$

Example of Using DeMorgan's Theorem:

$$F = A \bullet B + C \bullet D \bullet E = \overline{\overline{AB} \bullet \overline{CDE}}$$

Thus any sum of products expression can be immediately synthesized from NAND gates alone

What Are Some Limitations of Digital?

It takes a lot of bits to represent even simple audio signals and if we convert a real-time audio signal to digital, we need to transmit a lot of bits every second.
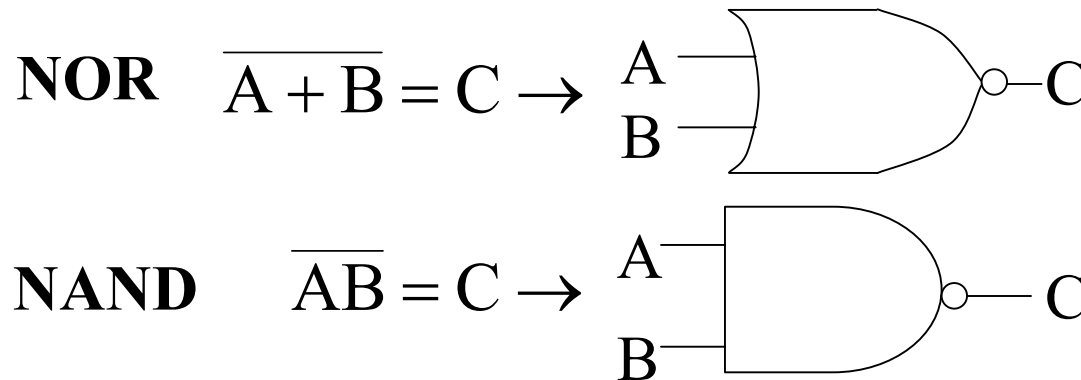
Example: An ordinary audio signal is sampled every 50µs (to achieve 10KHz frequency performance) and evaluated (converted to digital form) to an accuracy of 1 part in 10,000. Every sample requires how many bits?

2^{13} = 8,192 and 2^{14} = 16,384   so we need 14 bits for each sample. Now we need to transmit these bits 20,000 times per second. The bit rate is 280,000 baud!}

The transmission of digital signals as pulses through circuits and over transmission media leads to pulse degradation, just as analog signals are degraded. As a consequence, we must (a) detect and regenerate the signal before it gets "buried in the noise," and (b) accept that propagation delays are intrinsic to signal flow, and take these delays into account in our design (e.g., to avoid making a control decision based on a piece of information that has not yet arrived!). The RC transient lectures treated pulse degradation in real circuits quantitatively.

PHYSICAL LIMITATIONS OF LOGIC GATES

- Computer Datapath: Boolean algebraic functions using binary variables
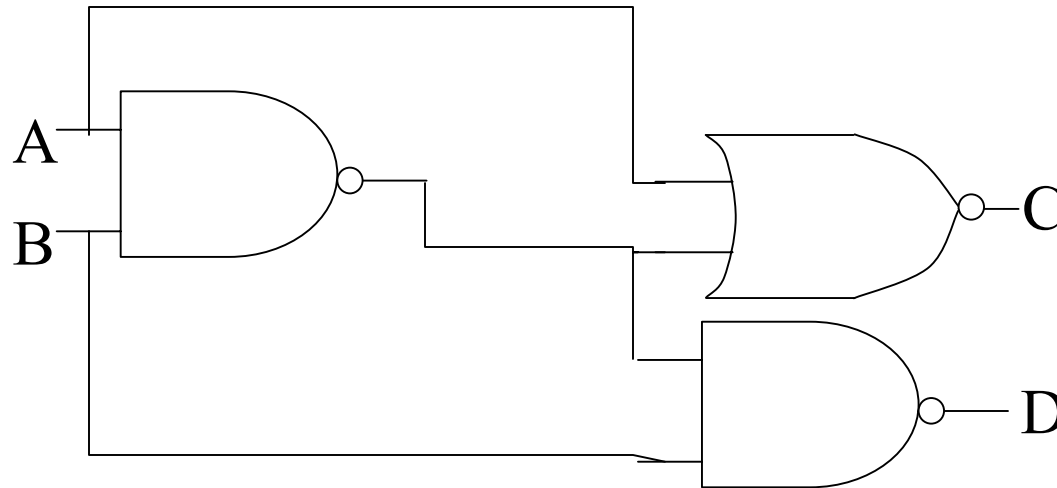
- Symbolic representation of functions using logic gates

NOR $\overline{A + B} = C \rightarrow$ A ─┐
                                            B ─┘ ─○─ C

NAND $\overline{AB} = C \rightarrow$ A ─┐
                                            B ─┘ ─○─ C

However:

- Every node has capacitance and interconnects have resistance. It takes time to charge these capacitances.

    Thus, output of all circuits, including logic gates is **delayed** from input.

PHYSICAL LIMITATIONS OF LOGIC GATES

Computer Datapath: Connected logic gates

Every node in any circuit (such as the internal circuit of a NAND gate) has capacitance and all interconnects have resistance. Thus it takes time to charge these capacitances.
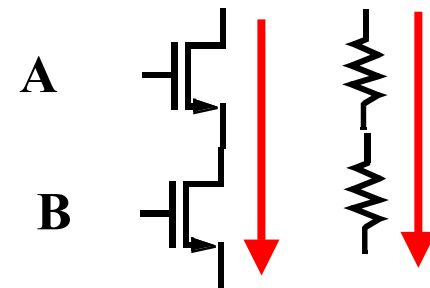
Thus, output of all circuits, including logic gates is **delayed** from input.

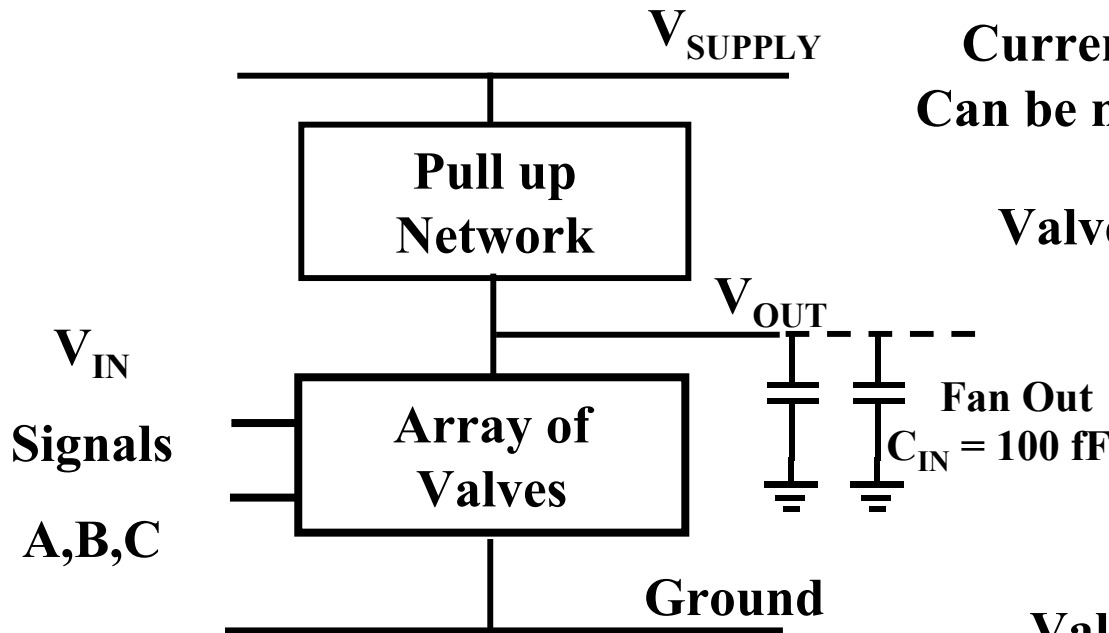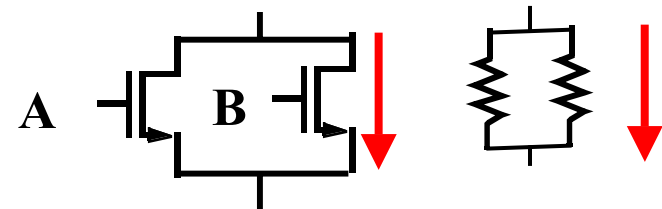# Logic Gates – How are they built in practice?

A Valve is a Transistor V_{IN}

Current flows when V_{IN} is high
Can be modeled by a 10kΩ resistor

Valves in Series => NAND

V_{SUPPLY}

Pull up Network

V_{OUT}

V_{IN}

Signals

Array of Valves

A,B,C

Fan Out
$C_{IN} = 100$ fF

Ground

A

B

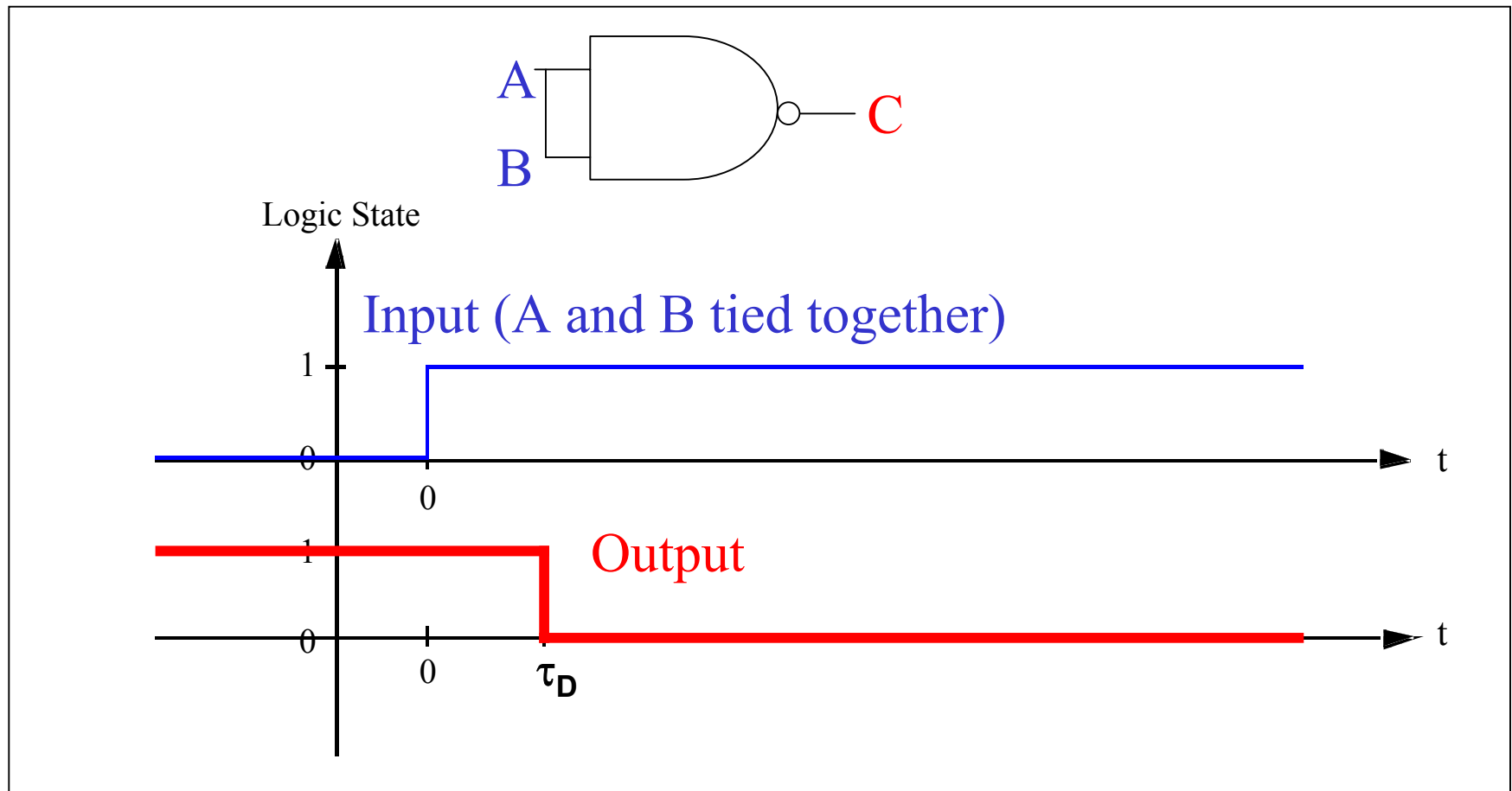**Valves in Parallel => NOR**

(You can learn about building gates in EE 141.)

A   B

UNIT GATE DELAY τ_D

Time delay τ_D occurs between input and output: "computation" is not instantaneous

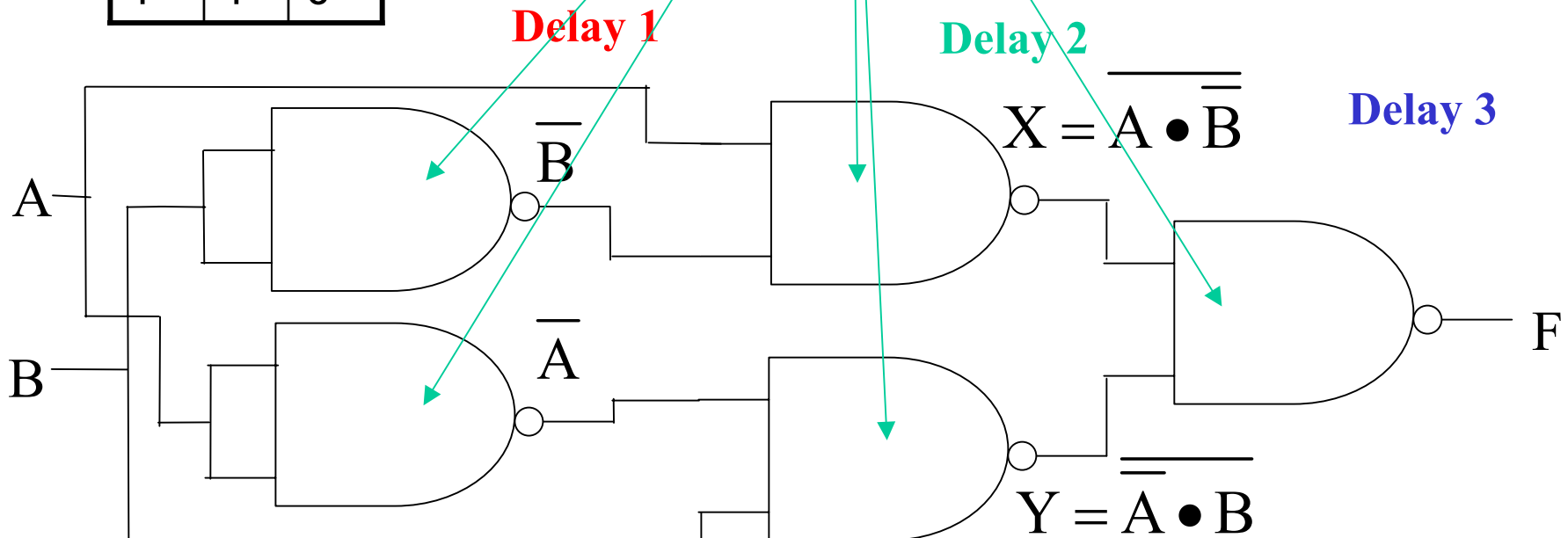Value of input at $t = 0^+$ determines value of output at later time $t = \tau_D$

Logical Synthesis of XOR

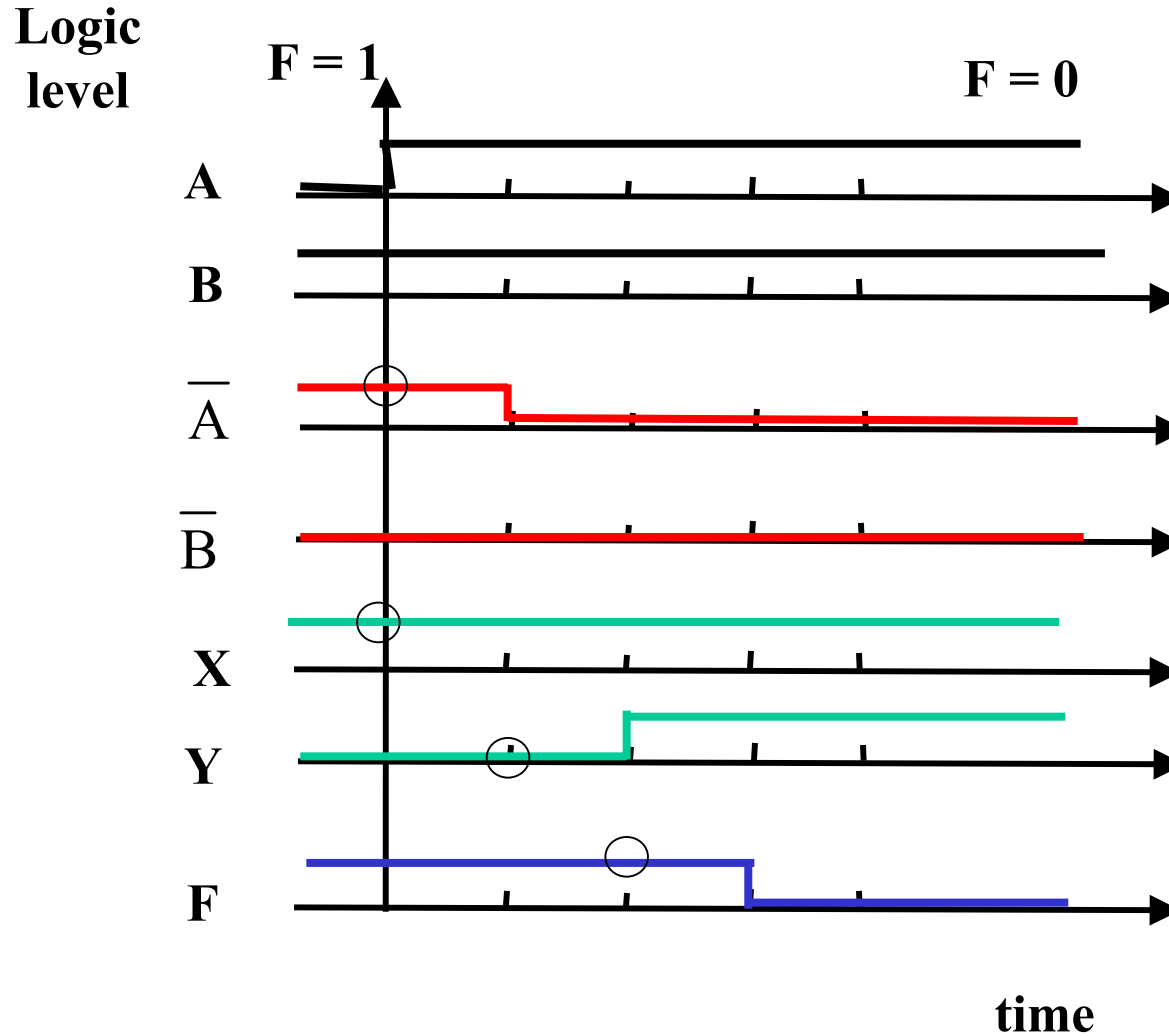| A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Inputs have different delays, but we ascribe a single worst-case delay τ to every gate

$$F = A \bullet \overline{B} + \overline{A} \bullet B$$

We Need a Timing Diagram!

Delay 1

Delay 2

Delay 3

$$X = \overline{\overline{A} \bullet \overline{\overline{B}}}$$

$$Y = \overline{\overline{\overline{A} \bullet B}}$$

$\overline{B}$

$\overline{A}$

A

B

F

Timing Diagram for Delays in Logic

Logic level

F = 1   F = 0

A

B

$\overline{A}$

$\overline{B}$

X

Y

F
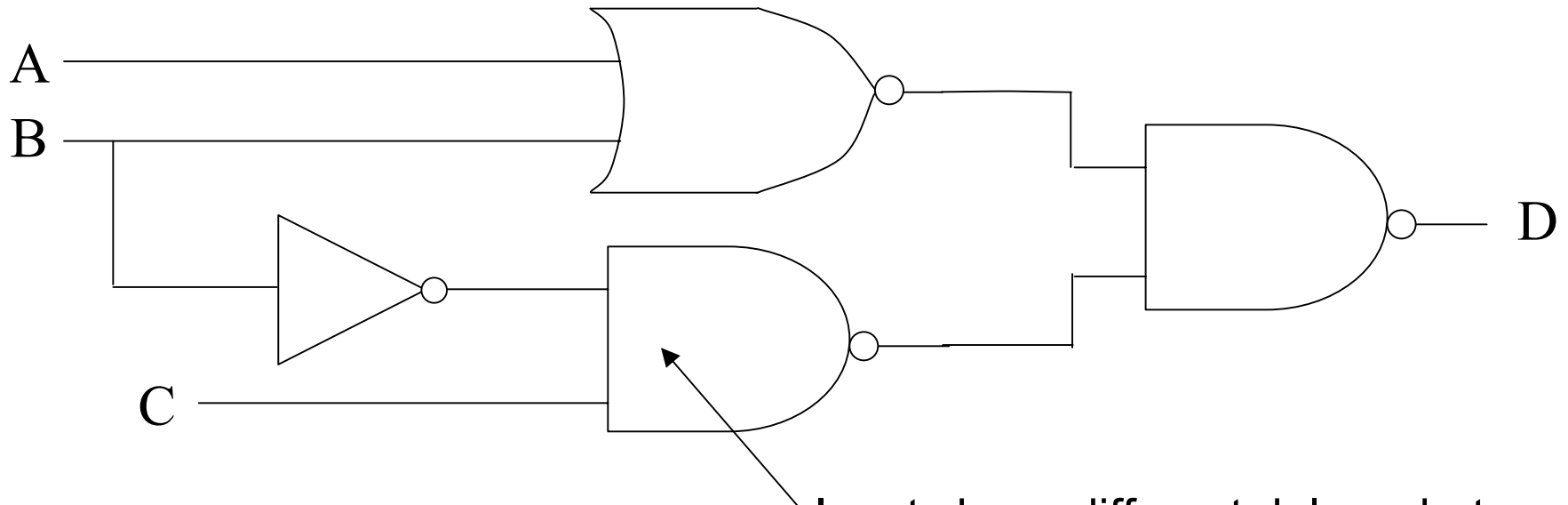
time

EFFECT OF GATE DELAY

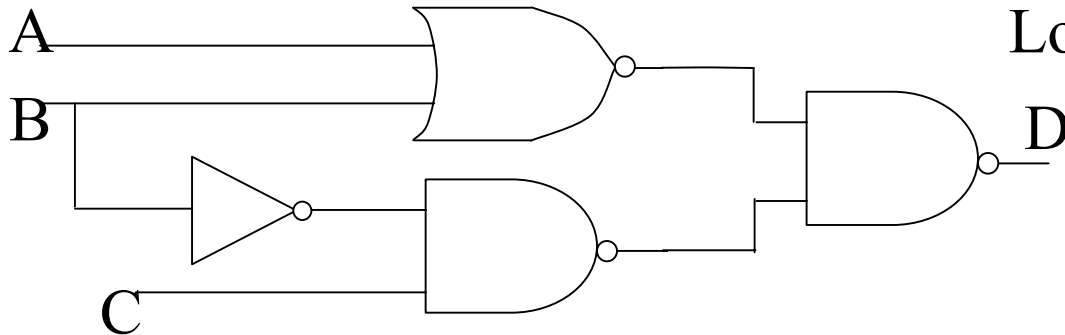Cascade of Logic Gates

Inputs have different delays, but we ascribe a single worst-case delay τ to every gate
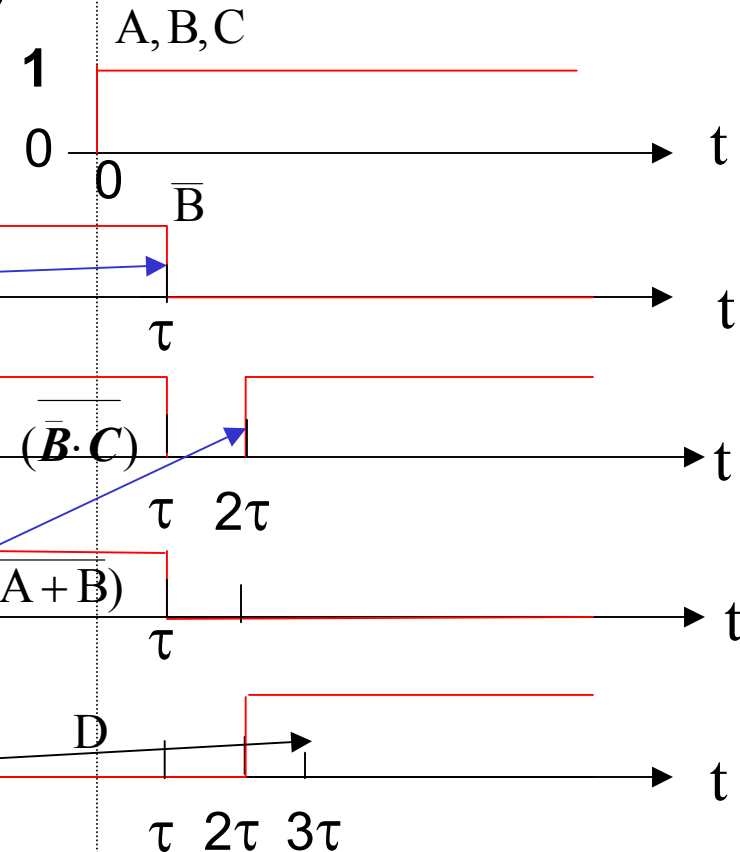
How many "gate delays for shortest path?   ANSWER : 2

How many gate delays for longest path?   ANSWER : 3

TIMING DIAGRAMS

Show transitions of variables vs time

Note $\overline{B}$ becomes valid one gate delay after B switches

Note that $(\overline{B} \cdot C)$ becomes valid two gate delays after B&C switch, because the invert function takes one delay and the NAND function a second.

No change at t = 3τ

Logic state

A, B, C

$\overline{B}$

$\overline{(\overline{B} \cdot C)}$

$(\overline{A + B})$

D