Static and Transient Analysis of Gates

A) Detailed Recap of Static Gate Analysis
   Transistor CMOS Inverter Example
   Terminology, \( I_{\text{OUT-SAT-D}} \), VTC, \( V_M \)

B) Break to Discuss Quiz and Midterm

C) Transient Gate Analysis

D) Switch Resistor (\( R_{\text{EQ}} \)) Approx. Model

E) Logic Block and 0.69\( R_{\text{EQ}} \)C Worst Case Inputs

Reading: 523-525, 604-611, (only the loadline methods) and lecture handouts
Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.
Case #1: $V_{IN} = V_{DD} = 5V$

The Output is Pulled-Down

- The PMOS transistor is OFF when $V_{IN} > V_{DD} - V_{TU}$
- The NMOS transistor is ON when $V_{IN} > V_{TD}$
Case #2: $V_{IN} = 0$
The Output is Pulled-Up

The PMOS transistor is ON when $V_{IN} < V_{DD} - V_{TU}$

The NMOS transistor is OFF when $V_{IN} < V_{TD}$
Terminology

\[ V_{DD} = \text{Power supply voltage (D is from Drain)} \]

**Pull-Down Network** = Set of devices used to carry current from the output node to ground to discharge the output node to ground.

\[ \text{Pull-Up Network} = \text{Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.} \]

\[ I_{OUT} = \text{Current for the device under study.} \]

\[ V_{TD} = \text{Threshold Voltage value of } V_{IN} \text{ at which the Pull-Down (NMOS transistor) begins to conduct.} \]

\[ V_{OUT-SAT-D} = \text{Value of } V_{OUT} \text{ beyond which the current } I_{OUT-D} \text{ saturates at the (drain) current saturation value } I_{OUT-SAT-D}. \]
States are Voltage Levels of $V_{IN}$

- **State 1 or** $V_{IN} = 1V$
- **State 3 or** $V_{IN} = 3V$
- **State 5 or** $V_{IN} = 5V$

(Drain) current saturation values:
- $I_{OUT-SAT-D} = 100 \mu A$
- $I_{OUT-SAT-D} = 50 \mu A$
- $I_{OUT-SAT-D} = 0 \mu A$

The maximum voltage is $V_{DD}$.

Current is flat (saturated) beyond $V_{OUT-SAT-D}$.

Current is zero until $V_{IN}$ is larger than $V_{TD}$.
Saturation Current NMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is larger than the threshold value $V_{TD}$ and the current is proportional to $V_{OUT}$ up to $V_{OUT-SAT-D}$ where it reaches the saturation current:

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold ($V_{TD}$) and saturation ($V_{OUT-SAT-D}$).

Example:

- $k_D = 25 \, \mu A/V^2$
- $V_{TD} = 1V$
- $V_{OUT-SAT-D} = 1V$

Use these values in the homework.

$$I_{OUT-SAT-PD} = 25 \frac{\mu A}{V^2} (3V - 1V) |V| = 50 \mu A$$

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Saturation Current PMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is smaller than $V_{DD}$ minus the threshold value $V_{TU}$ and the current is proportional to $(V_{DD} - V_{OUT})$ up to $(V_{DD} - V_{OUT-SAT-U})$ where it reaches the saturation current

$$I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}$$

Example:

$k_U = 20 \, \mu A/V^2$

$V_{TU} = 1V$

$V_{OUT-SAT-U} = 1V$

$$I_{OUT-SAT-U} = 20 \frac{\mu A}{V^2} (5V - 3V - 1V) 1V = 20 \mu A$$

Use these values in the homework.

State 3 $V_{IN} = 3V$

Linear (with $V_{OUT}$)

Saturation (with $V_{OUT}$)
**Composite $I_{OUT}$ vs. $V_{OUT}$ for CMOS**

- **PU current is flat (saturated) below** $V_{DD} - V_{OUT-SAT-D}$
- **PD current is flat (saturated) beyond** $V_{OUT-SAT-D}$

**Solution**
- State 3 or $V_{IN} = 3V$
- $V_{OUT-SAT-D}$
- $V_{OUT} = 5$ $V_{OUT}(V)$

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Voltage Transfer Function for the Complementary Logic Circuit

State 1 for $V_{IN} = 1V$

Vertical section due to zero slope of $I_{OUT}$ vs. $V_{OUT}$ in the saturation region of both devices.

State 3 for $V_{IN} = 3V$

State 5 for $V_{IN} = 5V$
Method for Finding $V_M$

At $V_M$,

1) $V_{OUT} = V_{IN} = V_M$

2) Both devices are in saturation

3) $I_{OUT-SAT-D} = I_{OUT-SAT-U}$

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

$$= I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}$$

Substitute $V_M$

Solve for $V_M$

Example Result: When $k_D = k_P$, $V_{OUT-SAT-D} = V_{OUT-SAT-U}$ and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$
Lecture 17: October 29, 2001

Reminder: Quiz and Midterm

Quiz 20 minutes At Start of Class Wed. Oct 31
Covers Material 6th-9th week including HW#9

Midterm in Class Wed. Nov 7th
Covers Material 6th-10th week including HW#10

Closed Book, Closed Notes, Bring Calculator, Paper Provided
Last Name A-K 2040 Valley LSB; Last Name L-Z in 10 Evans

Topic Coverage Review in class Oct 31; Old Exams on Web
Review Session: Sat 1-2:30 (TBA Evans); Tu 5-6:00 (? Cory)

EE 43 Labs Are Not Cancelled:

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Transient Gate Problem: Discharging and Charging Capacitance on the Output

\[ V_{IN} = V_{DD} = 5V \]

\[ V_{OUT} \]

\[ C_{OUT} = 50 \text{ fF} \]
Output Capacitance Voltage vs. Time

When $V_{OUT} > V_{OUT-SAT-D}$ the available current is $I_{OUT-SAT-D}$

Assume that the necessary voltage swing to cause the next downstream gate to begin to switch is $V_{DD}/2$ or 2.5V. The propagation delay is thus

$$
\Delta t = \frac{C_{OUT} \Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT} V_{DD}}{2 I_{OUT-SAT-D}} = \frac{50 \text{fF} \cdot 2.5V}{100 \mu A} = 1.25 \text{ns}
$$

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Switched Equivalent Resistance Model

The above model assumes the device is an ideal constant current source.

1) This is not true below \( V_{\text{OUT-SAT-D}} \) and leads to inaccuracies.

2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting \( 0.69R_D C \) equal to the \( \Delta t \) found above

\[
\Delta t = \frac{C_{\text{OUT}} V_{\text{DD}}}{2I_{\text{OUT-SAT-D}}} = 0.69 R_D C_{\text{OUT}}
\]

This gives

\[
R_D = \frac{V_{\text{DD}}}{2 \cdot (0.69) I_{\text{OUT-SAT-D}}} \approx \frac{3}{4} \frac{V_{\text{DD}}}{I_{\text{OUT-SAT-D}}} = \frac{3}{4} \frac{5V}{100 \mu A} = 37.5k\Omega
\]

Each device can now be replaced by this equivalent resistor.
Switched Equivalent Resistance Network

Switches close when input is low.

Switches close when input is high.
Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportional to the gate width/length in the geometrical layout.

Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume $R_D = R_U = 10 \, \text{k}\Omega$
Inverter Propagation Delay

Discharge (pull-down)

\[ \Delta t = 0.69 R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps} \]

\[ V_{IN} = V_{dd} \]

\[ V_{OUT} \]

\[ C_{OUT} = 50fF \]

Discharge (pull-up)

\[ \Delta t = 0.69 R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps} \]

\[ V_{IN} = V_{dd} \]

\[ V_{OUT} \]

\[ C_{OUT} = 50fF \]
Logic Gate Propagation Delay

The initial state depends on the previous inputs.

The equivalent resistance of the pull-down or pull-up network depends on the current input state.

Example: A=0, B=0, C=0 for a long time.

The capacitor has precharged up to \( V_{DD} = 5V \).

\( C_{OUT} = 50 \text{ fF} \)
Logic Gate Propagation Delay (Cont.)

At $t=0$, B and C switch to high = $V_{DD}$ and A remains low.

$C_{OUT}$ discharges through the pull-down resistance of gates B and C in series.

$$\Delta t = 0.69(R_{DB} + R_{DC})C_{OUT} = 0.69(20k\Omega)(50fF) = 690 \text{ ps}$$

The propagation delay is **two times longer** than that for the inverter!