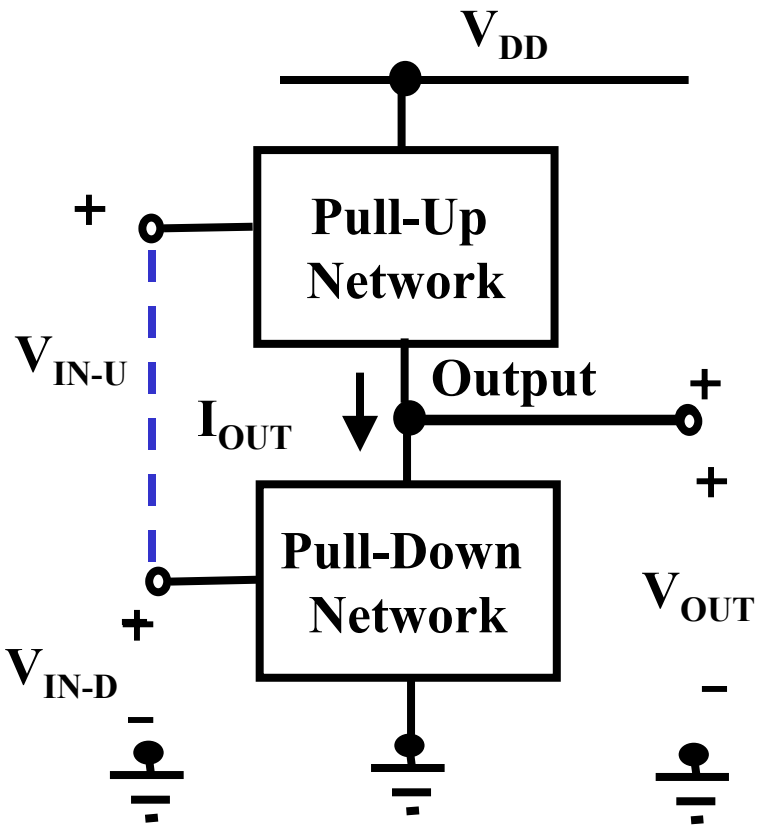
Static and Transient Analysis of Gates

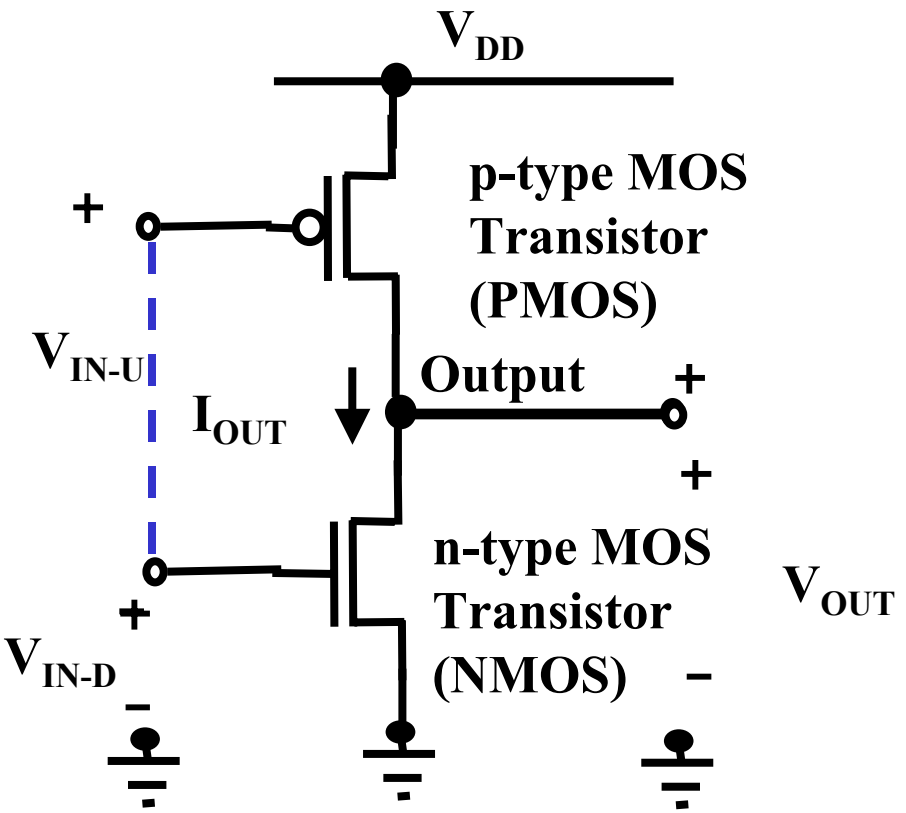
A) Detailed Recap of Static Gate Analysis
   Transistor CMOS Inverter Example
   Terminology, $I_{OUT-SAT-D}$, VTC, V_M
B) Break to Discuss Quiz and Midterm
C) Transient Gate Analysis
D) Switch Resistor (R_{EQ}) Approx. Model
E) Logic Block and $0.69R_{EQ}C$ Worst Case Inputs

Reading: 523-525, 604-611, (only the loadline methods) and lecture handouts

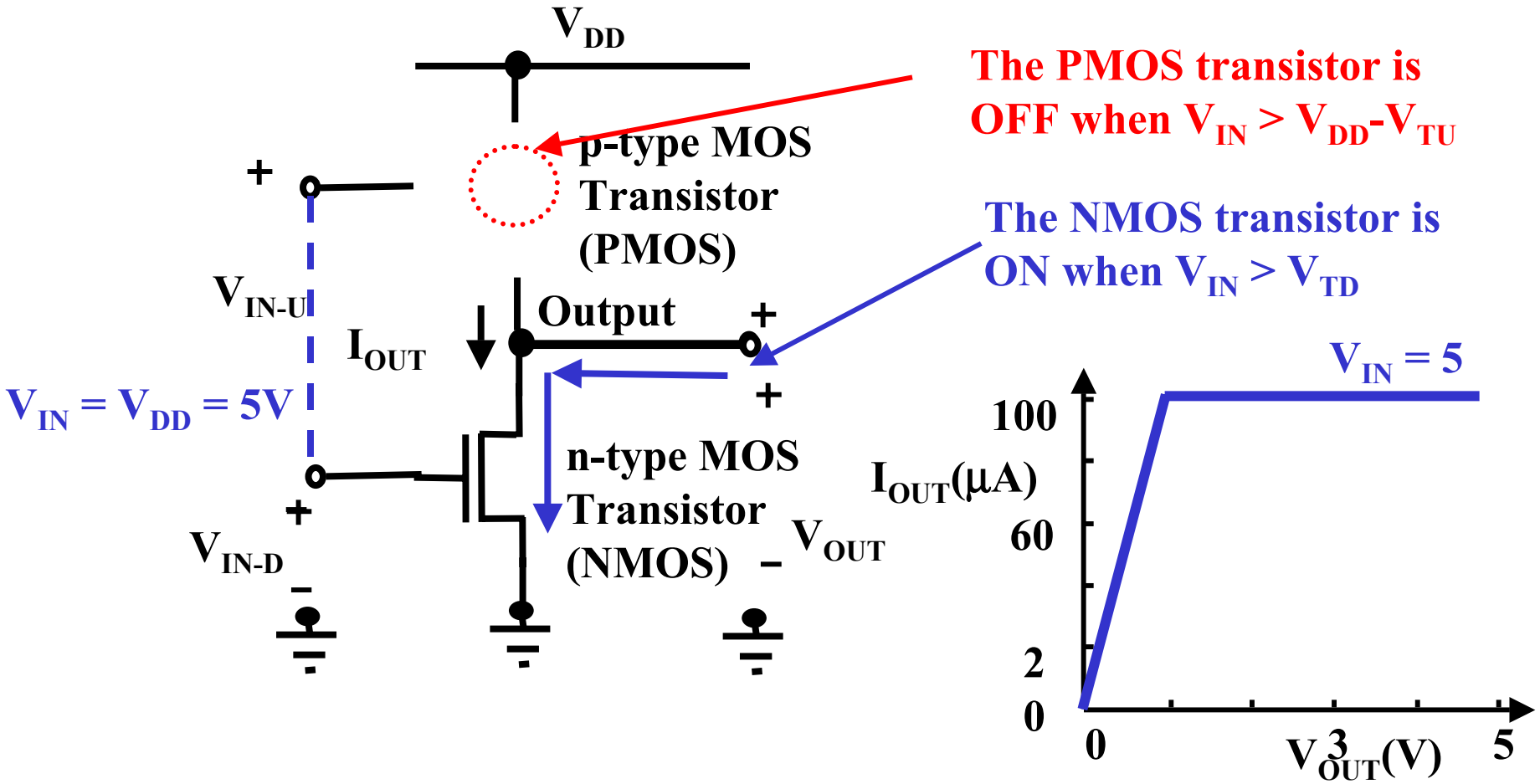
Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

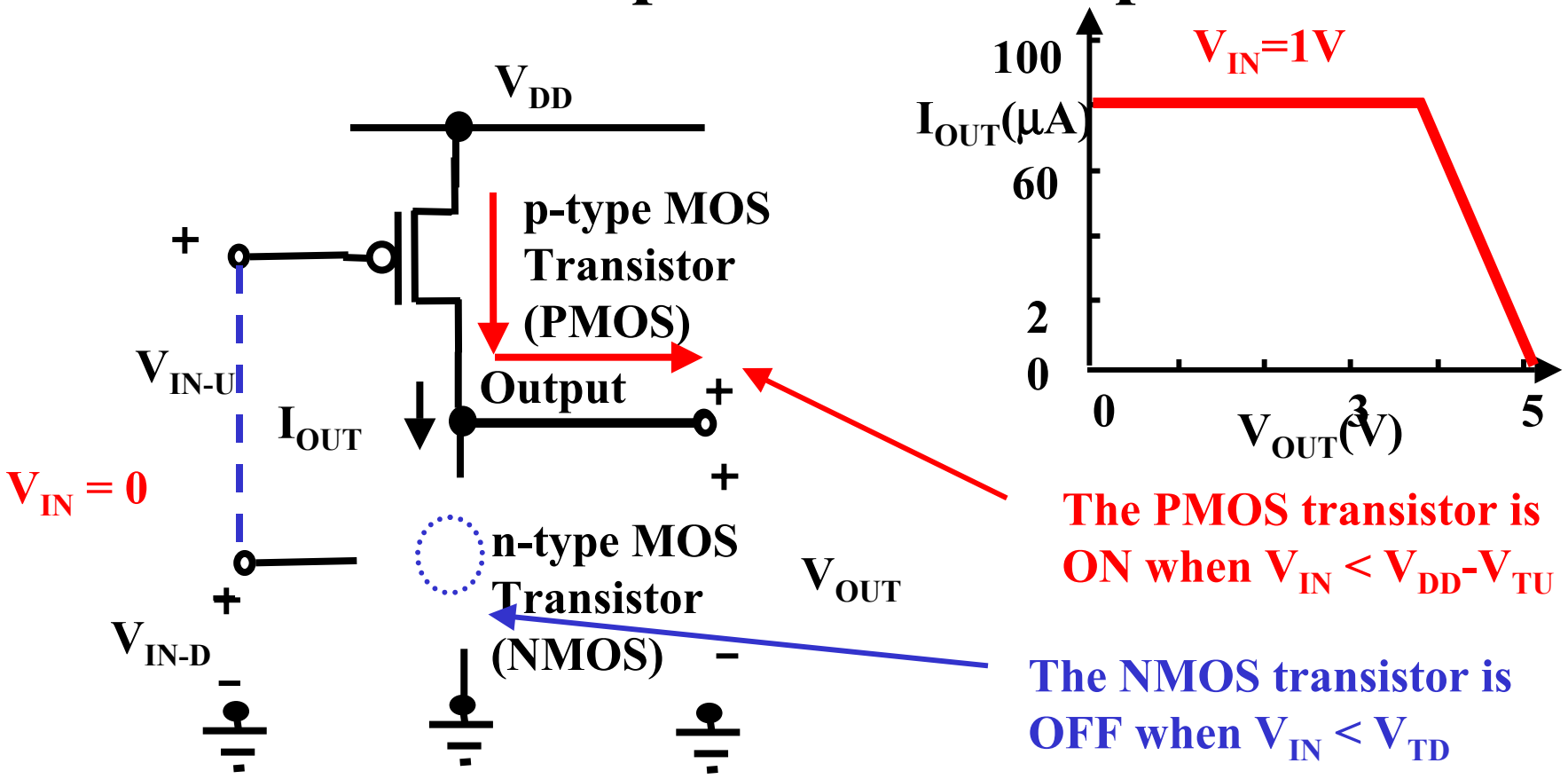




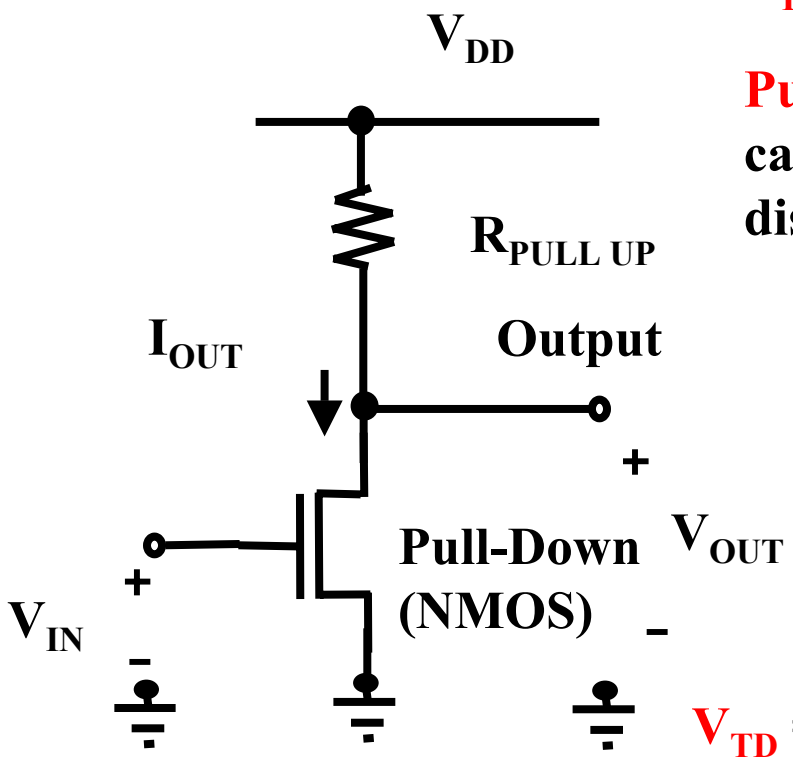
Case #1: $V_{IN} = V_{DD} = 5V$ The Output is Pulled-Down



Case #2: $V_{IN} = 0$
The Output is Pulled-Up



Terminology



V_{DD} = Power supply voltage (D is from Drain)

Pull-Down Network = Set of devices used to carry current from the output node to ground to discharge the output node to ground.

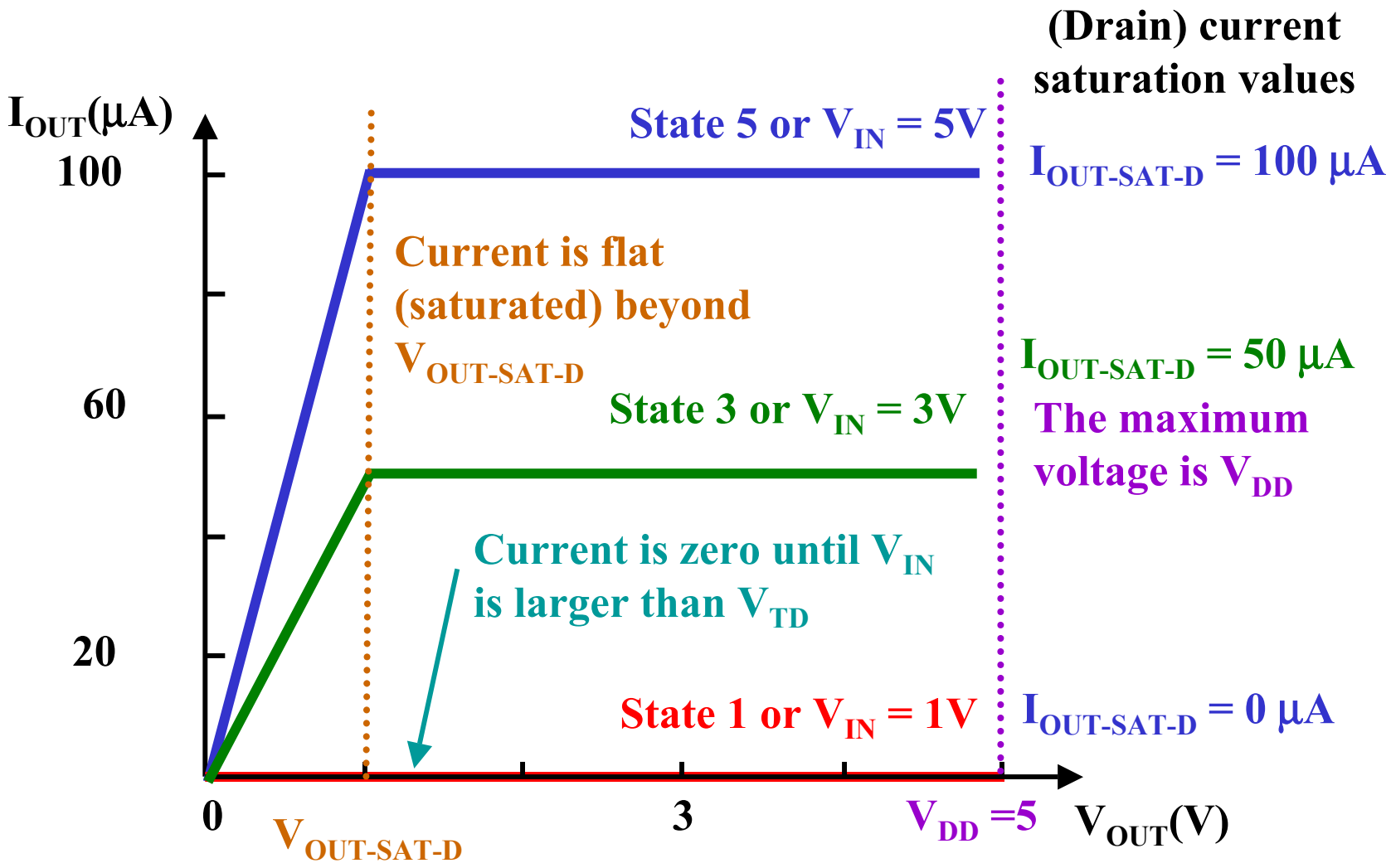
Pull-Up Network = Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.

I_{OUT} = Current for the device under study.

V_{TD} = Threshold Voltage value of V_{IN} at which the Pull-Down (NMOS transistor) begins to conduct.

$V_{OUT-SAT-D}$ = Value of V_{OUT} beyond which the current I_{OUT-D} saturates at the (drain) current saturation value $I_{OUT-SAT-D}$.

States are Voltage Levels of V_{IN}



Saturation Current NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches the saturation current

$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:

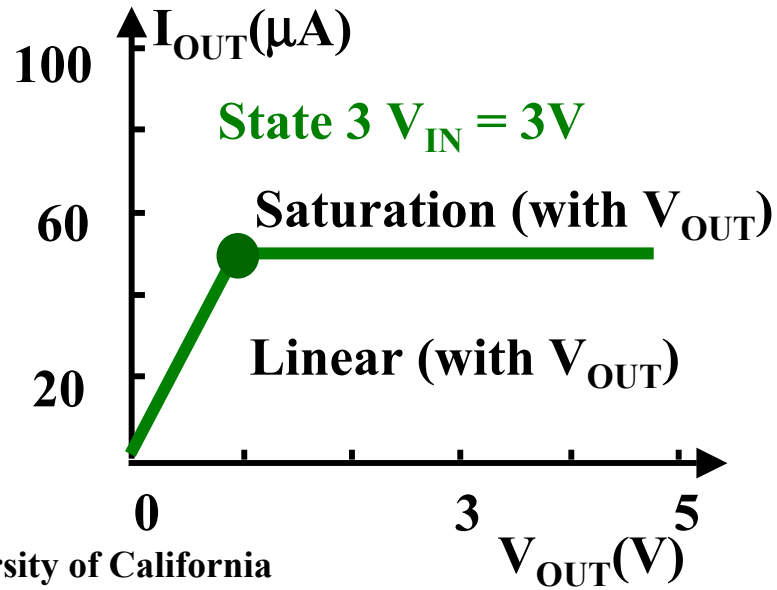
$k_D = 25\ \mu A/V^2$

$V_{TD} = 1V$

$V_{OUT-SAT-D} = 1V$

Use these values in the homework.

$$I_{OUT-SAT-PD} = 25\frac{\mu A}{V^2}\left(3V - 1V\right)1V = 50\mu A$$



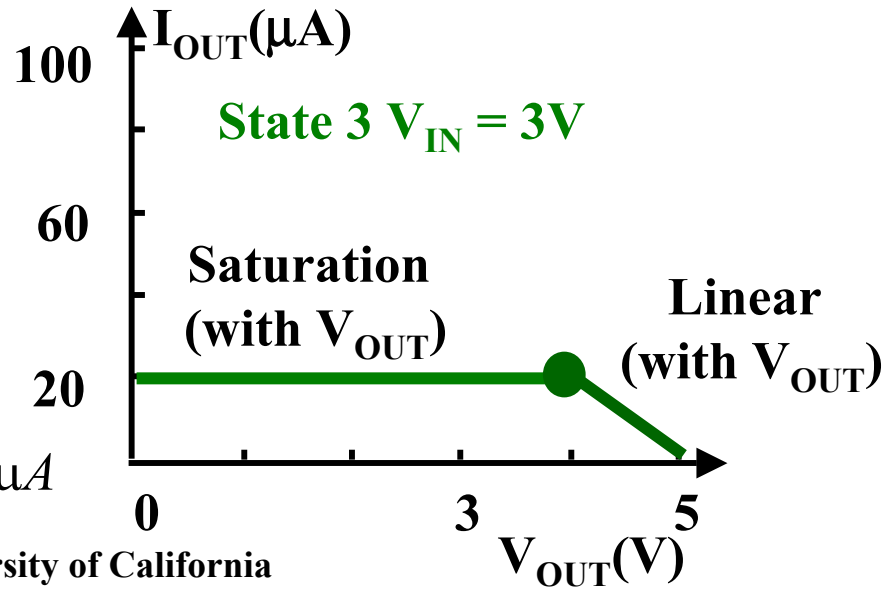
Saturation Current PMOS Model

Current I_{OUT} only flows when V_{IN} is smaller than V_{DD} minus the threshold value V_{TU} and the current is proportional to (V_{DD}-V_{OUT}) up to (V_{DD}-$V_{OUT-SAT-U}$) where it reaches the saturation current

$$I_{OUT-SAT-U} = k_U \left(V_{DD} - V_{IN} - V_{TU}\right) V_{OUT-SAT-U}$$

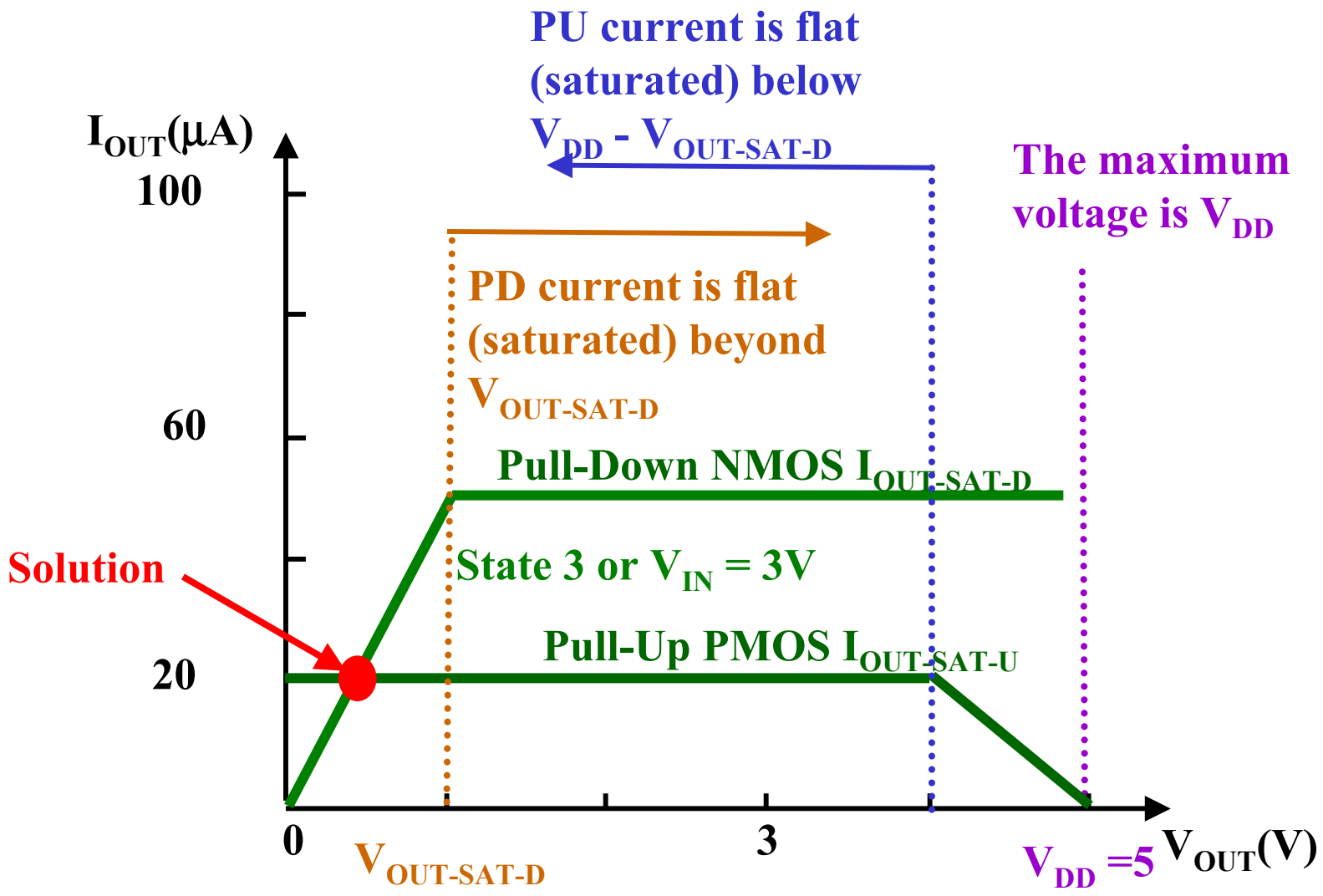
Example:
k_U = 20 μA/V²
V_{TU} = 1V
$V_{OUT-SAT-U}$= 1V

Use these values in the homework.

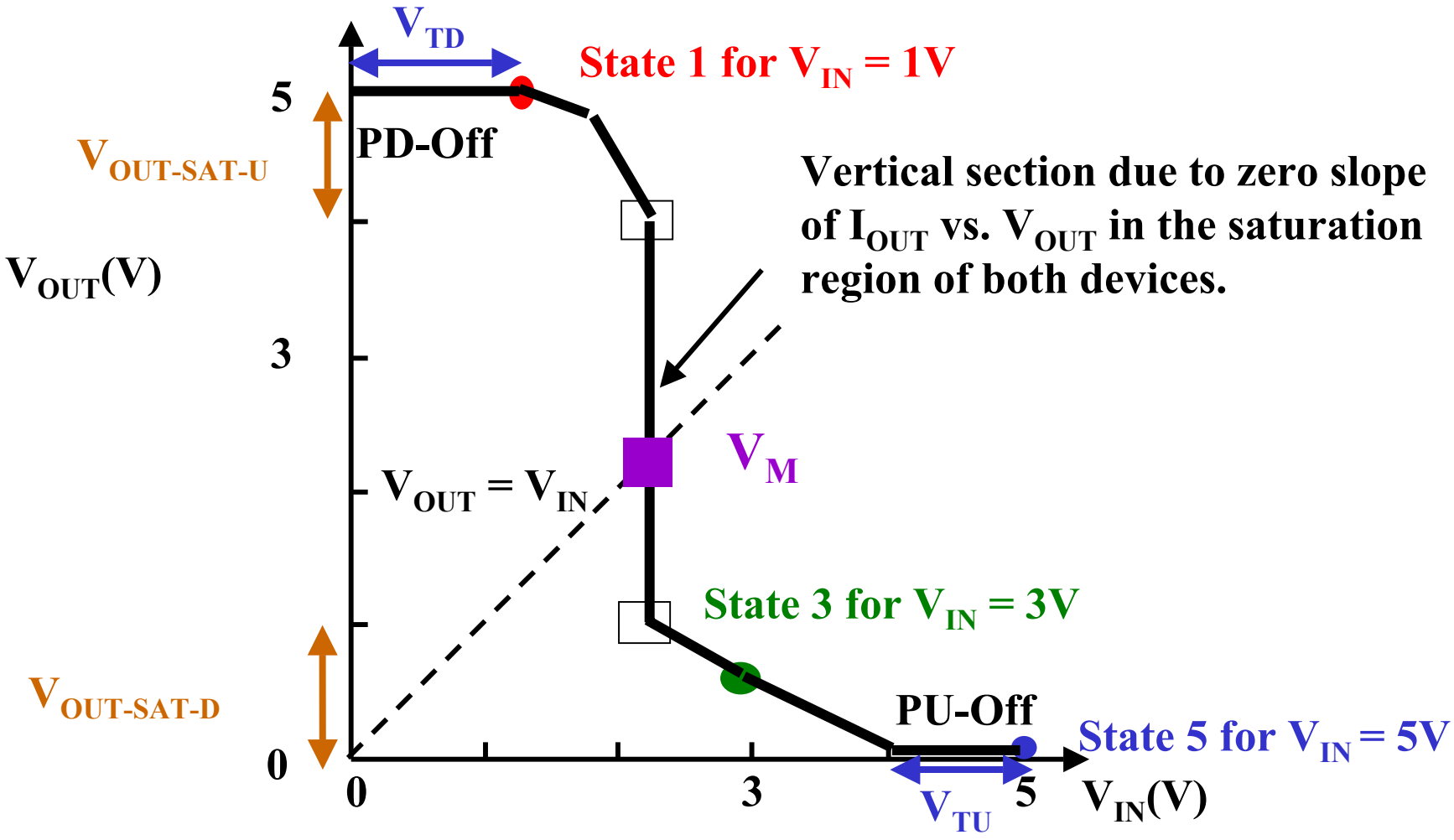


$$I_{OUT-SAT-U} = 20\frac{\mu A}{V^2}\left(5V - 3V - 1V\right)1V = 20\mu A$$

Composite I_{OUT} vs. V_{OUT} for CMOS



Voltage Transfer Function for the Complementary Logic Circuit



Vertical section due to zero slope of I_{OUT} vs. V_{OUT} in the saturation region of both devices.

Method for Finding V_M

At V_M,

1) $V_{OUT} = V_{IN} = V_M$

2) **Both devices are in saturation**

3) $I_{OUT\text{-}SAT\text{-}D} = I_{OUT\text{-}SAT\text{-}U}$

$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

$$= I_{OUT-SAT-U} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{OUT-SAT-U}$$

Substitute V_M

Solve for V_M

Example Result: When $k_D = k_P$, $V_{OUT\text{-}SAT\text{-}D} = V_{OUT\text{-}SAT\text{-}U}$ and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$

Lecture 17: October 29, 2001

Reminder: Quiz and Midterm

Quiz 20 minutes At Start of Class Wed. Oct 31

Covers Material 6th-9th week including HW#9

Midterm in Class Wed. Nov 7th

Covers Material 6th-10th week including HW#10

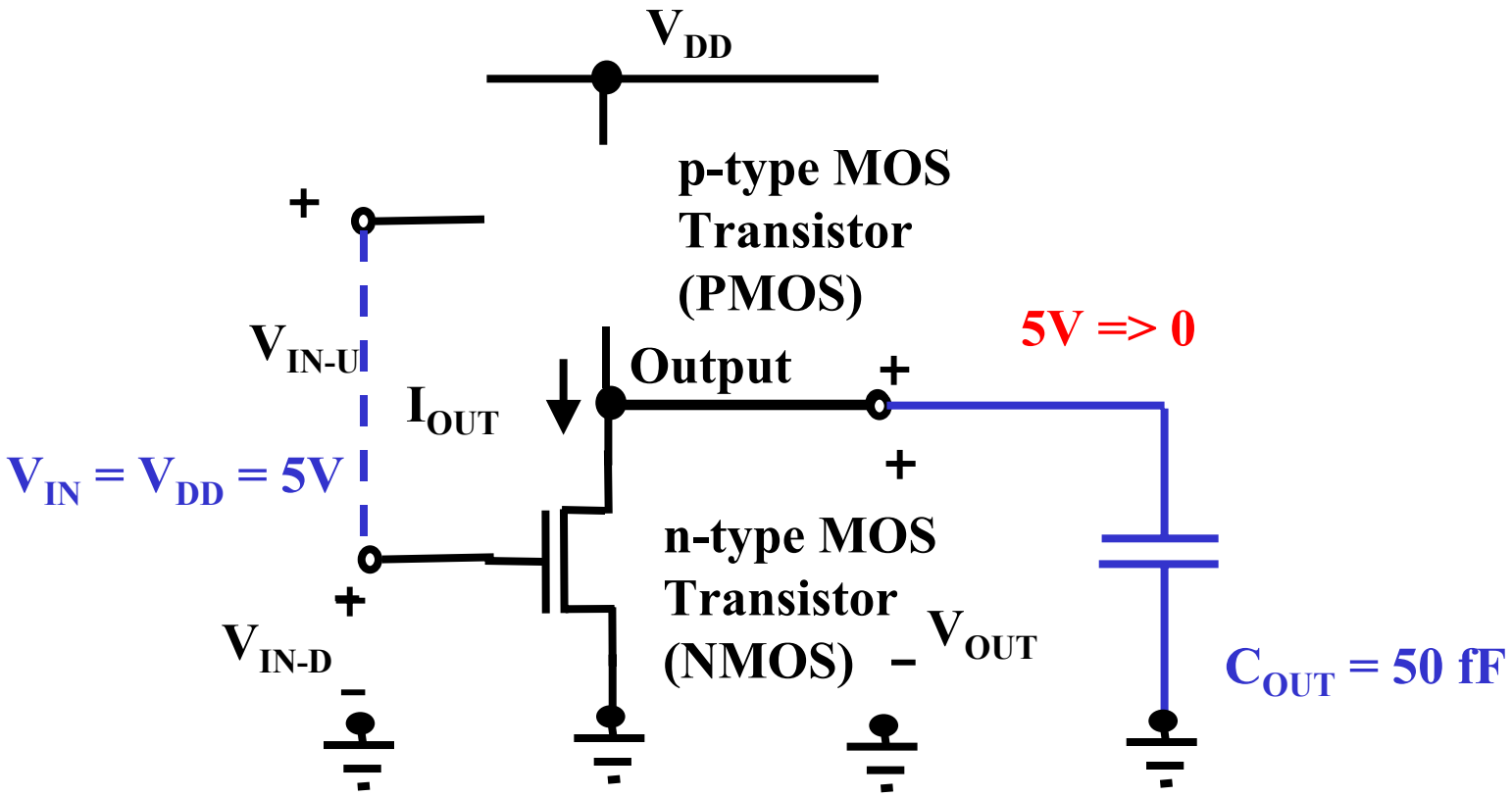
Closed Book, Closed Notes, Bring Calculator, Paper Provided
Last Name A-K 2040 Valley LSB; Last Name L-Z in 10 Evans

Topic Coverage Review in class Oct 31; Old Exams on Web

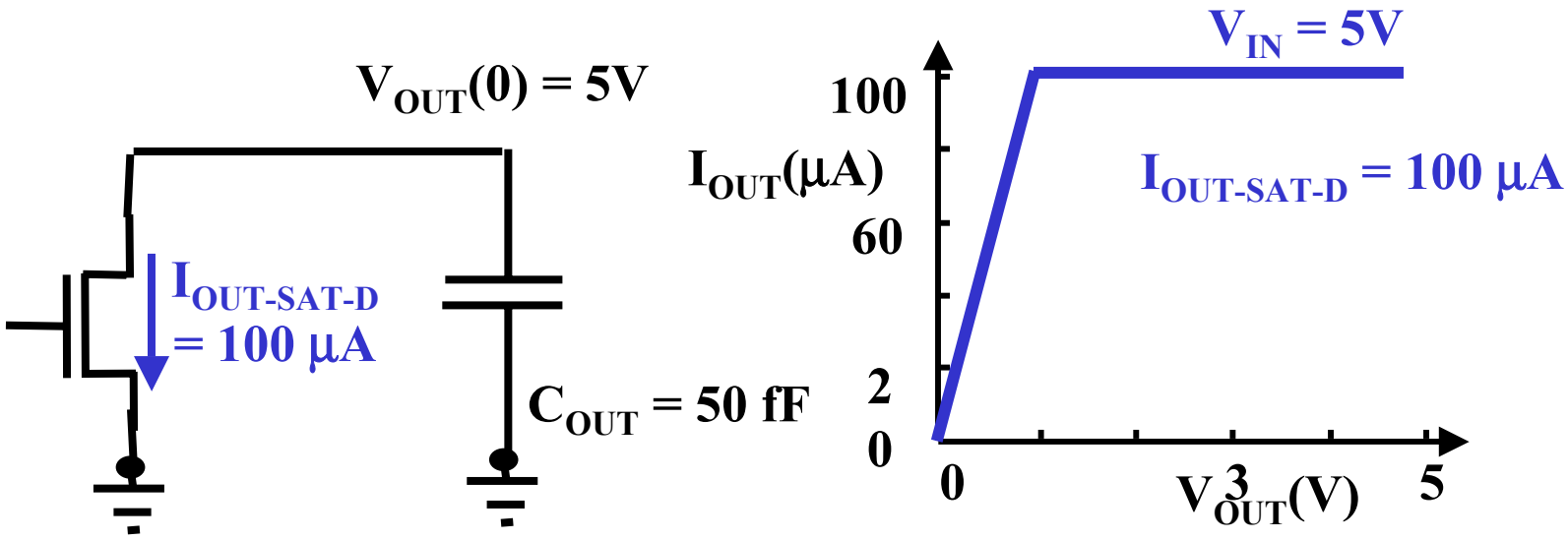
Review Session: Sat 1-2:30 (TBA Evans); Tu 5-6:00 (? Cory)

EE 43 Labs Are Not Cancelled:

Transient Gate Problem: Discharging and Charging Capacitance on the Output



Output Capacitance Voltage vs. Time



When $V_{OUT} > V_{OUT\text{-}SAT\text{-}D}$ the available current is $I_{OUT\text{-}SAT\text{-}D}$

Assume that the necessary voltage swing to cause the next downstream gate to begin to switch is $V_{DD}/2$ or 2.5V. The **propagation delay** is thus

$$\Delta t = \frac{C_{OUT}\Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = \frac{50\,fF \cdot 2.5V}{100\mu A} = 1.25ns$$

Switched Equivalent Resistance Model

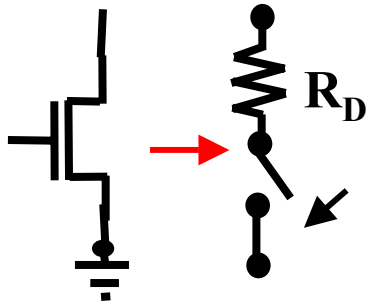
The above model assumes the device is an ideal constant current source.

1) This is not true below $V_{OUT\text{-}SAT\text{-}D}$ and leads to in accuracies.

2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting $0.69R_DC$ equal to the Δt found above

$$\Delta t = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_DC_{OUT}$$

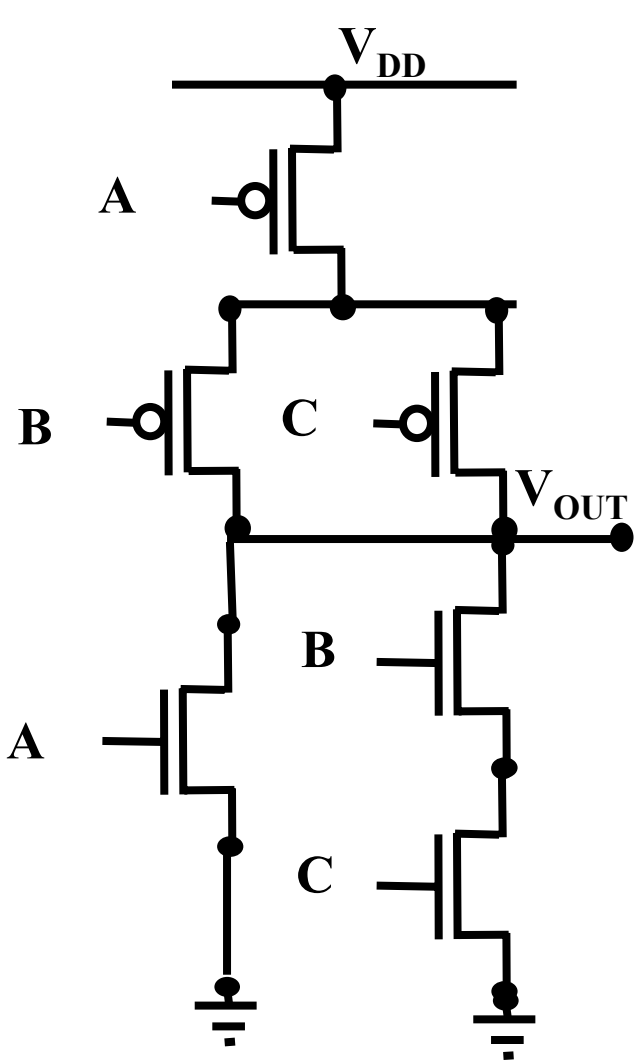


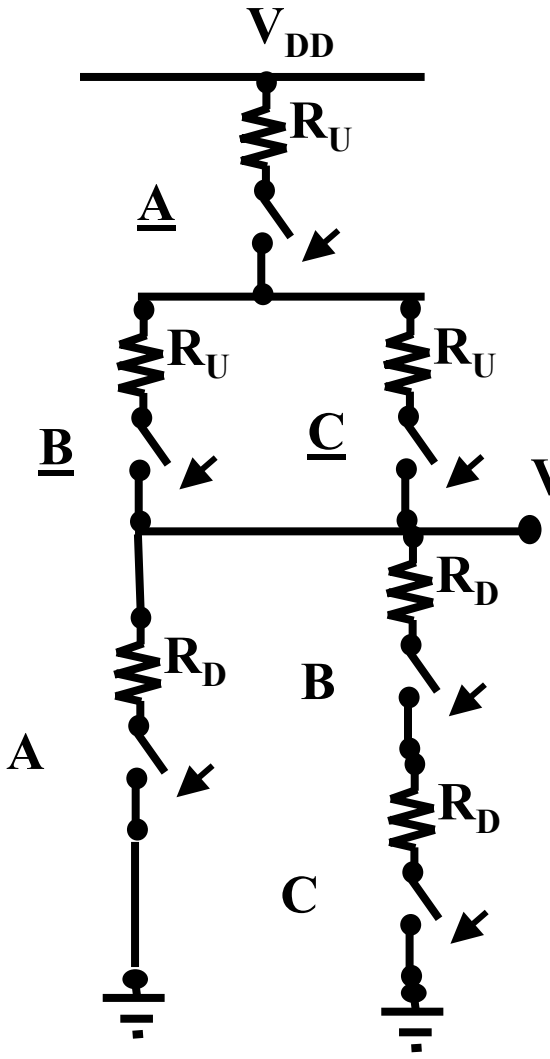
This gives

$$R_D = \frac{V_{DD}}{2\cdot(0.69)I_{OUT-SAT-D}} \approx \frac{3}{4}\frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4}\frac{5V}{100\mu A} = 37.5k\Omega$$

Each device can now be replaced by this equivalent resistor.

Switched Equivalent Resistance Network





Switches close when input is low.

Switches close when input is high.

Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

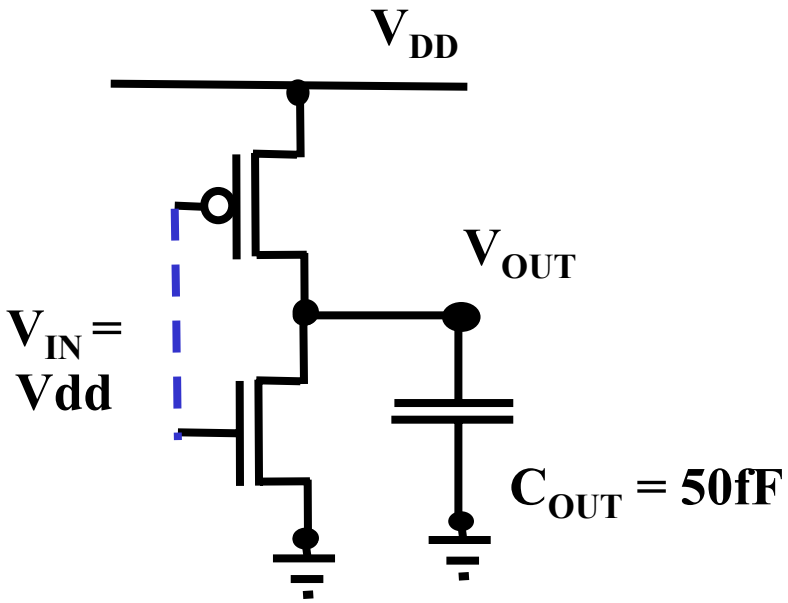
Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

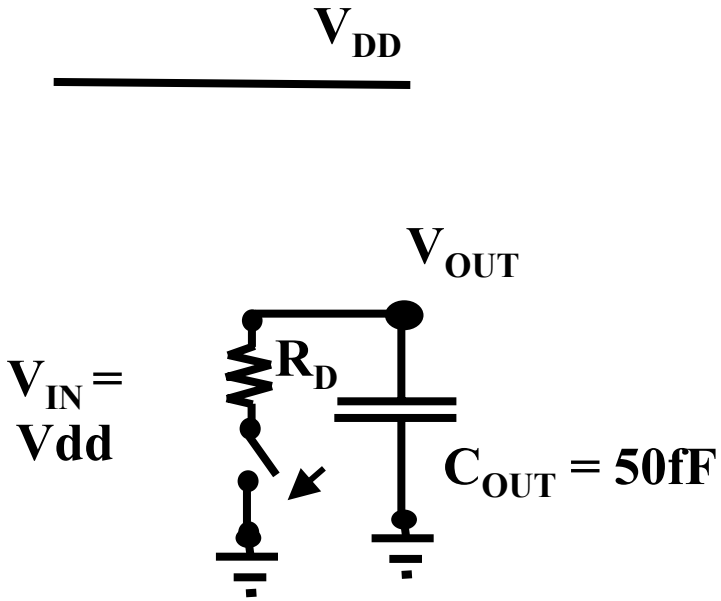
The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume $R_D = R_U = 10\ k\Omega$

Inverter Propagation Delay

Discharge (pull-down)



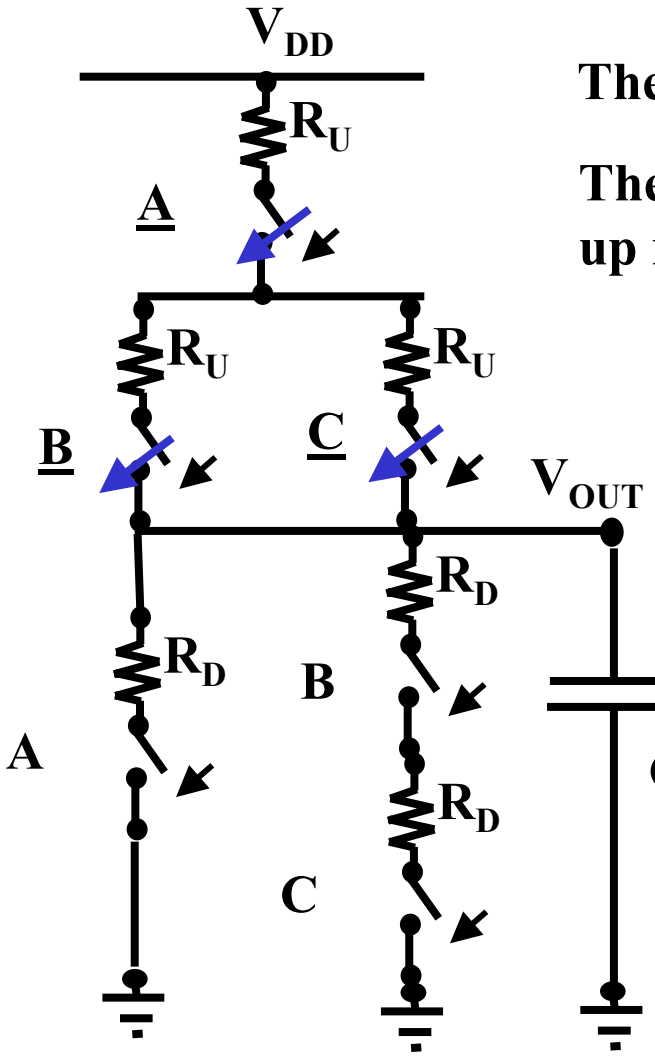


$$\Delta t = 0.69 R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps}$$

Discharge (pull-up)

$$\Delta t = 0.69 R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps}$$

Logic Gate Propagation Delay



The initial state depends on the previous inputs.

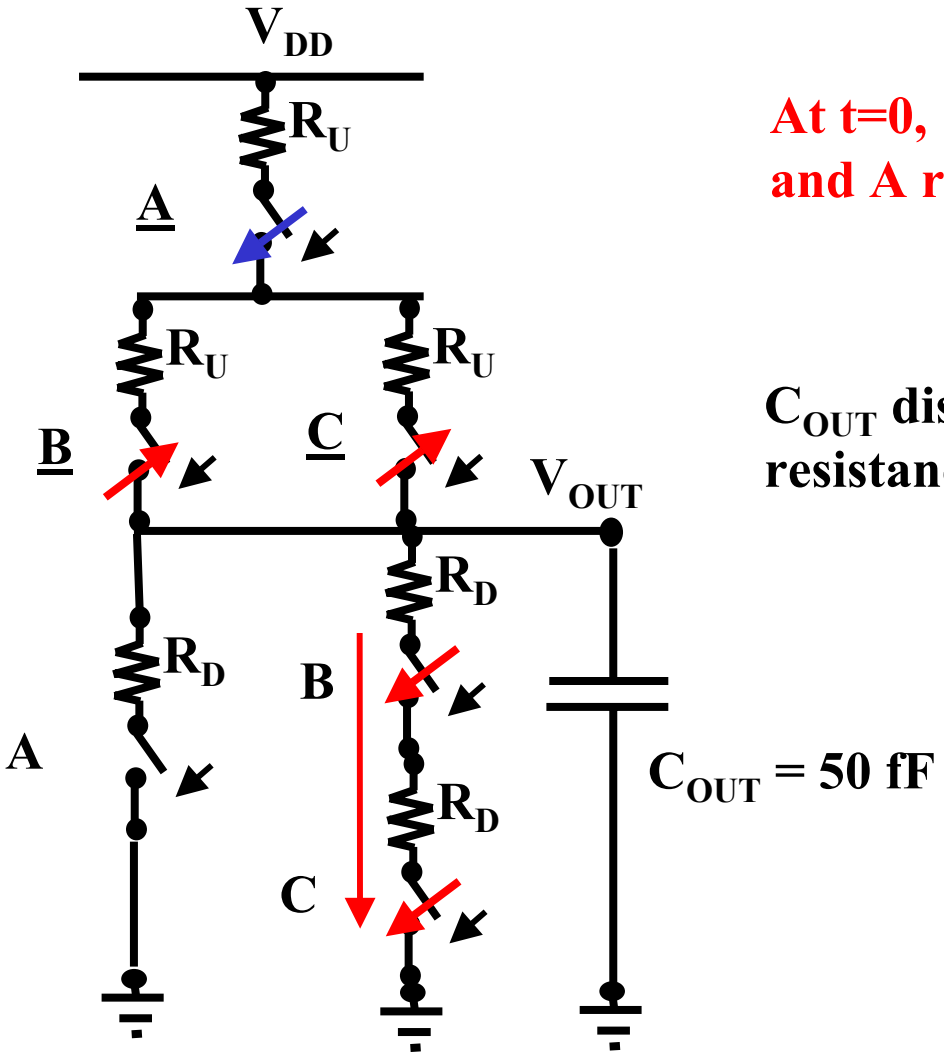
The equivalent resistance of the pull-down or pull-up network depends on the current input state.

Example: A=0, B=0, C=0 for a long time.

The capacitor has precharged up to V_{DD} = 5V.

C_{OUT} = 50 fF

Logic Gate Propagation Delay (Cont.)



At t=0, B and C switch to high = V_{DD} and A remains low.

C_{OUT} discharges through the pull-down resistance of gates B and C in series.

$$\Delta t = 0.69(R_{DB}+R_{DC})C_{OUT}$$
$$= 0.69(20k\Omega)(50fF) = 690 \text{ ps}$$

The propagation delay is two times longer than that for the inverter!