Lecture 18: October 31, 2001

Logic Switched Resistor Model

A) Worst Case Input Scenario

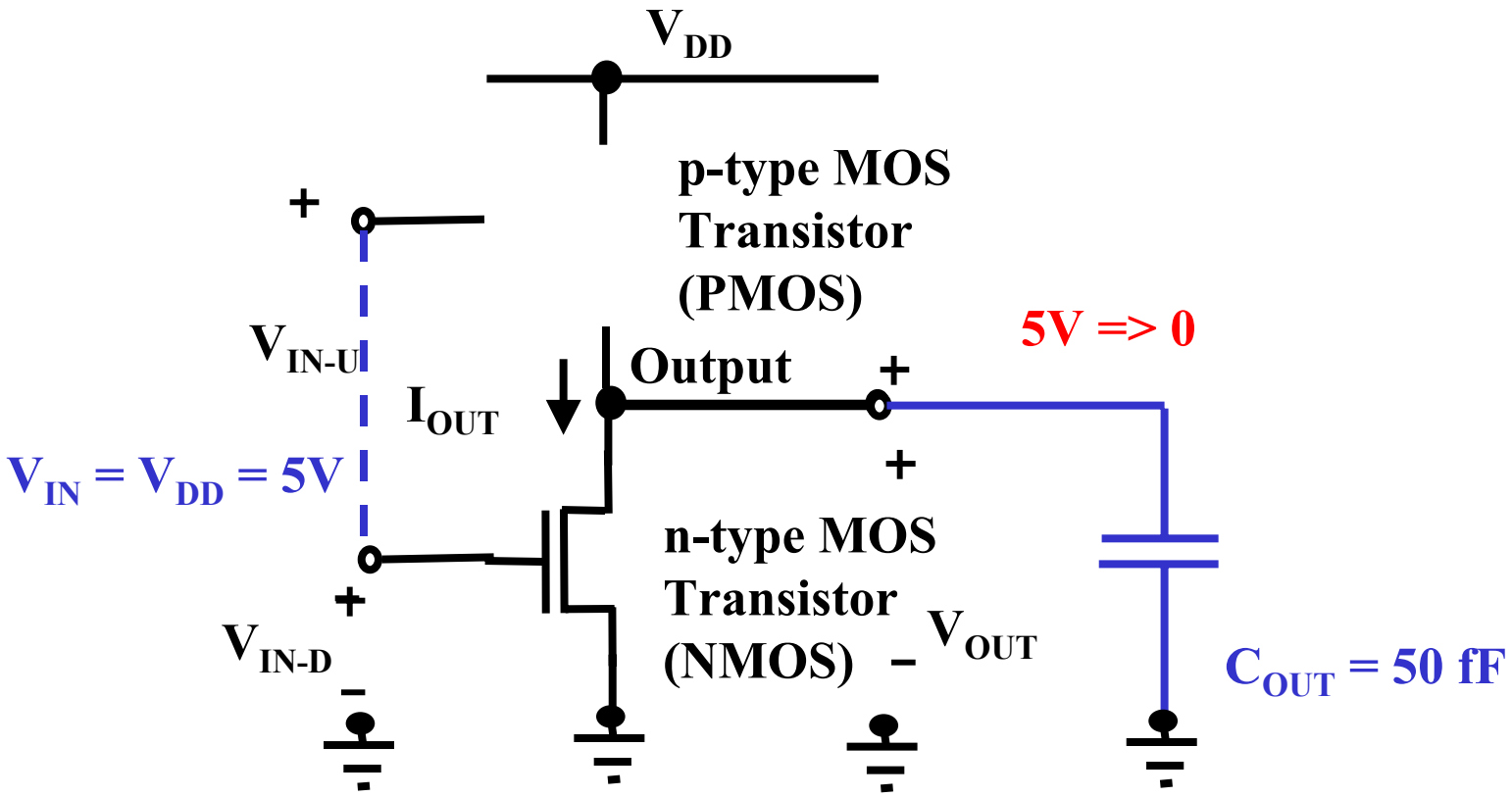
B) Cascade Stages for Many Inputs

C) Typical 0.25 μm Device Parameters

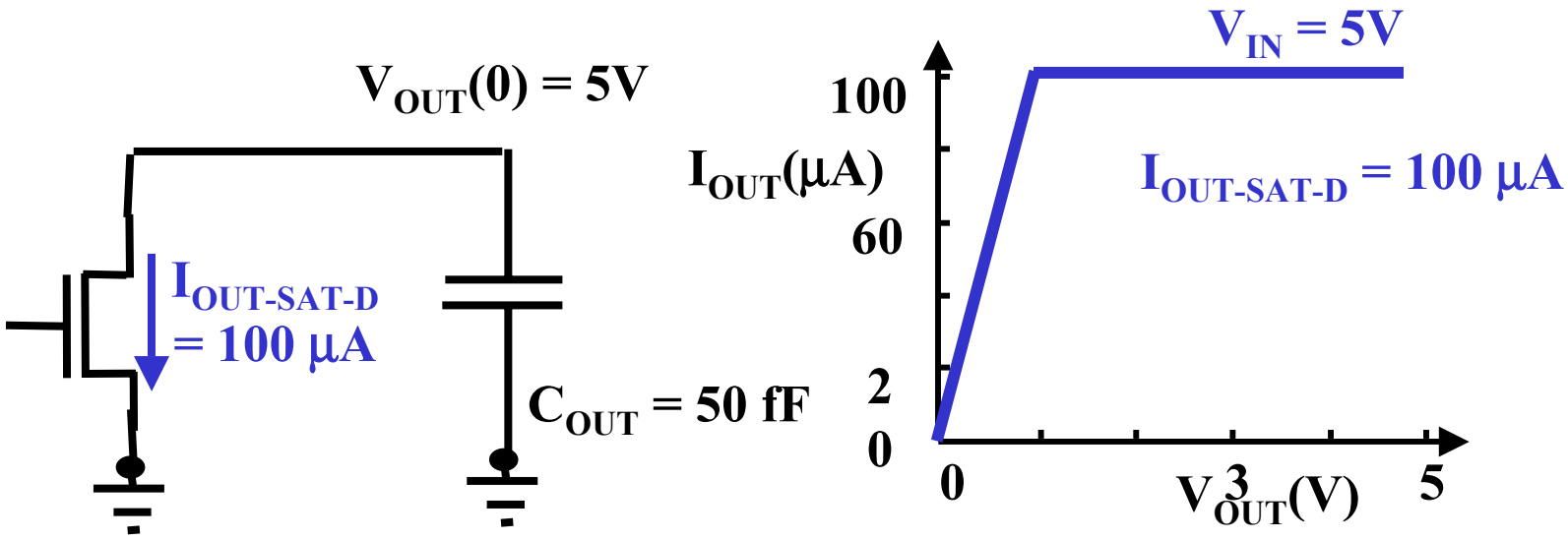
Reading:

lecture viewgraphs

Transient Gate Problem: Discharging and Charging Capacitance on the Output



Output Capacitance Voltage vs. Time



When $V_{OUT} > V_{OUT-SAT-D}$ the available current is $I_{OUT-SAT-D}$

Assume that the necessary voltage swing to cause the next downstream gate to begin to switch is $V_{DD}/2$ or 2.5V. The **propagation delay** is thus

$$\Delta t = \frac{C_{OUT}\Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = \frac{50\,fF \cdot 2.5V}{100\mu A} = 1.25ns$$

Switched Equivalent Resistance Model

The above model assumes the device is an ideal constant current source.

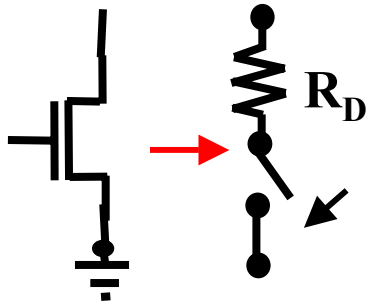
1) This is not true below $V_{OUT\text{-}SAT\text{-}D}$ and leads to in accuracies.

2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting $0.69R_DC$ equal to the Δt found above

This gives

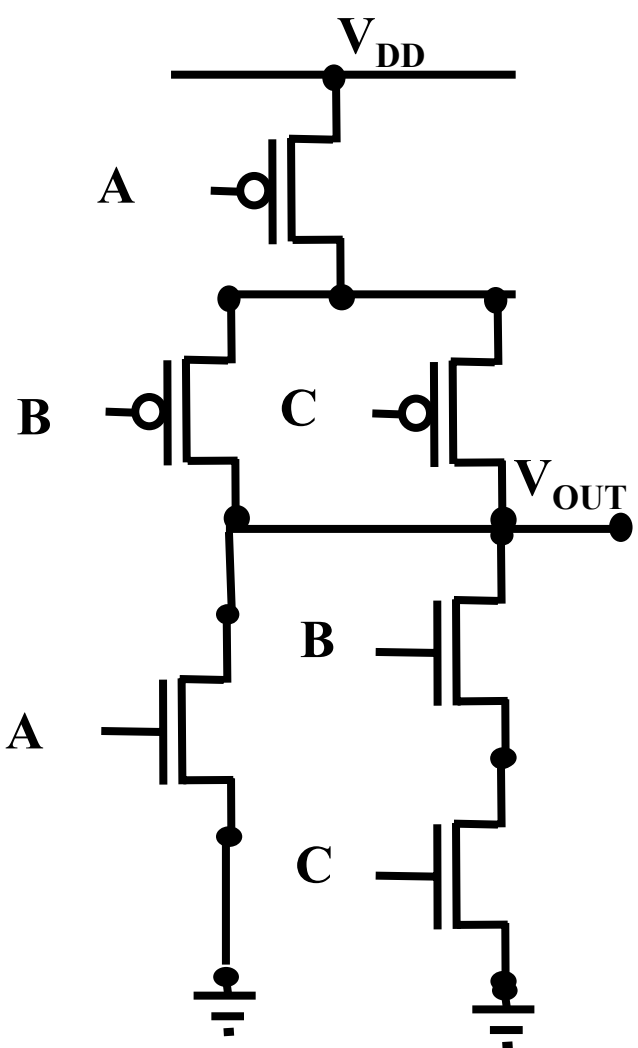
$$\Delta t = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_DC_{OUT}$$

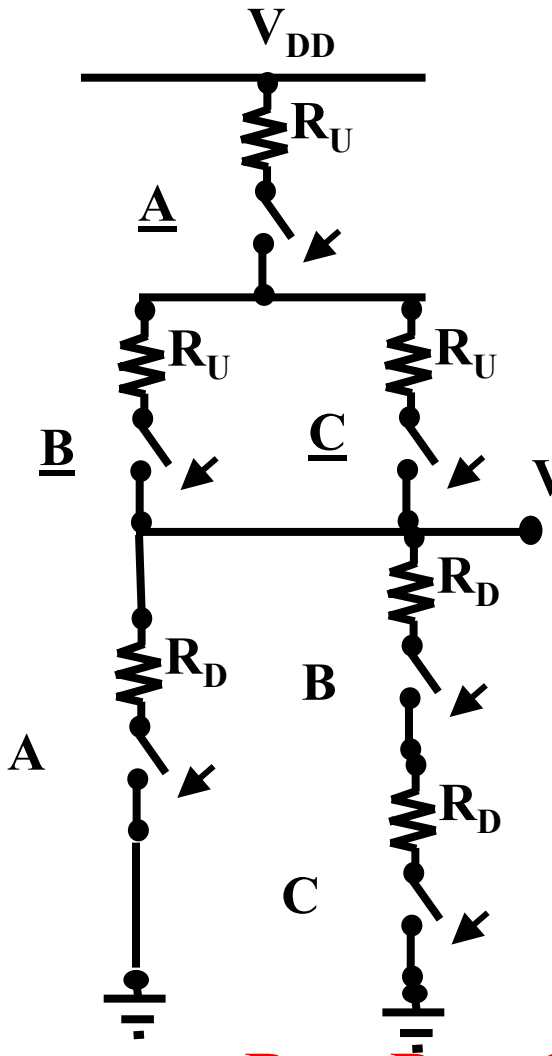


$$R_D = \frac{V_{DD}}{2\cdot(0.69)I_{OUT-SAT-D}} \approx \frac{3}{4}\frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4}\frac{5V}{100\mu A} = 37.5k\Omega$$

Each device can now be replaced by this equivalent resistor.

Switched Equivalent Resistance Network





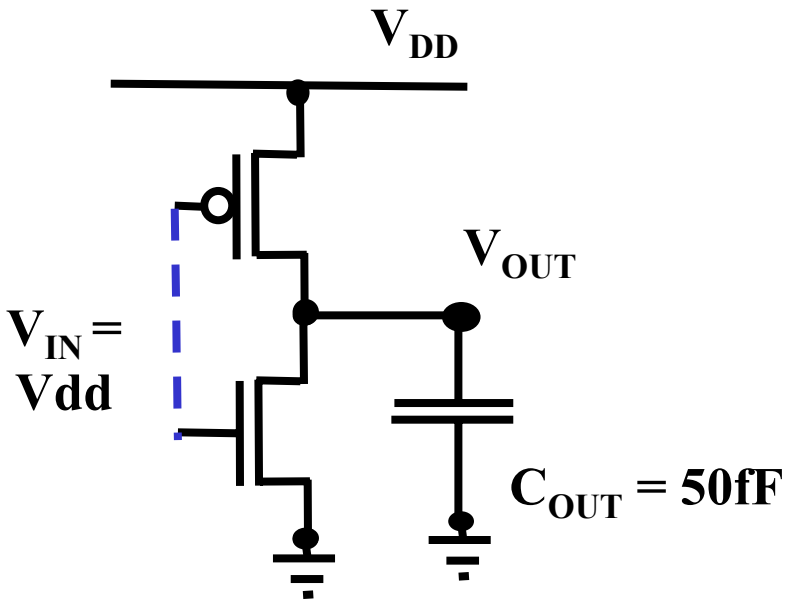
Switches **open** when input is **high**.

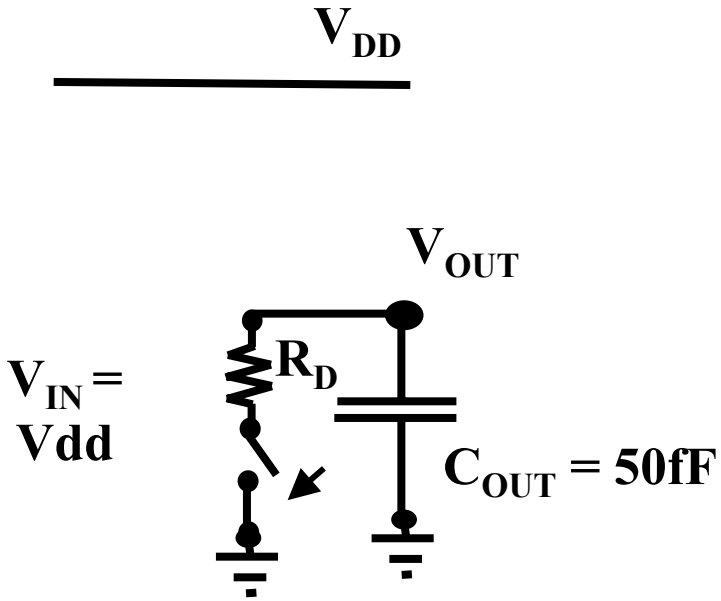
Switches **close** when input is **high**.

For convenience in EE 42 we assume $R_D = R_U = 10\ k\Omega$

Inverter Propagation Delay

Discharge (pull-down)



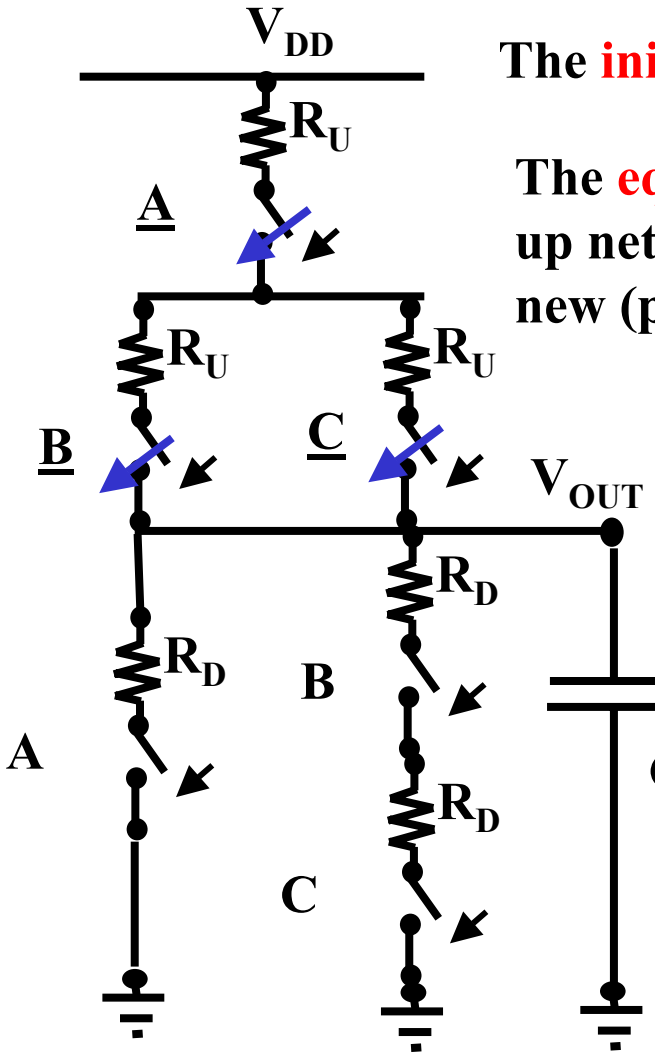


$$\Delta t = 0.69 R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps}$$

Discharge (pull-up)

$$\Delta t = 0.69 R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345 \text{ ps}$$

Logic Gate Propagation Delay: Initial State



The initial state depends on the old (previous) inputs.

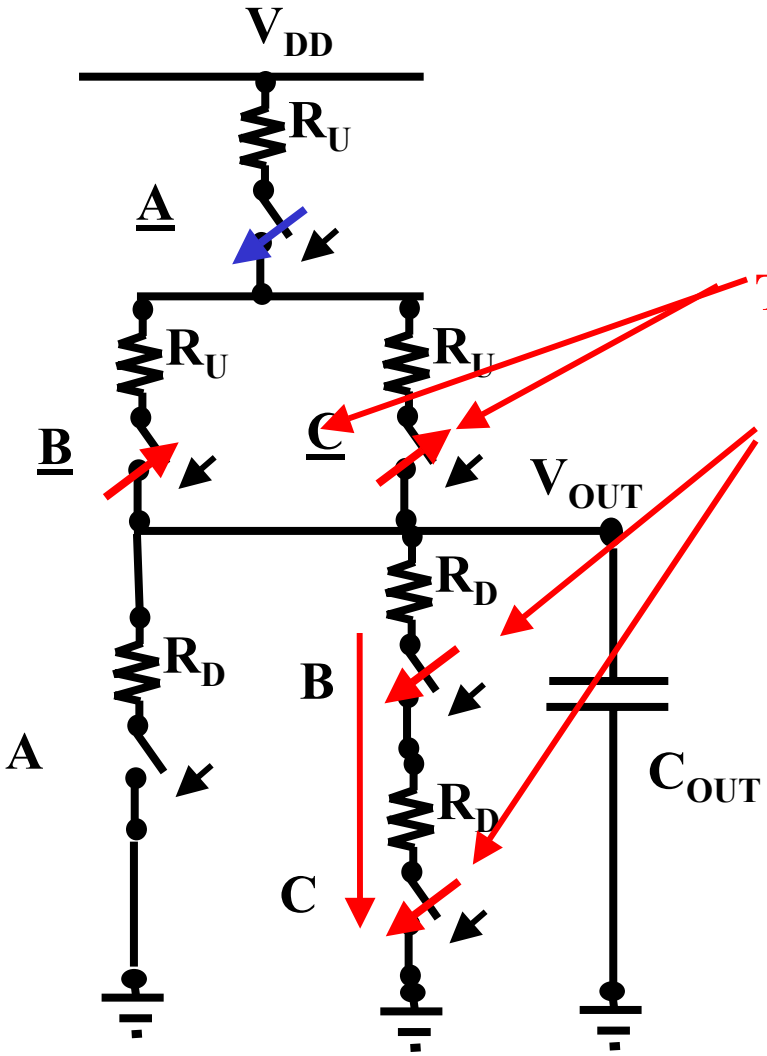
The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

These inputs provided a path to V_{DD} for a long time and the capacitor has precharged up to V_{DD} = 5V.

C_{OUT} = 50 fF

Logic Gate Propagation Delay: Transient



At t=0, B and C switch from low to high (V_{DD}) and A remains low.

This breaks the path from V_{OUT} to V_{DD}

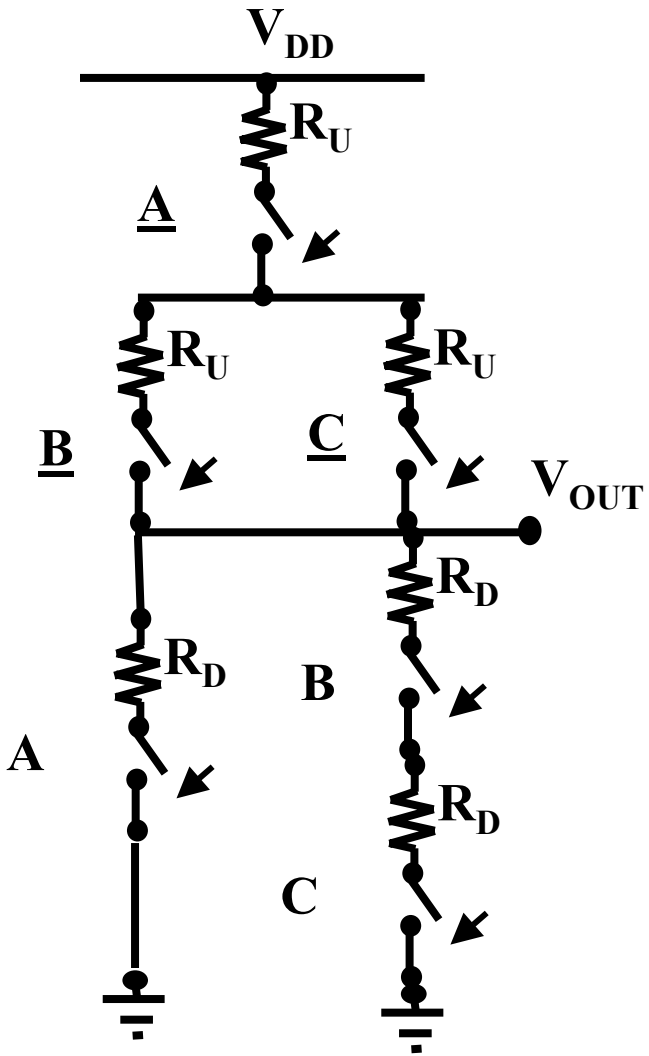
And opens a path from V_{OUT} to GND

C_{OUT} discharges through the pull-down resistance of gates B and C in series.

$$\Delta t = 0.69(R_{DB}+R_{DC})C_{OUT}$$
$$= 0.69(20k\Omega)(50fF) = 690 \text{ ps}$$

The propagation delay is two times longer than that for the inverter!

Logic Gate: Worst Case Scenarios



What combination of previous and present logic inputs will make the Pull-Up the fastest?

What combination of previous and present logic inputs will make the Pull-Up the slowest?

What combination of previous and present logic inputs will make the Pull-Down the fastest?

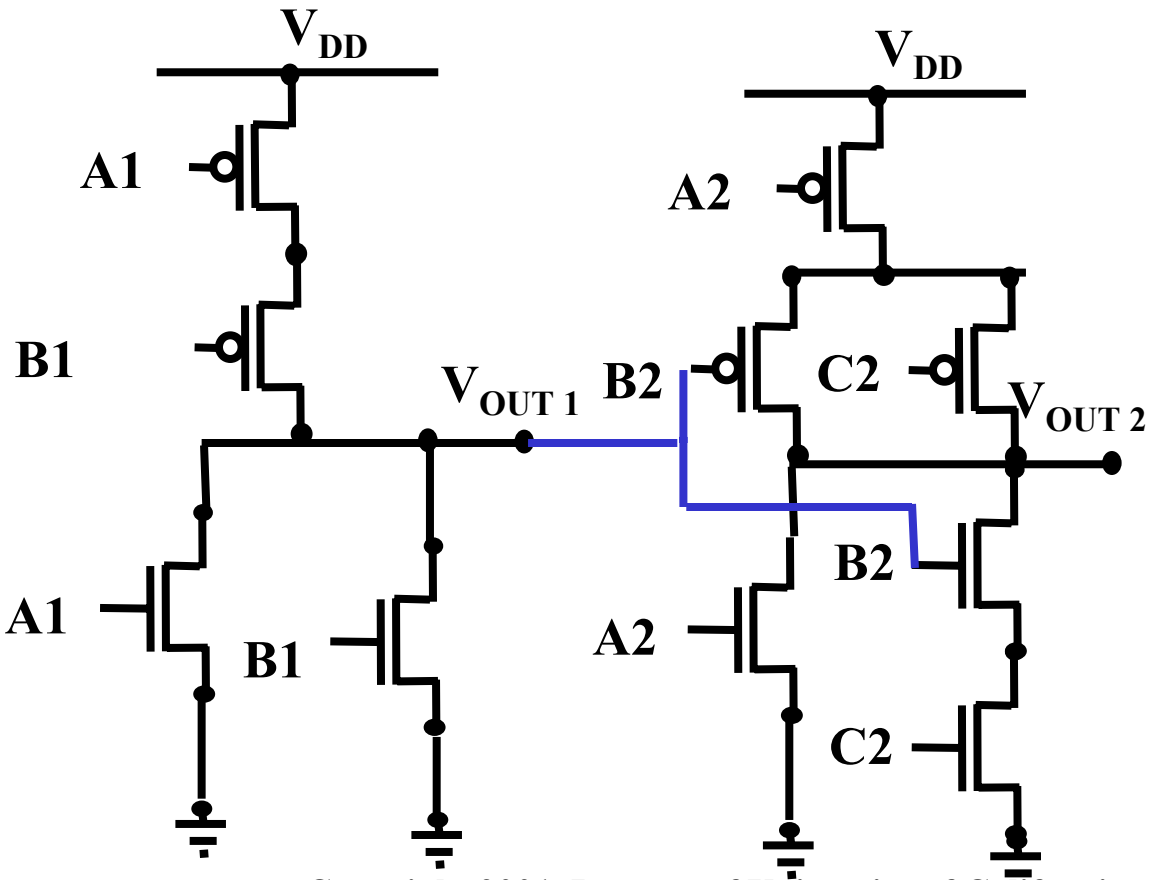
What combination of previous and present logic inputs will make the Pull-Down the slowest?

Fastest overall?

Slowest overall?

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



$B2 = V_{OUT\ 1}$

The four independent input are A1, B1, A2 and C2.

A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output

Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

The current per unit width of the gate increases nearly inversely with the linewidth.

CMOS Device Parameters at 0.25μm

Gate length is 0.25 μm = 250 nm

V_{DD} = 2.5V

A minimum sized device has W =0.5 μm and L = 0.25 μm so W/L=2

$$k = k' \frac{(W/L)}{(W/L)_{\min}}$$

	V_T(V)	$V_{OUT\text{-}SAT}$ (V)	k' (μA/V^2)
NMOS	0.43	0.63	115
PMOS	0.4	1	30

$$I_{OUT-SAT-D} = (115\mu A/V^2)(\frac{2}{2})(2.5V - 0.43V)(0.63V) = 150\mu A$$