# Lecture 19: November 5, 2001

**Midterm in Class Wed. Nov 7th**

**Covers Material 6th-10th week including HW#10**

**Closed Book, Closed Notes, Bring Calculator, Paper Provided**
**Last Name A-K 2040 Valley LSB; Last Name L-Z in 10 Evans**

**Review Session: Sat 1-2:30 (241 Cory); Tu 5-6:00 (241 Cory)**

**EE 43 Labs Are Not Cancelled:**

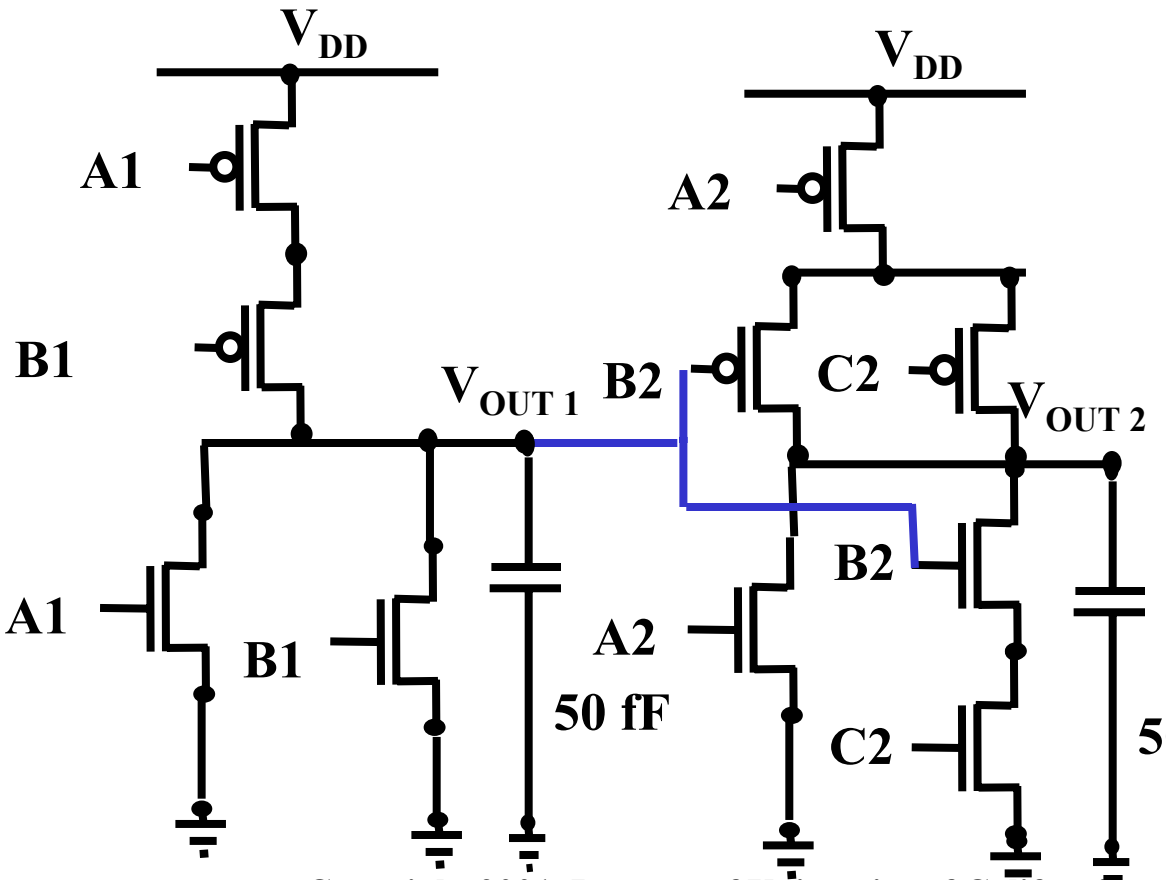
**Flip-Flops**

A) Synchronization: Clocks and Latches
B) Two Stage Latch
C) Memory Requires Feedback
D) Simple Flip-Flop Gate

**Reading: Schwarz and Oldham 11.3 and lecture viewgraphs**

# Logic Gate Cascade

**To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.**




$B2 = V_{OUT\ 1}$

**The four independent input are A1, B1, A2 and C2.**

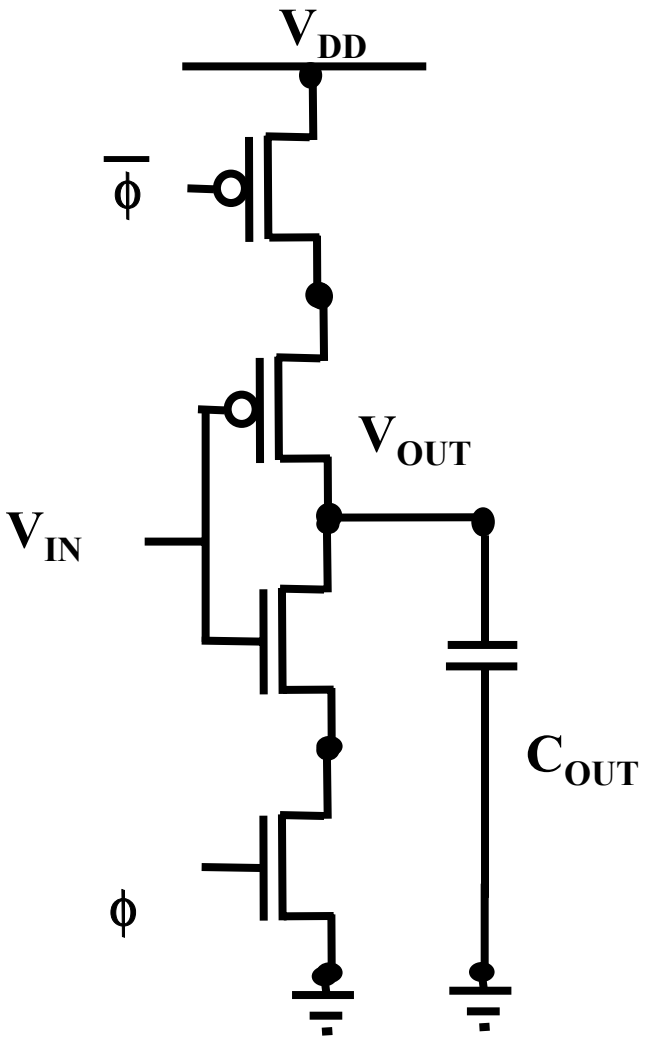
**A2 high discharges gate 2 without even waiting for the output of gate 1.**

**C2 high and A2 low makes gate 2 wait for Gate 1 output**

# Data Synchronization problem

- Combinatorial logic gates can give incorrect answers prematurely and may take several gate propagation delays produce an answer.
- Clocks (signals as to when to proceed) and latches (which capture and hold the correct outputs) can provide synchronization.

# Latch Controlled by a Clock

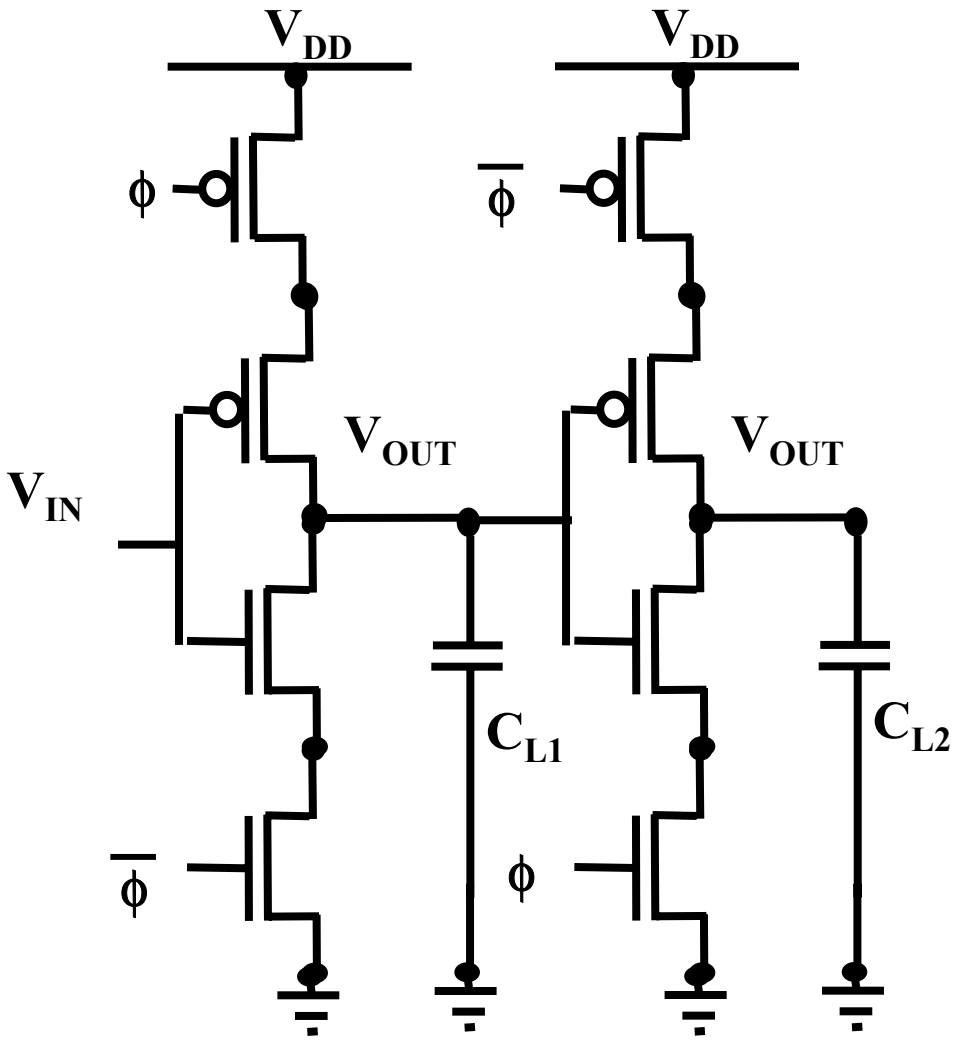



**An inverter with clocked devices in series can form a latch.**

**When the clock $\phi$ is high its complement $\overline{\phi}$ is low and the inverter operates.**

**To synchronize the data the clock remains low until the data is correct at all locations on the chip. When the clock goes high the inverse of the data is passed.**

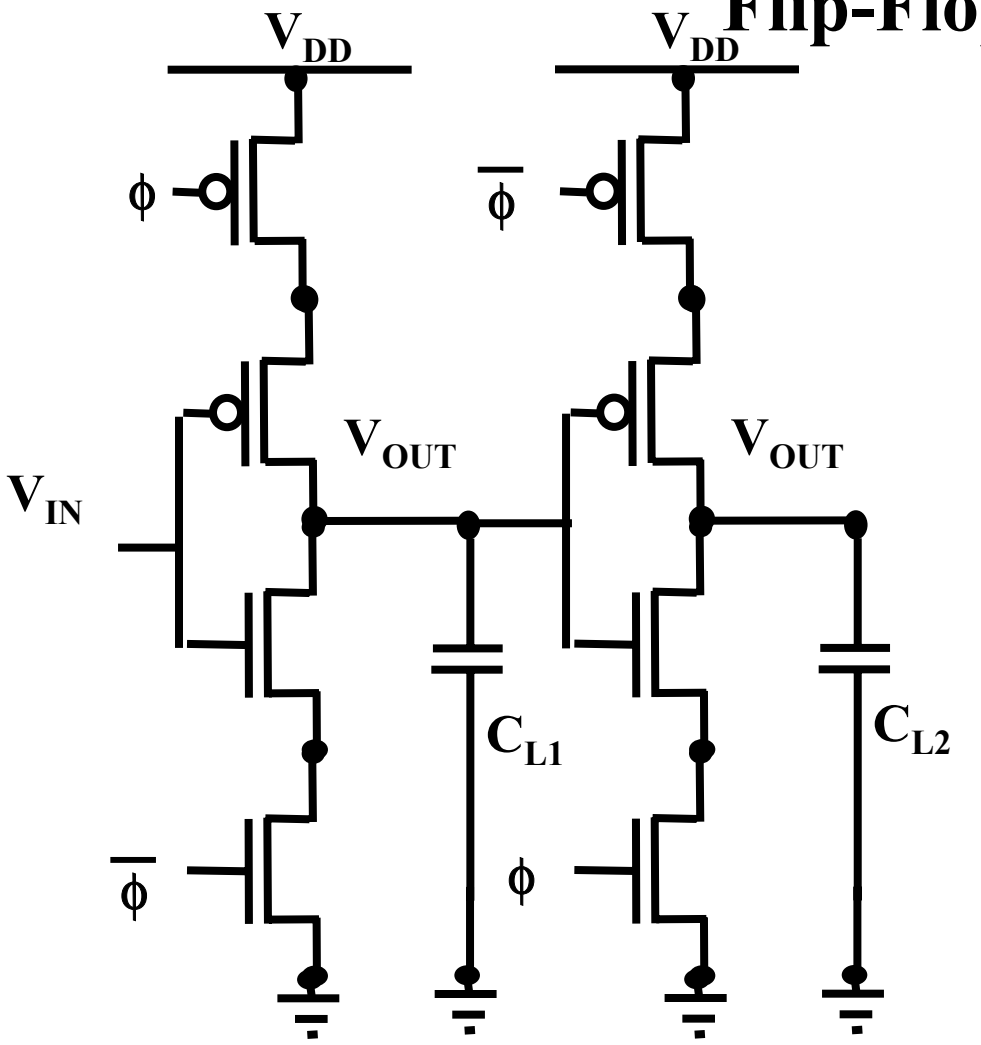
# Latch Work Best In Pairs




**The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges $C_{L1}$.**

**The second stage operates while the clock is high and inverts the signal on $C_{L1}$ to charge or discharge $C_{L2}$ and downstream logic gate inputs.**

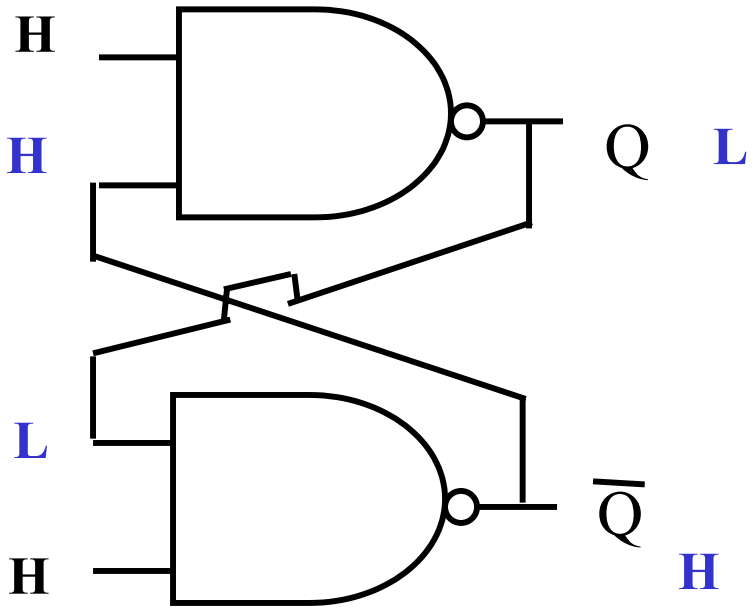
# A Double Latch is an Edge-Triggered D Type Flip-Flop



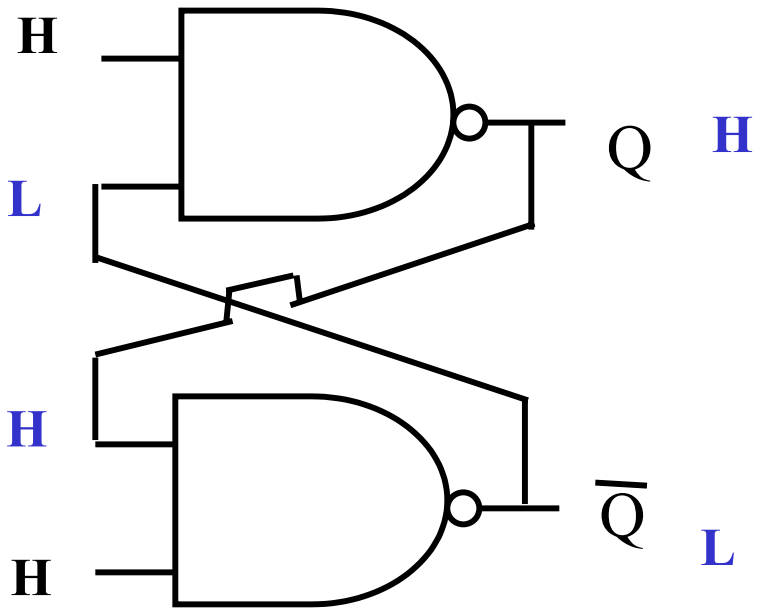

During the low part of the clock cycle this circuit records the input value and when the clock goes high drives $V_{OUT\,2}$ to the voltage level that arrived. (This is the classic function of a D flip-flop.)

Note that this circuit is not fooled by noise on the input and makes its decision on the rising edge of the clock (edge-triggered).

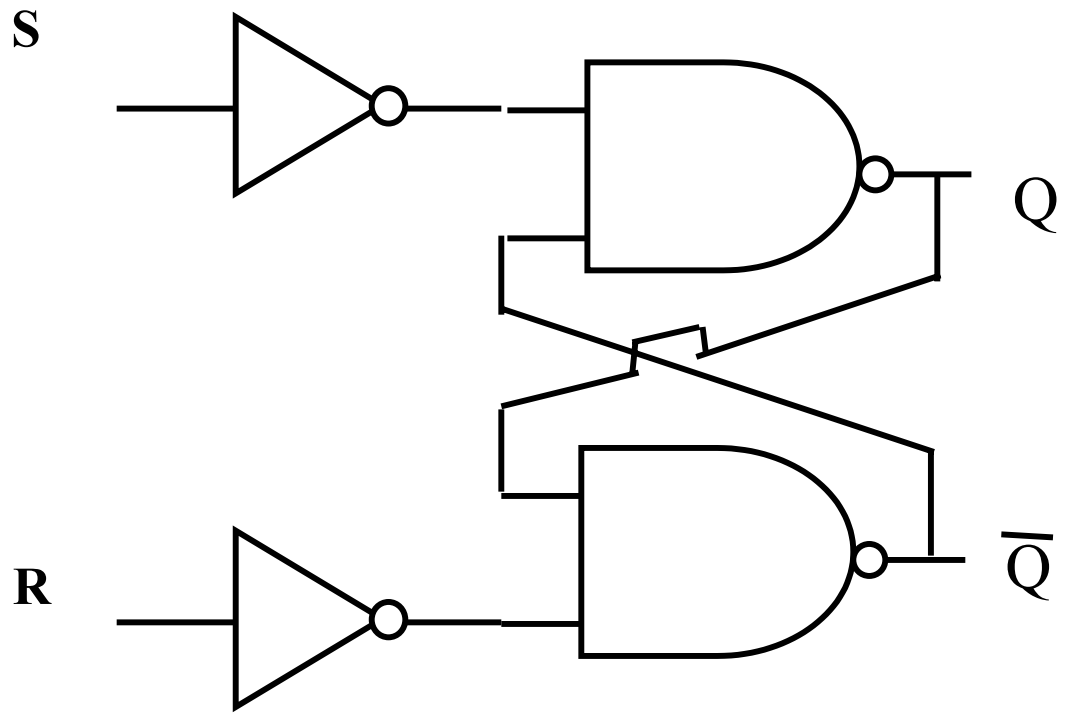
# Feedback Can Provide Memory



# Example of the Opposite State

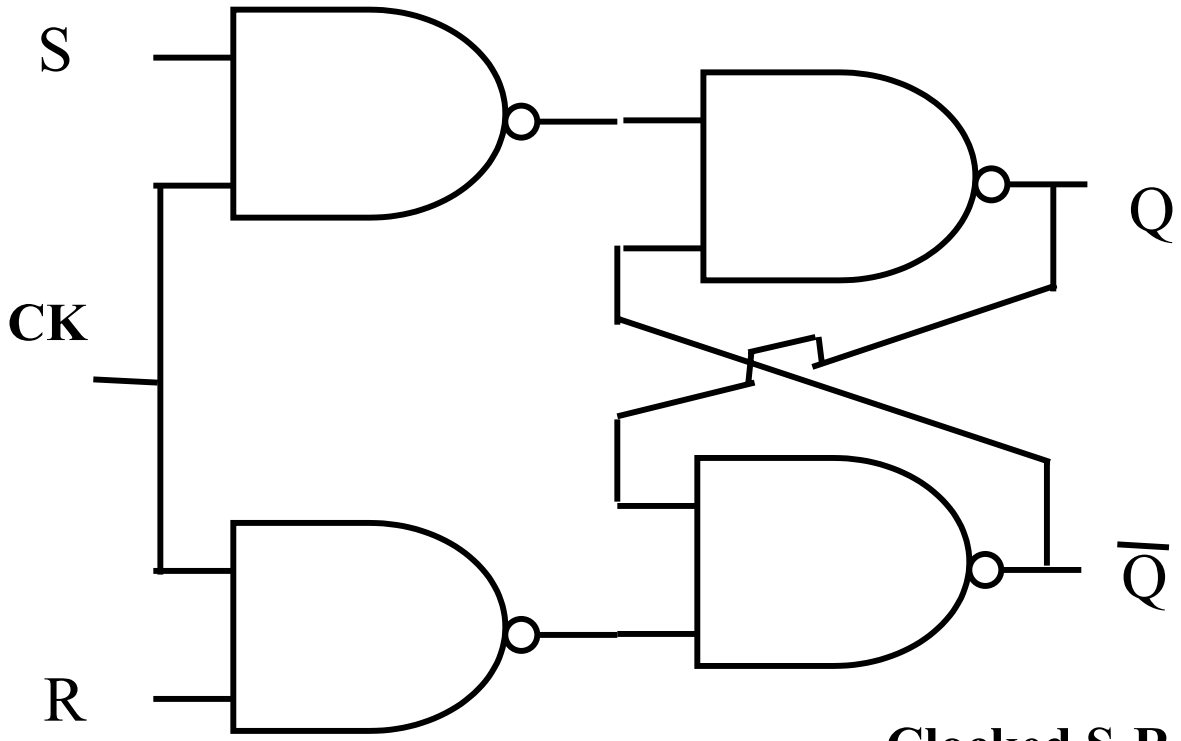


# Adding Memory Controls




**Set-Reset Flip-Flop**

# Adding a Clock




**Clocked S-R Flip-Flop**

# Switched Equivalent Resistance Values

**The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.**

**n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.**

**The resistance is inversely proportion to the gate width/length in the geometrical layout.**

**Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.**

**The current per unit width of the gate increases nearly inversely with the linewidth.**

# CMOS Device Parameters at 0.25μm

**Gate length is 0.25 μm = 250 nm**

**$V_{DD}$ = 2.5V**

**A minimum sized device has W =0.5 μm and L = 0.25 μm so W/L=2**

$$k = k' \frac{(W/L)}{(W/L)_{\min}}$$

| | $V_T$(V) | $V_{OUT\text{-}SAT}$ (V) | k' (μA/V$^2$) |
|---|---|---|---|
| NMOS | 0.43 | 0.63 | 115 |
| PMOS | 0.4 | 1 | 30 |

$$I_{OUT-SAT-D} = (115\mu A/V^2)(\frac{2}{2})(2.5V - 0.43V)(0.63V) = 150\mu A$$