Lecture 23

P-MOS Device and CMOS Inverters

A) P-MOS Device Structure and Operation

B) Relation of Current to t_{OX}, μ V_{LIMIT}

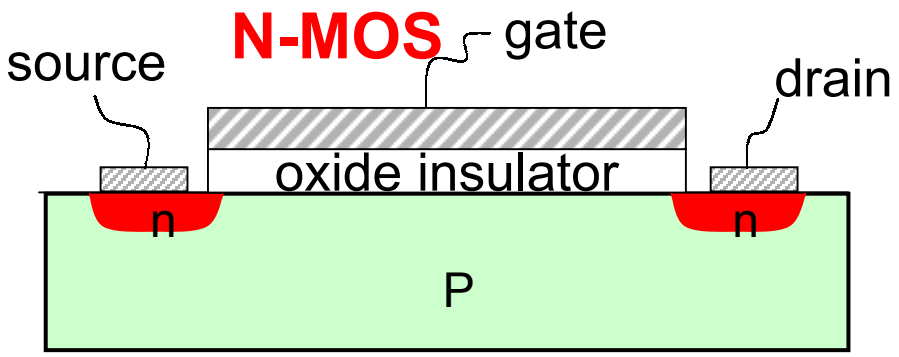
C) CMOS Device Equations and Use

D) CMOS Inverter V_{OUT} vs. V_{IN}

E) CMOS Short Circuit Current

Reading: Schwarz and Oldham, pp. 518-526

CMOS = Complementary MOS (PMOS is a second Flavor)



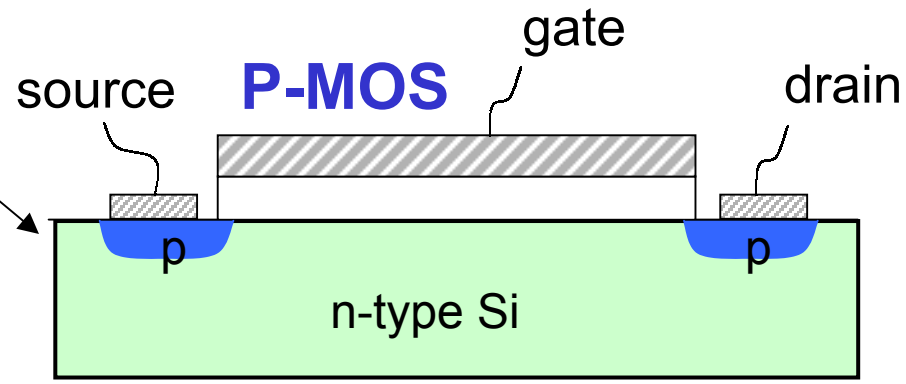
In this device the gate controls electron flow from source to drain.

It is made in p-type silicon.

The NEW FLAVOR! P-MOS

In this device the gate controls hole flow from source to drain.

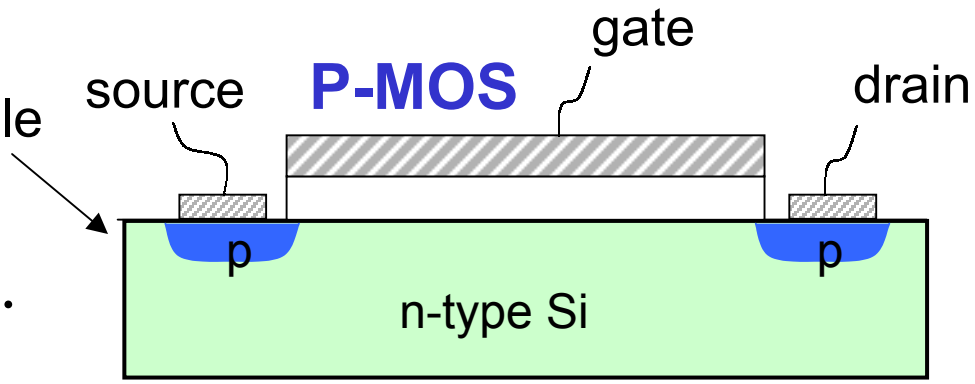
It is made in n-type silicon.

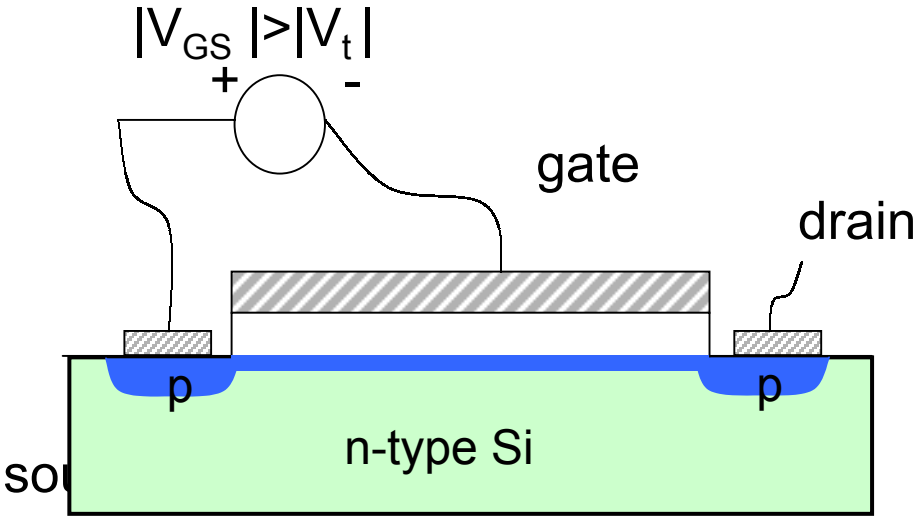


PMOS

In this device the gate controls hole flow from source to drain.

It is made in n-type silicon.





What if we apply a big negative voltage on the gate?

If $|V_{GS}|>|V_t|$ (both negative)

then we induce a + charge on the surface (holes)

NMOS and PMOS Compared

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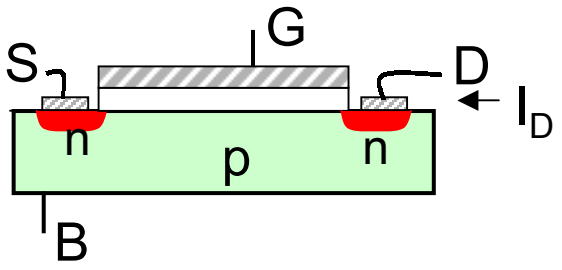
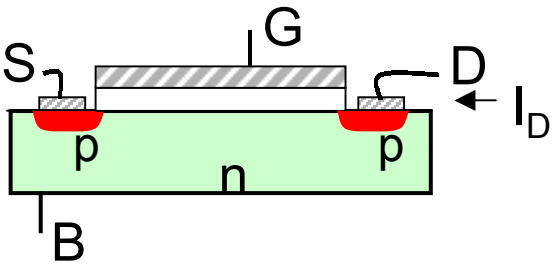
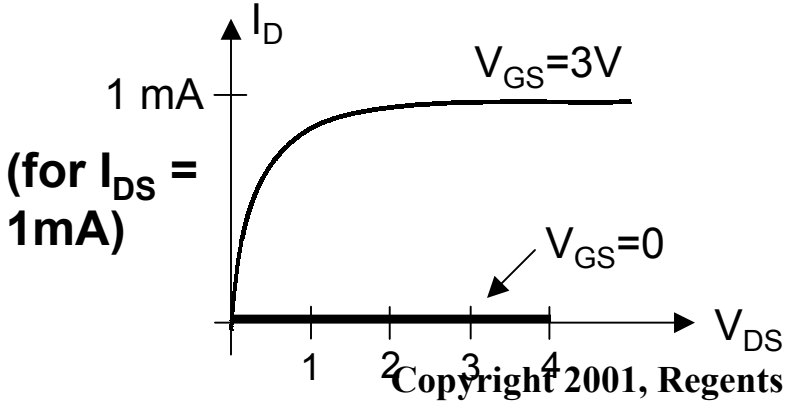
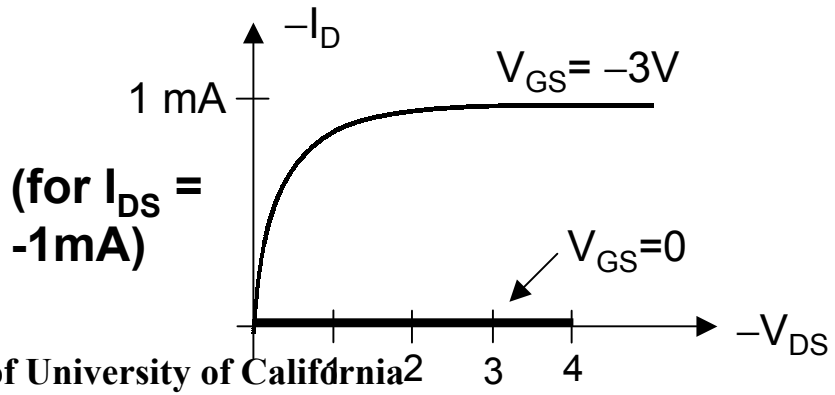
NMOS			PMOS		
"Body"	–	p-type	"Body"	–	n-type
Source	–	n-type	Source	–	p-type
Drain	–	n-type	Drain	–	p-type
V_{GS}	–	positive	V_{GS}	–	negative
V_T	–	positive	V_T	–	negative
V_{DS}	–	positive	V_{DS}	–	negative
I_D	–	positive (into drain)	I_D	–	negative (into drain)









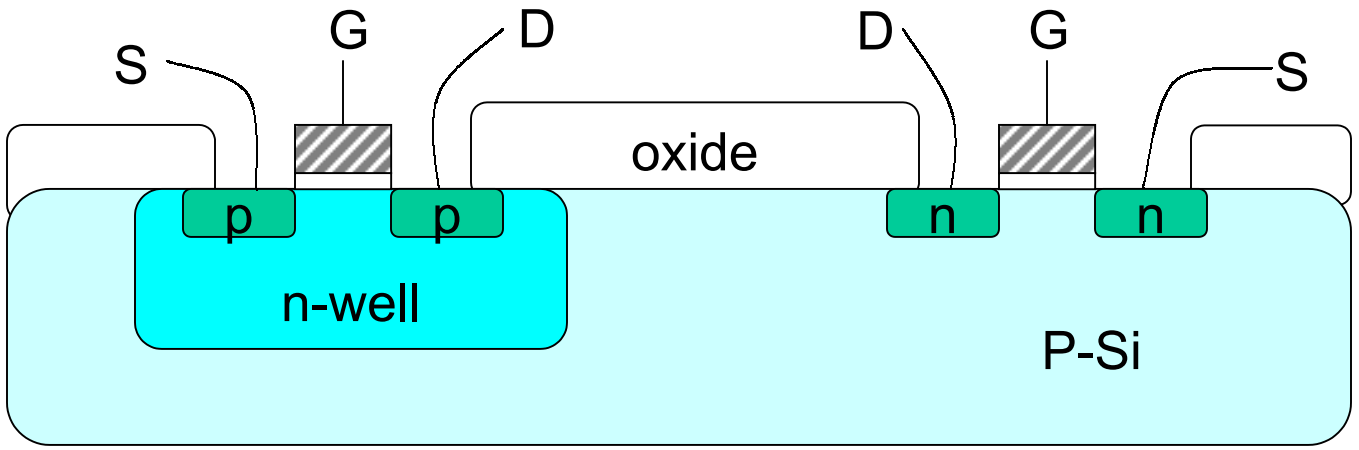
CMOS

Challenge: build both NMOS and PMOS on a single silicon chip

NMOS needs a p-type substrate

PMOS needs an n-type substrate

Requires extra process steps

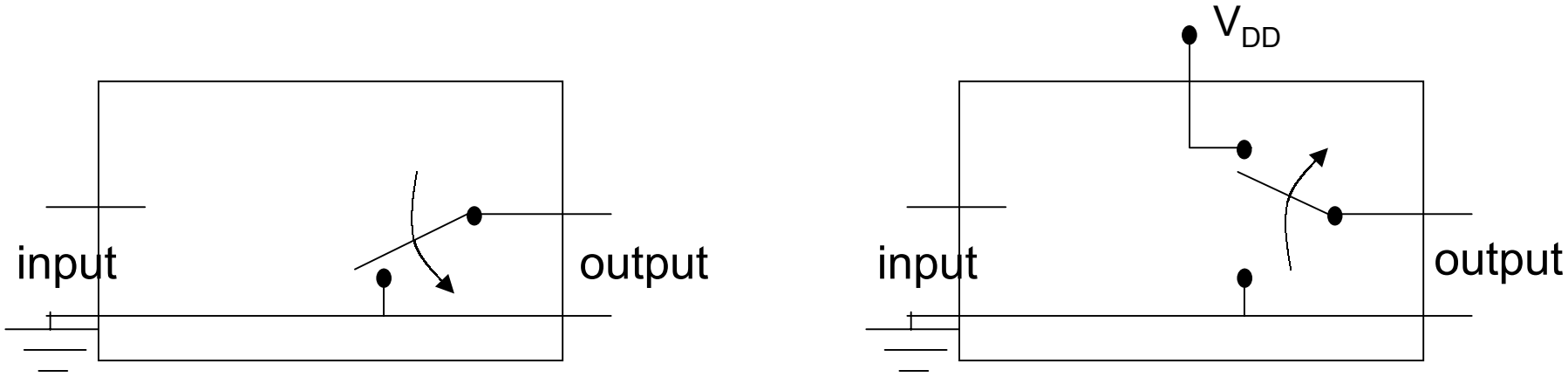


Why do we want PMOS?

We already have the ideal switch to connect any node to ground.

An NMOS transistor with gate held high has a very low resistance and essentially switches a node to ground (logic low).

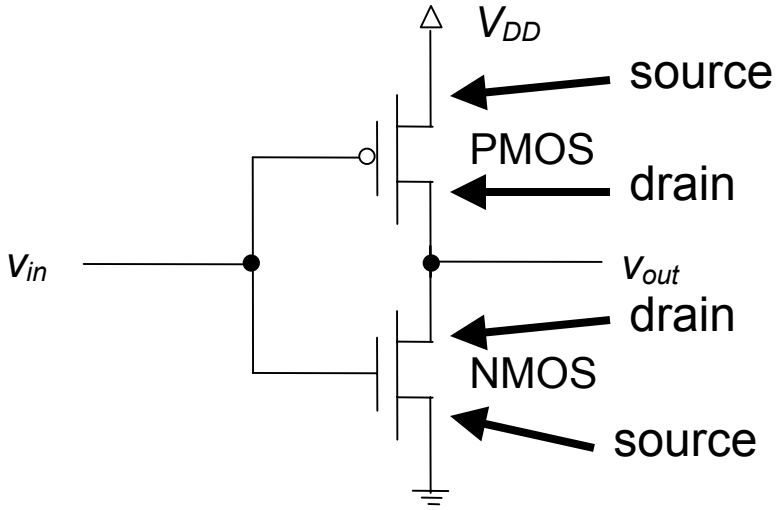
We also need a switch to switch nodes to whatever voltage is chosen as logic high (typically V_{DD}).



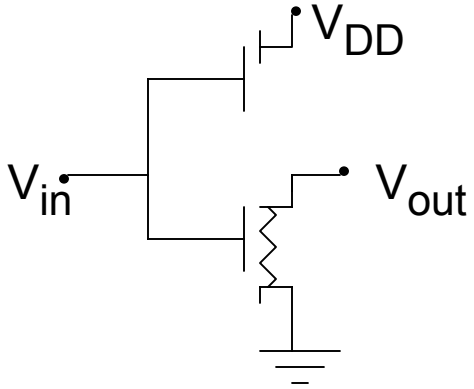
• A PMOS transistor is just the ticket. It is precisely as ideal a switch for connections to high as NMOS transistors are for connections to low.

• What's cool is that there is little more to learn about PMOS. These devices are essentially the same as NMOS except *all signs on V and I are reversed.*

THE BASIC STATIC CMOS INVERTER

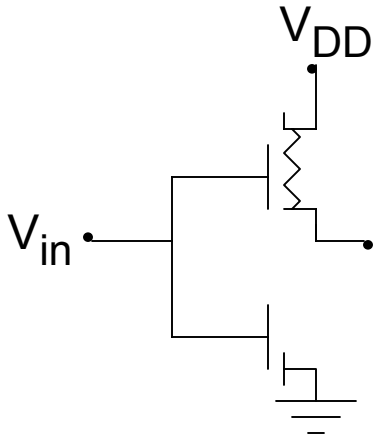


For V_{in} > 1.5V NMOS on , PMOS off



V_{out} **= 0**

For V_{in} < 1V NMOS off , PMOS on



$V_{out} = V_{DD}$

Example for Discussion:

NMOS: V_{Tn} = 1V

PMOS: V_{Tp} = -1V

Let V_{DD} = 2.5V

MOS Current Levels

The current values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The current proportion to the gate width/length in the geometrical layout.

Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

The current per unit width of the gate increases nearly inversely with the linewidth.

Relation of Current to Physical Parameters

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_T) \cdot V_{OUT-SAT-n}$$

Mobility of carriers

Oxide thickness

Geometrical Layout

Excess Gate drive

Voltage of scattering velocity limit

$$\mu_n = 500\left(cm^2/Vs\right) \qquad \mu_p = 150\left(cm^2/Vs\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\left(8.85x10^{-14}\,F/cm\right)(3.9)}{6x10^{-7}\,cm} = 5.75x10^{-7}\,F/cm^2$$

$$V_{OUT-SAT-n} = E_{Crit} \cdot L = 10^4\left(V/cm\right) \cdot 0.25x10^{-4}\,cm = 0.25V$$

CMOS Device Parameters at 0.25μm

Gate length is 0.25 μm = 250 nm

V_{DD} = 2.5V

	V_T(V)	$V_{OUT-SAT}$ (V)	k' (μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

These parameters are from re-fitting I vs. V data in Chapter 3 of the EECS 141 Text Book by Rabaey with saturation current model we are using in EE42.

Here $V_{IN} = V_{DD}$ is used to estimate the maximum I_{DS}

$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

$$I_{OUT-SAT-D} = \left(100\mu A/V^2\right)\left(\frac{0.375}{0.25}\right)(2.5V - 0.43V)(0.63V) = 196\mu A$$

Saturation Current 0.25 μm NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-n}$ where it reaches the saturation current

$$I_{OUT-SAT-n} = k_n' \left(\frac{W}{L}\right)_n \left(V_{IN} - V_{Tn}\right) V_{OUT-SAT-n}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:

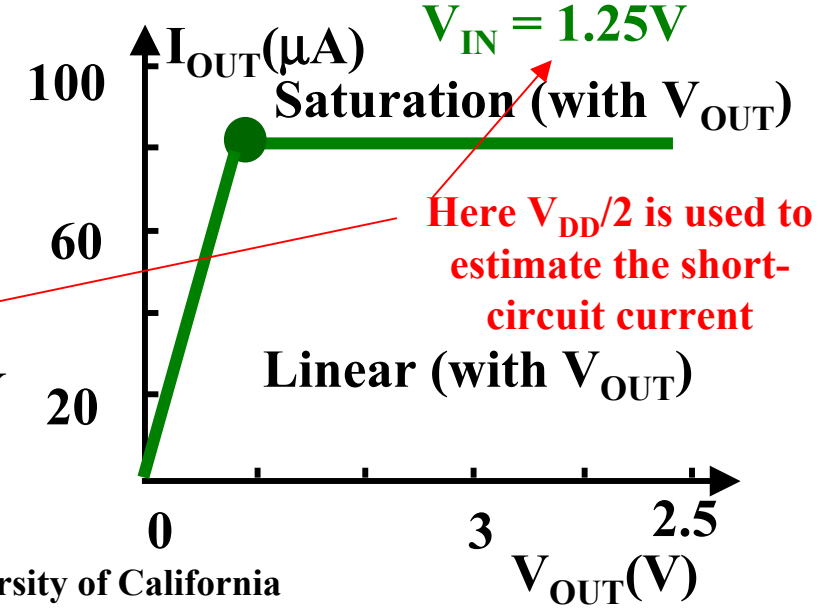
$k_n = 100\ \mu A/V^2$ **$W = 0.375\mu m$**

$V_{Tn} = 0.43V$ **$V_{DD} = 2.5V$**

$V_{OUT-SAT-n} = 0.63V$

$$I_n = 100\frac{\mu A}{V^2}\left(\frac{0.375}{0.25}\right)(1.25V - 0.4V)0.63V$$

$$= 77.5\mu A$$



Saturation Current 0.25 μm PMOS Model

Current I_{OUT} only flows when V_{IN} is smaller than V_{DD} minus the threshold value V_{TU} and the current is proportional to (V_{DD}-V_{OUT}) up to (V_{DD}-$V_{OUT-SAT-p}$) where it reaches the saturation current

$$I_{OUT-SAT-p} = k'_p \left(\frac{W}{L}\right)_p \left(V_{DD} - V_{IN} - |V_{Tp}|\right) V_{OUT-SAT-p}$$

Example:

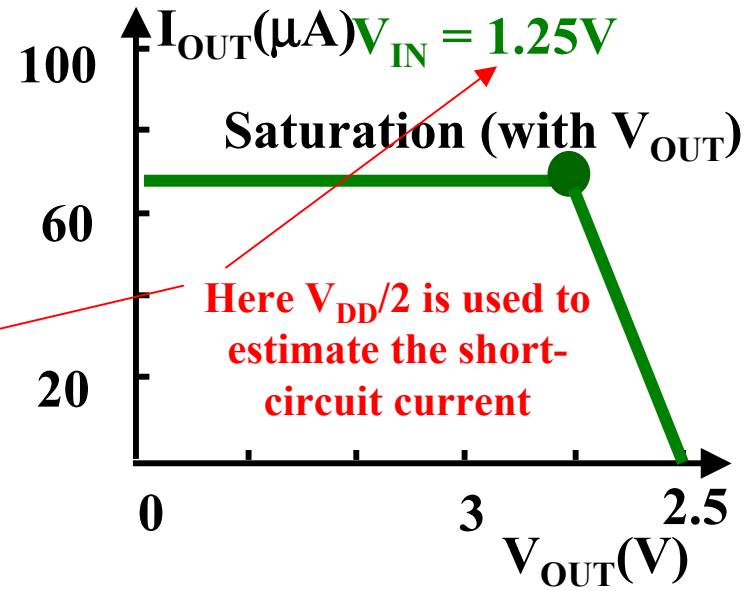
k'_p = 25 μA/V² **W = 0.75μm**

V_{Tp} = 0.4V **V_{DD} = 2.5V**

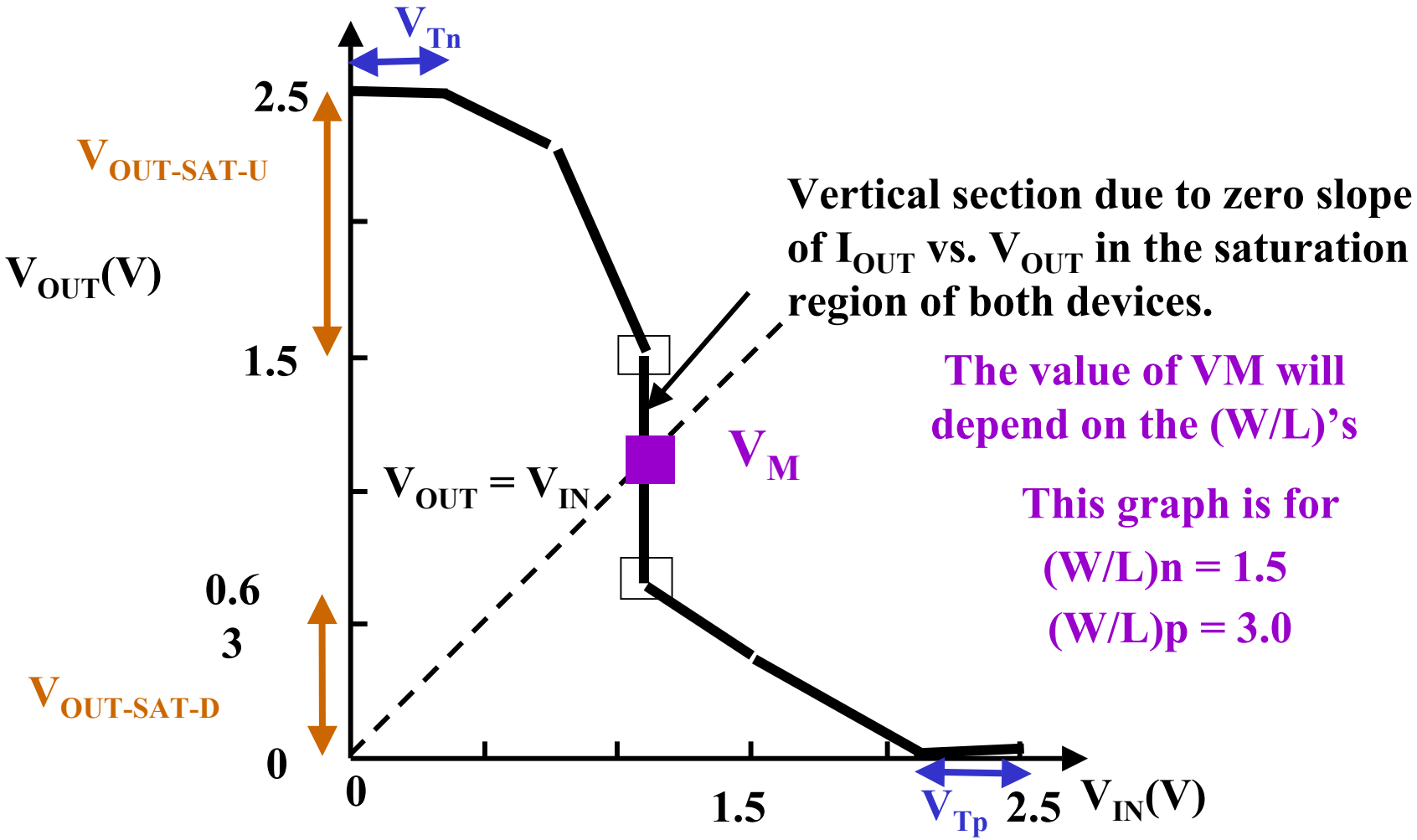
$V_{OUT-SAT-p}$= 1V

$$I_p = 25\frac{\mu A}{V^2}\left(\frac{0.75}{0.25}\right)(2.5V - 1.25V - 0.4V)1V$$

$$= 63.8\mu A$$



Voltage Transfer Function for the 0.25 μm CMOS Inverter



Vertical section due to zero slope of I_{OUT} vs. V_{OUT} in the saturation region of both devices.

The value of VM will depend on the (W/L)'s

This graph is for

(W/L)n = 1.5

(W/L)p = 3.0

Finding V_M for 0.25 μm Inverter

At V_M,

1) $V_{OUT} = V_{IN} = V_M$

2) **Both devices are in saturation**

3) $I_{OUT\text{-}SAT\text{-}n} = I_{OUT\text{-}SAT\text{-}p}$

Result will depend on (W/L) ratios.

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n (V_{IN} - V_{Tn})V_{OUT-SAT-n} =$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p (V_{DD} - V_{IN} - V_{Tp})V_{OUT-SAT-p}$$

Substitute V_M **Solve for V_M**

For $(W/L)_n = 1.5$ and $(W/L)_p = 3.0$ V_M is 1.17V

CMOS Short-Circuit Current

When V_{IN} is at an intermediate value both the NMOS and PMOS can conduct simultaneously.

If in addition V_{OUT} is at an intermediate value, both the NMOS and PMOS devices will have sizeable currents and only the difference between their currents will be flowing through the load.

Most of the current will simply flow from the power supply through both devices to ground as what is termed a 'short-circuit current.'

Example for the above inverter at the an instant $V_{IN} = 1.25V$ and $V_{OUT} = 1.25V$

$$I_p = 63.8\ \mu A \text{ and } I_n = 77.5\ \mu A$$

This means 63.8 μA flows directly to ground and only 13.7 μA flows out of the load and into the NMOS and on to ground.

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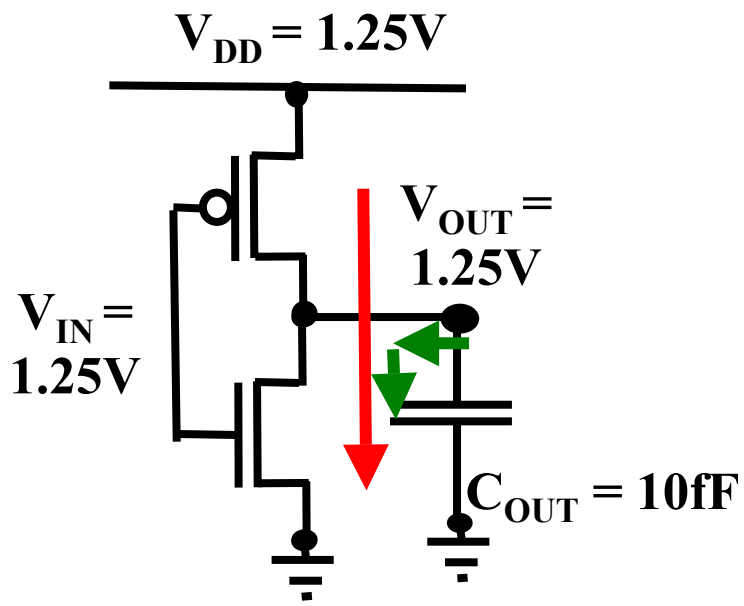
CMOS Inverter in Short-Circuit Condition

Assume the CMOS inverter from above with V_{IN} = 1.25V and V_{OUT} = 1.25V driving a 10 fF capacitor



What happens to the output signal?

The capacitor slowly discharges to try to find an output voltage that balances the NMOS and PMOS currents for the given value of V_{IN}.

$$\frac{\partial V}{\partial t} = \frac{I}{C} = \frac{13.7\mu A}{10\,fF} = 1.37(V/ns)$$

$I_{Short\text{-}Circuit}$ = 63.8 µA
(We used $V_{IN} = V_{DD}/2$)

$I_{Discharge\_Load}$ = 13.7 µA
(We Used $V_{IN} = V_{DD}/2$)