Lecture 25

Integrated Circuit Layout and Fabrication

A) Assistance on HW #13

B) CMOS Layout

C) Process Flow

D) Device Structure Evolution in Process Flow

Reading: Schwarz and Oldham, pp. 527-532

Copyright 2001, Regents of University of California

CMOS Device Parameters at 0.25μm

Lecture 23

Gate length is 0.25 μm = 250 nm

V_{DD} = 2.5V

	V_T(V)	$V_{OUT-SAT}$ (V)	k' (μA/V^2)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

These parameters are from re-fitting I vs. V data in Chapter 3 of the EECS 141 Text Book by Rabaey with saturation current model we are using in EE42.

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

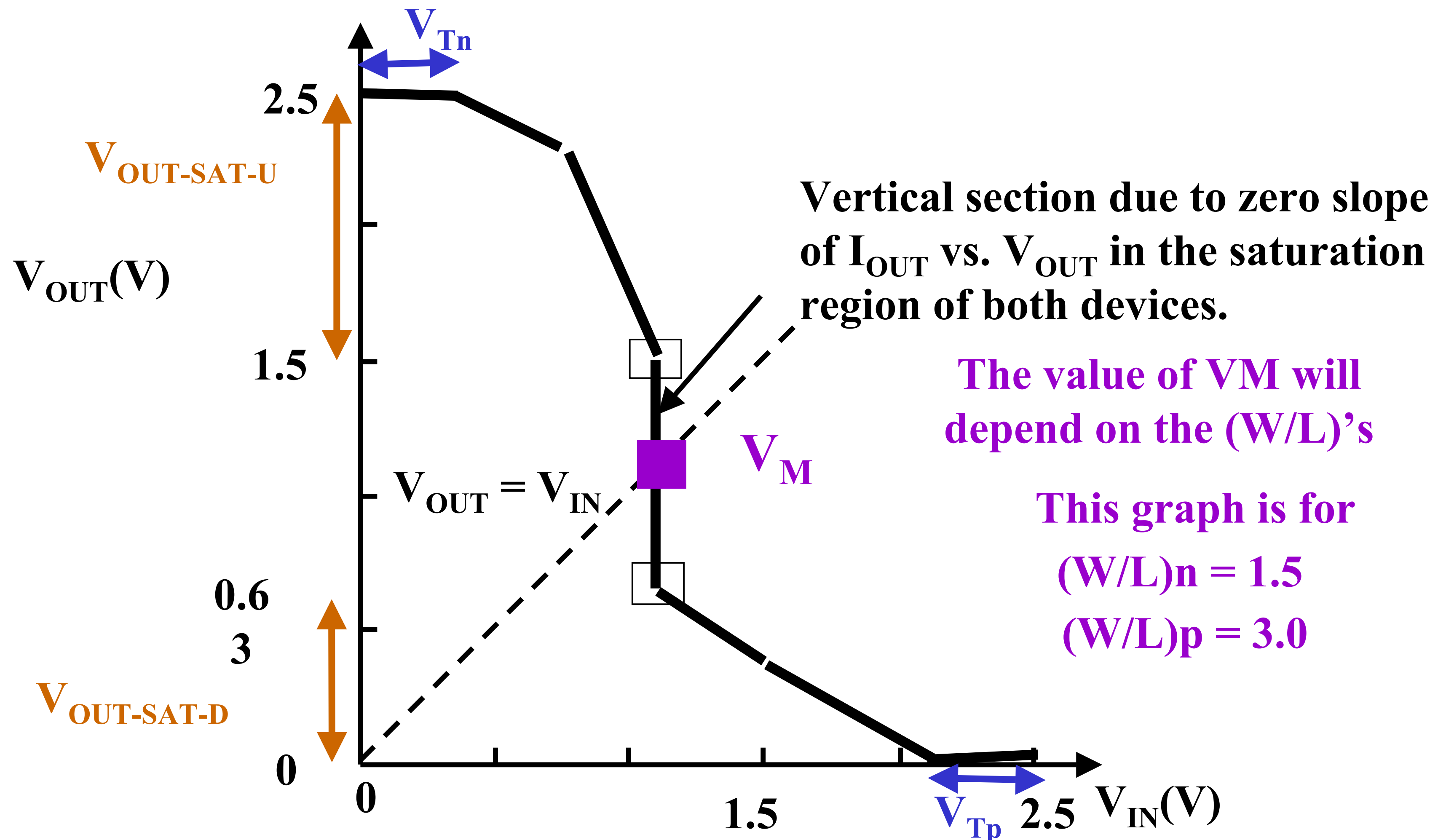
Here $V_{IN} = V_{DD}$ is used to estimate the maximum I_{DS}

$$I_{OUT-SAT-D} = (100\mu A/V^2)\left(\frac{0.375}{0.25}\right)(2.5V - 0.43V)(0.63V) = 196\mu A$$

Copyright 2001, Regents of University of California

Voltage Transfer Function for the 0.25 μm CMOS Inverter

Lecture 23



Copyright 2001, Regents of University of California

Lecture 23

Finding V_M for 0.25 μm Inverter

At V_M,

1) $V_{OUT} = V_{IN} = V_M$
2) Both devices are in saturation
3) $I_{OUT\text{-}SAT\text{-}n} = I_{OUT\text{-}SAT\text{-}p}$

Result will depend on (W/L) ratios.

$$I_{OUT-SAT-n} = k_n' \left(\frac{W}{L}\right)_n (V_{IN} - V_{Tn}) V_{OUT-SAT-n} =$$

$$I_{OUT-SAT-p} = k_p' \left(\frac{W}{L}\right)_p (V_{DD} - V_{IN} - V_{Tp}) V_{OUT-SAT-p}$$

Substitute V_M Solve for V_M

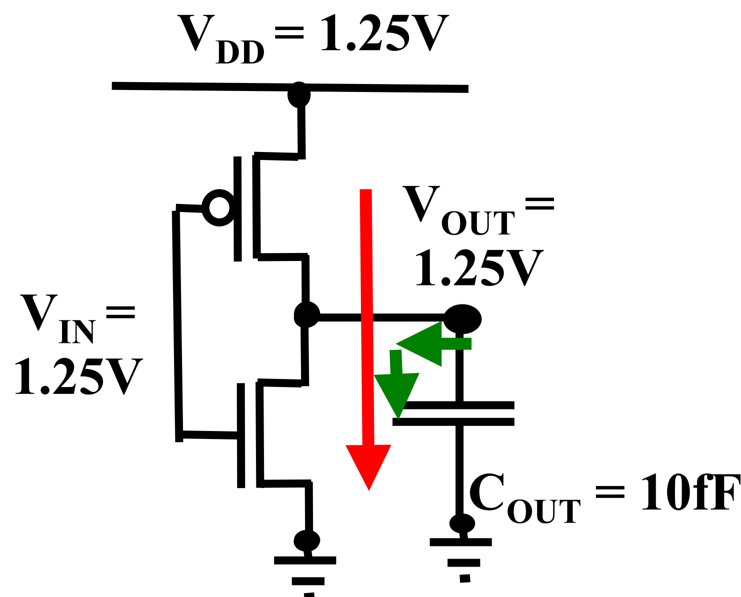
For $(W/L)_n = 1.5$ and $(W/L)_p = 3.0$ V_M is 1.17V

Copyright 2001, Regents of University of California

Lecture 23

CMOS Inverter in Short-Circuit Condition

Assume the CMOS inverter from above with
V_{IN} = 1.25V and V_{OUT} = 1.25V driving a 10 fF capacitor



$I_{Short-Circuit}$ = 63.8 μA
(We used $V_{IN} = V_{DD}/2$)

$I_{Discharge_Load}$ = 13.7 μA
(We Used $V_{IN} = V_{DD}/2$)

What happens to the output signal?

The capacitor slowly discharges to try to find an output voltage that balances the NMOS and PMOS currents for the given value of V_{IN}.

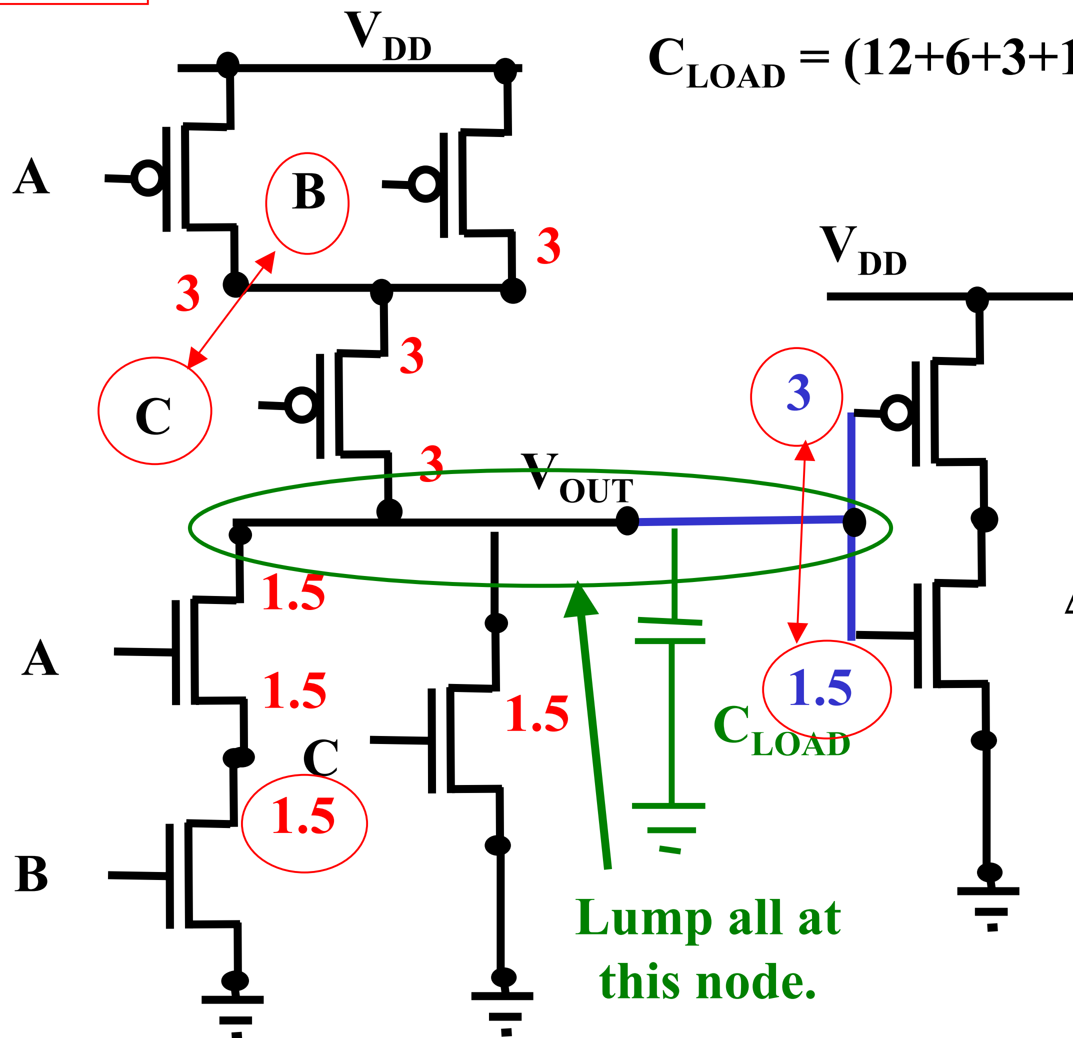
$$\frac{\partial V}{\partial t} = \frac{I}{C} = \frac{13.7\mu A}{10\,fF} = 1.37(V/ns)$$

Copyright 2001, Regents of University of California

Study this page carefully as three starting point mistakes were corrected.

Lecture 24

Example CMOS Circuit



$C_{LOAD} = (12+6+3+1.5)(0.4fF) = 9$ fF

Worst case is a=1, c =0, and b changes 1 => 0

$R = 2R_{DP} = 24k\Omega$

$\Delta t = 0.69(24k\Omega)(9\text{ fF}) = 149$ ps

For comparison the inverter had a pull-up delay of 30 ps

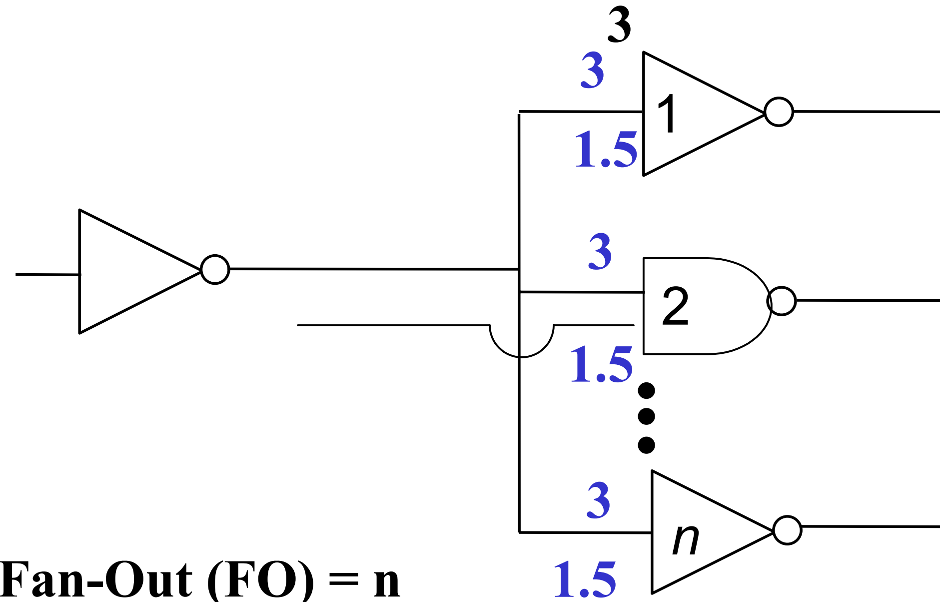
Copyright 2001, Regents of University of California

Lecture 24

Fanout

Fanout is always ≥ 1 (there is always a load)

Gate capacitances sum and are charged by the driver resistance



Fan-Out (FO) = n

One load device was in included in the initial estimate of C_{LOAD}.

$$C'_{LOAD} = C_{LOAD} + (FO - 1)((W/L)_p + (W/L)_n)(C_{G/MS})$$

$$C'_{LOAD} = C_{LOAD} + (FO - 1)(1.5+3.0)(0.4\ fF)$$

Assumes minimum length devices.

Copyright 2001, Regents of University of California

Lecture 24

Coping with Power Consumption

D.C. POWER

a.c. POWER

Tube: 300V x 20 mA = 6W

Bipolar Transistor: 5V x 20 mA = 200 mW

NMOS Transistor: 5V x 200 μA = 1 mW

CMOS Transistors: 5V x 100 nA = 0.5 μW

True of every gate!

$$P_{SHORT\text{-}CIRCUIT} = (1/2)\, I_{SHORT\text{-}CIRCUIT}\, V_{DD}\, \tau_{30\text{-}70}\, f_{CLOCK}$$

$$= (1/2)\,(60\ \mu A)\ 2.5V\ (0.1ns)\ (10^9) = 7.5\ \mu W$$

Assumes ½ of the gates change state

$$P_{DYNAMIC} = (1/2)(1/2)\, C\, V_{DD}^{\ 2}\, f_{CLOCK}$$

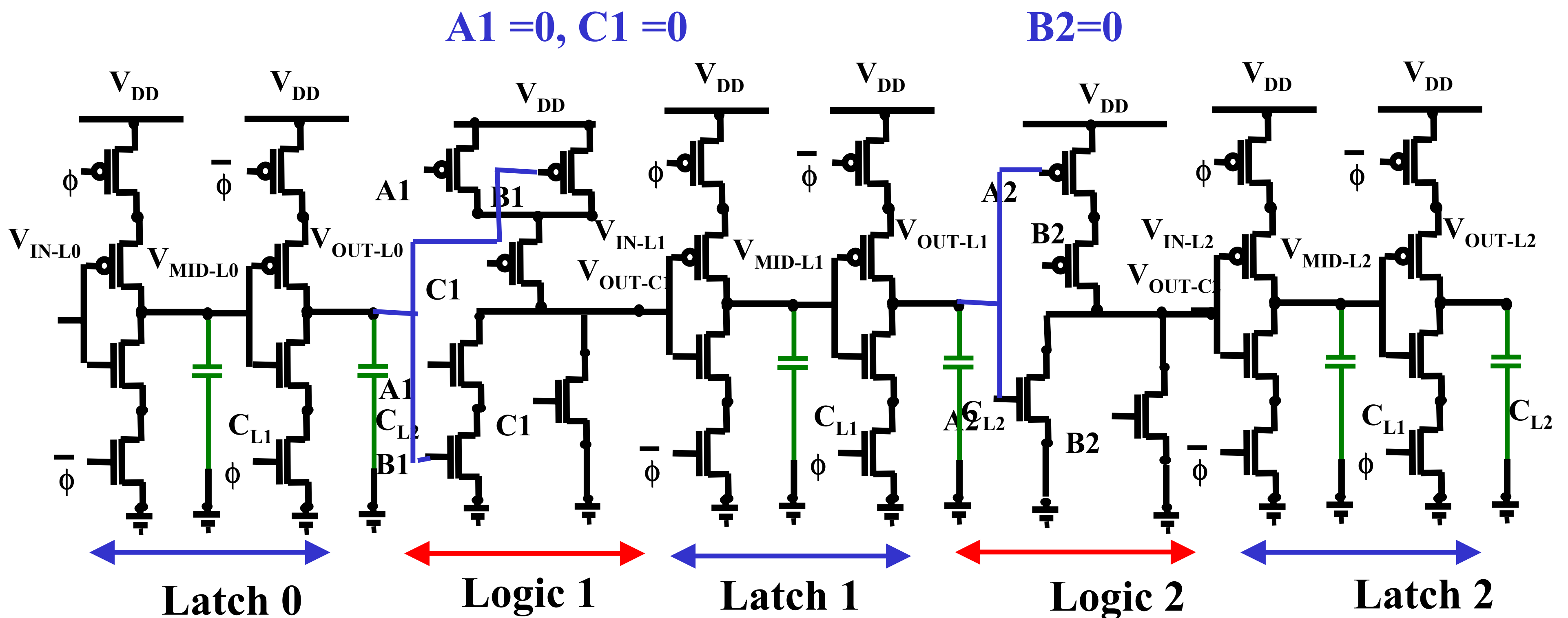
$$= (1/2)\,(1/2)(10\ fF)\,(2.5)^2\, 10^9 = 15.6\ \mu W$$

Only the L =>H takes energy from V_{DD}

True for only active gates.

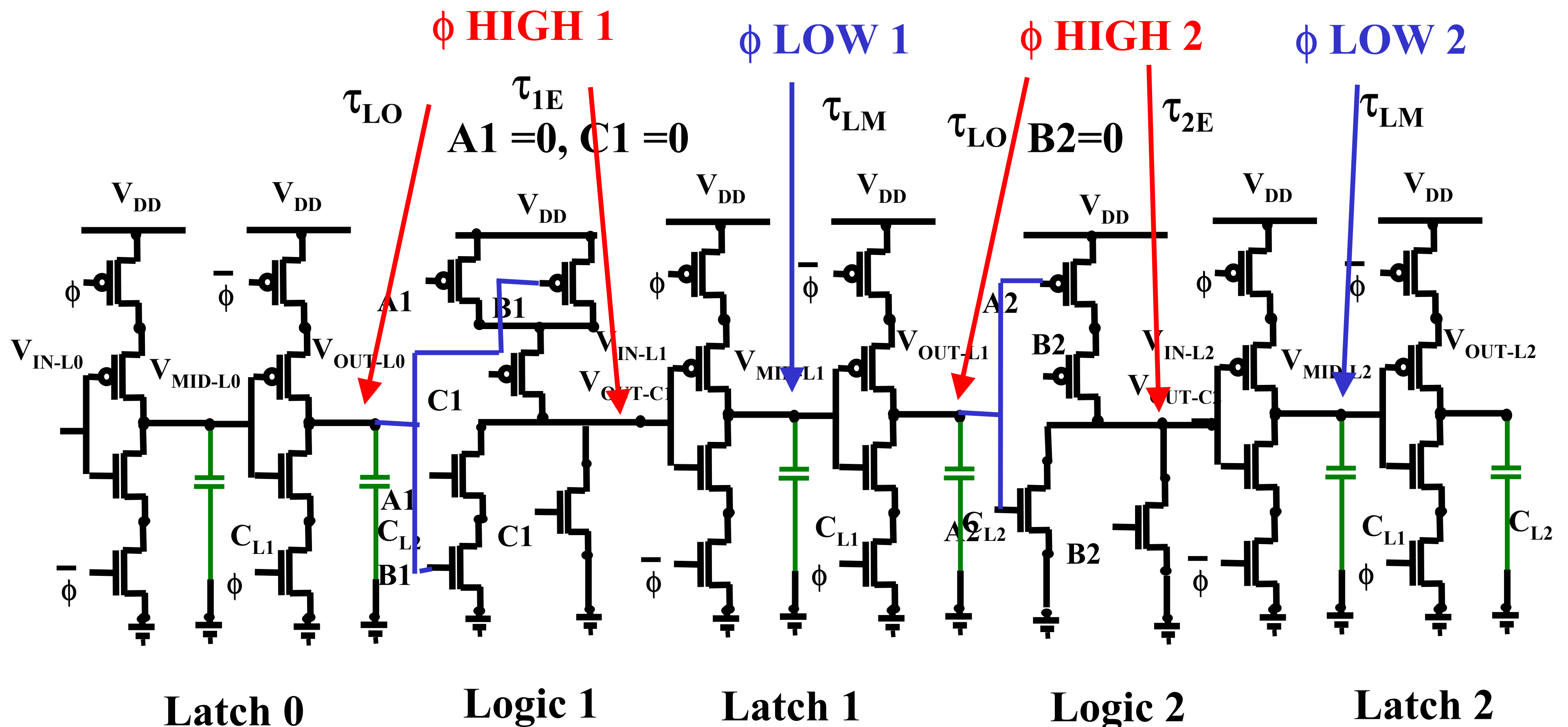
Copyright 2001, Regents of University of California

Combinatorial Logic and Clocked Latches: Wiring



Copyright 2001, Regents of University of California

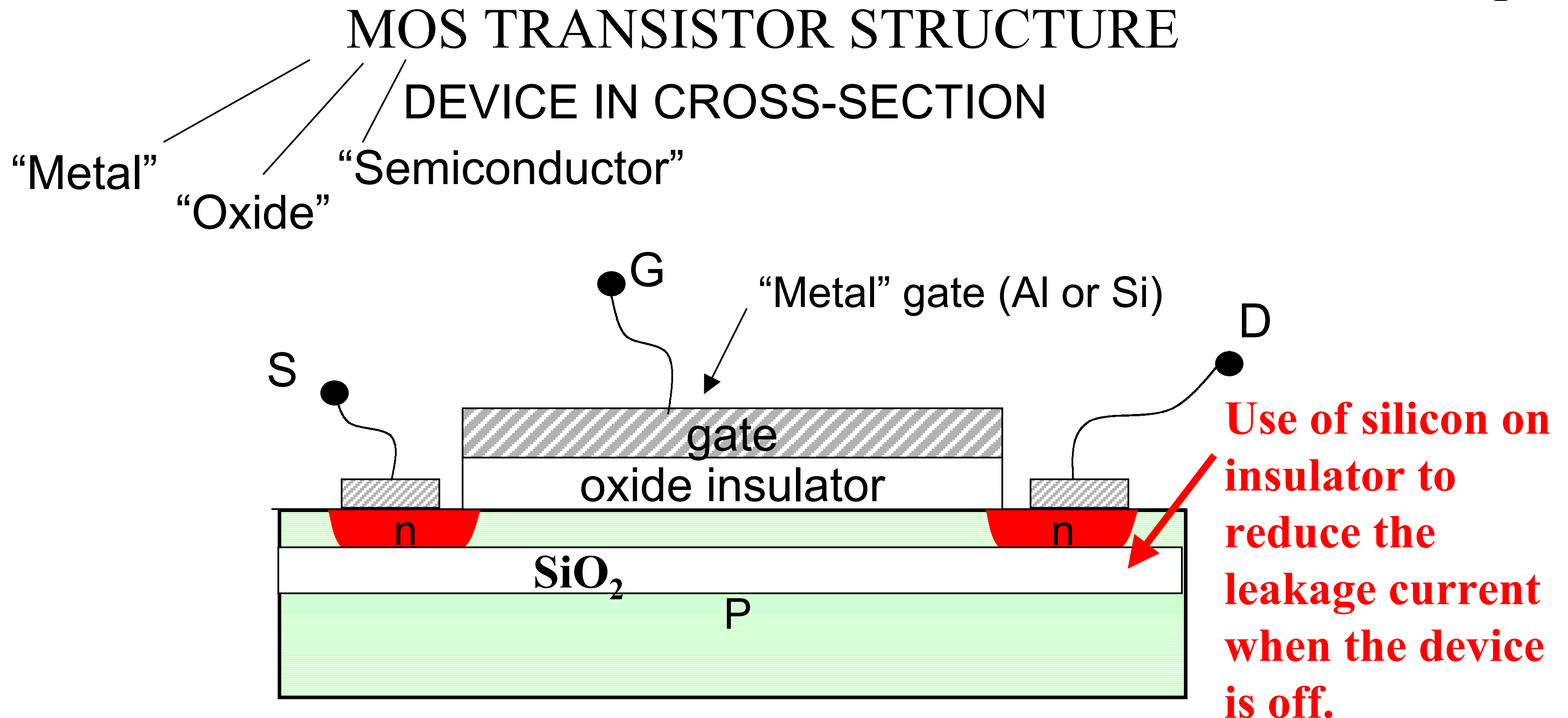
Combinatorial Logic and Clocked Latches: Signal Flow



$\tau_{\phi-HIGH} > \tau_{LO} + \text{Max}(\tau_{1E} \text{ or } \tau_{2E})$ $\tau_{\phi-LOW} > \tau_{LM}$ $f_{CLOCK} = 1/(\tau_{\phi-HIGH} + \tau_{\phi-LOW})$

Copyright 2001, Regents of University of California

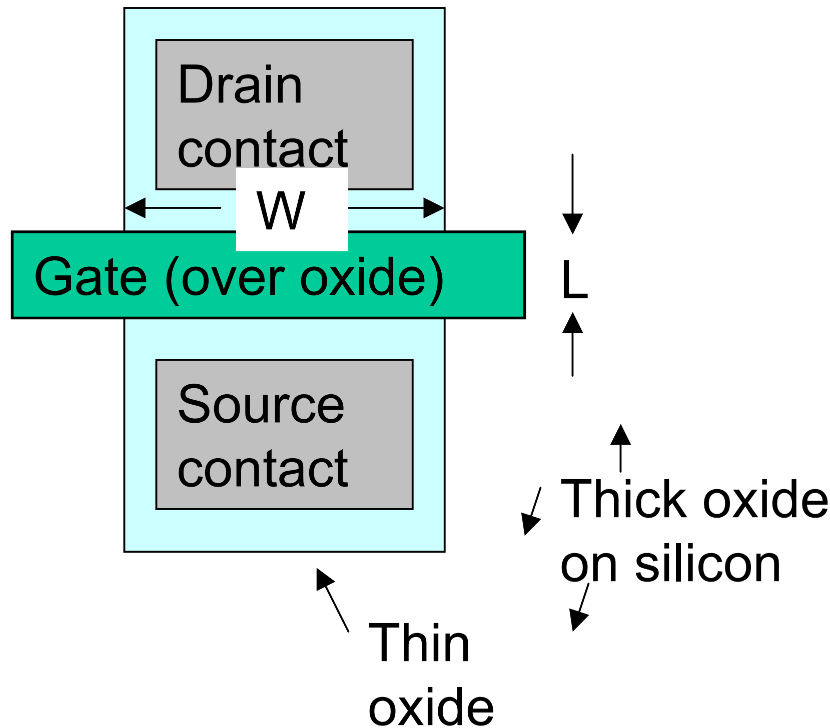
MOS TRANSISTOR STRUCTURE



- In the absence of gate voltage, no current can flow between S and D.
- Above a certain gate to source voltage V_t (the "threshold"), electrons are induced at the surface beneath the oxide. (Think of it as a capacitor.)
- These electrons can carry current between S and D if a voltage is applied.

Copyright 2001, Regents of University of California

MOS LAYOUT



What are device dimensions?

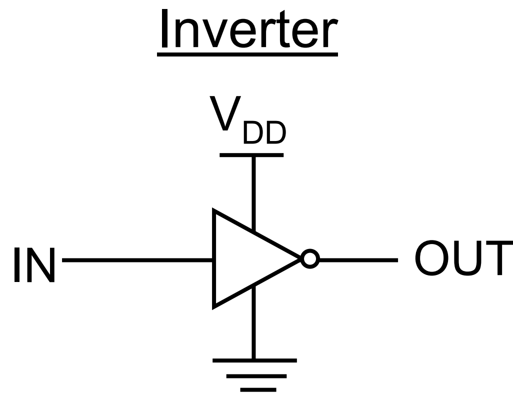
Gate Length = L

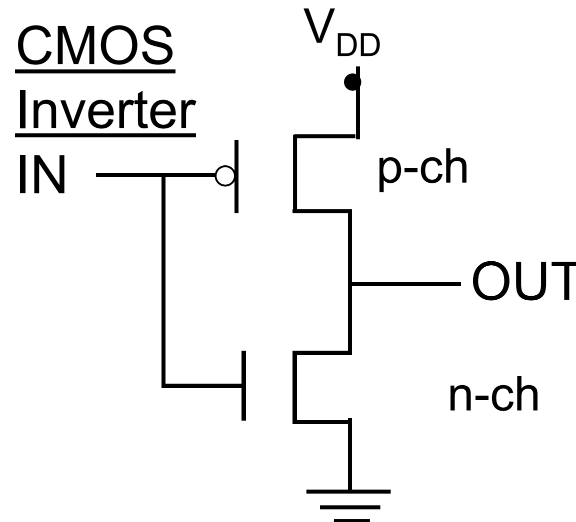
Gate Width = W

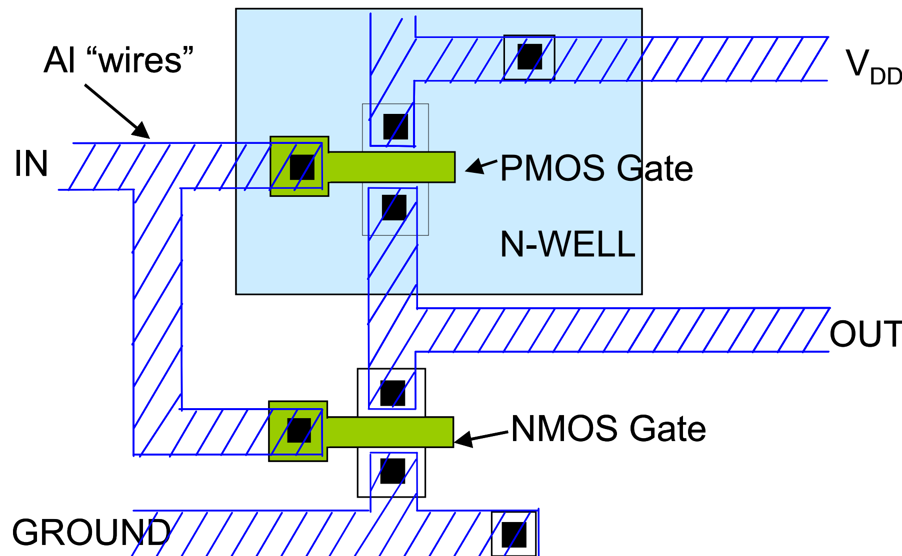
Gate Area (for capacitance) is W x L (because that is the thin oxide area covered by the gate)

Copyright 2001, Regents of University of California

Basic CMOS Inverter





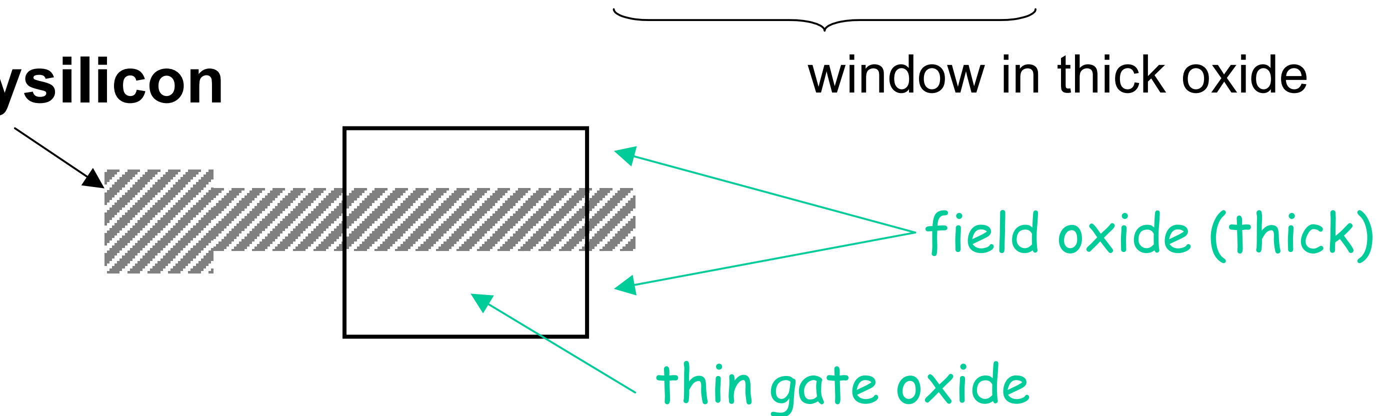


Example layout of CMOS Inverter

Copyright 2001, Regents of University of California

MOSFET "Identification"

Poly line crossing a thin oxide region → MOSFET

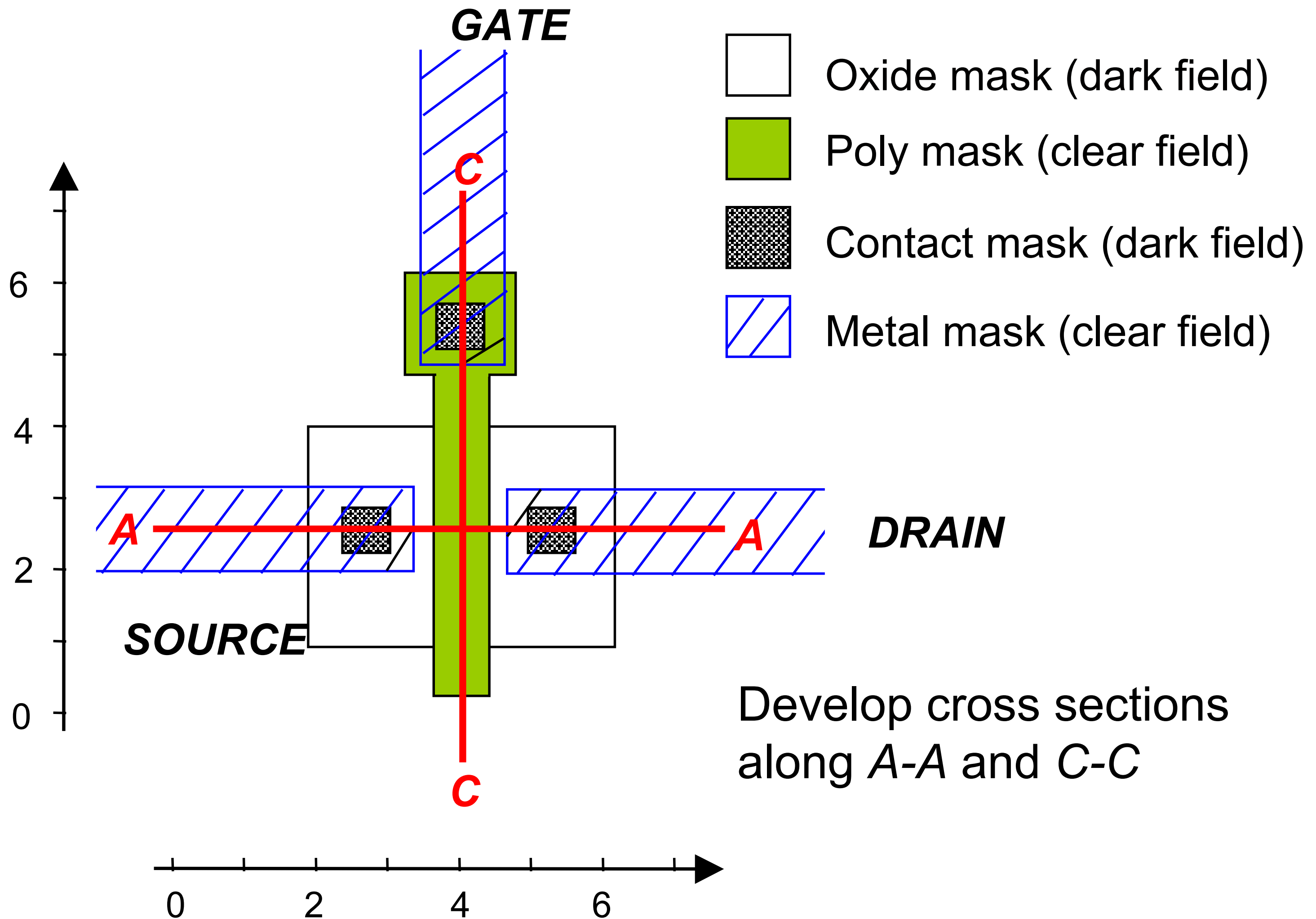


Is oxide region inside the n-well? If Yes, then PMOS; If No, then NMOS

Copyright 2001, Regents of University of California

NMOS Transistor Layout

("CAD View" = top view and 'Cut-Lines'))



Develop cross sections along *A-A* and *C-C*

Copyright 2001, Regents of University of California

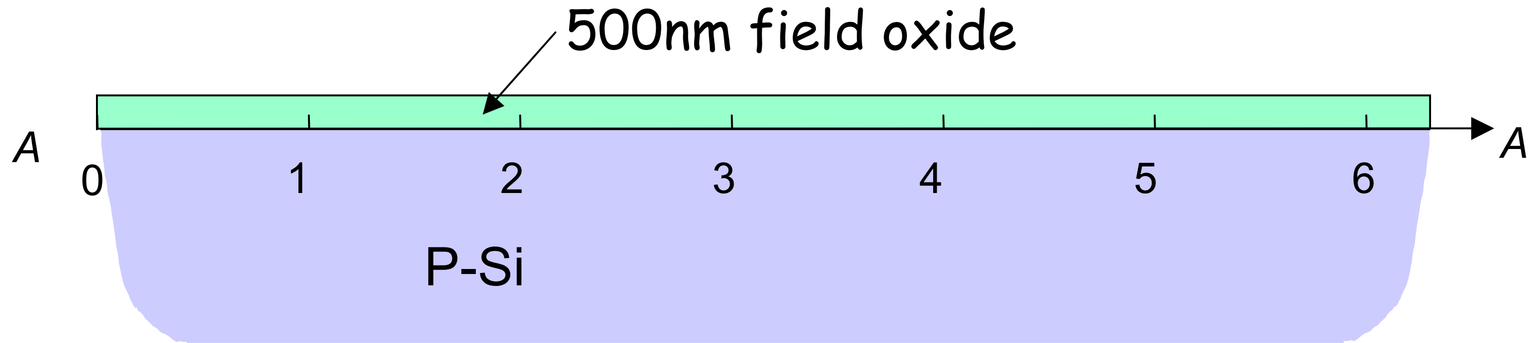
EXAMPLE NMOS Process Sequence

1. Starting material: p-type silicon. Grow 500 nm (5000 Å) of “field” SiO_2
2. Pattern oxide using the oxide mask
3. Grow 15 nm of “gate” SiO_2
4. Deposit 500 nm of n-type polysilicon
5. Pattern poly using the polysilicon mask
6. Implant arsenic (penetrates gate oxide, but not poly or field oxide) and anneal to form source and drain regions
7. Deposit 500 nm of SiO_2
8. Pattern oxide using contact mask (etch sufficiently long to clear oxide from all contact windows)
9. Deposit 1 μm of aluminum
10. Pattern aluminum with metal mask
11. Anneal at 450 °C to heal gate oxide damage and make good Si-Al contacts

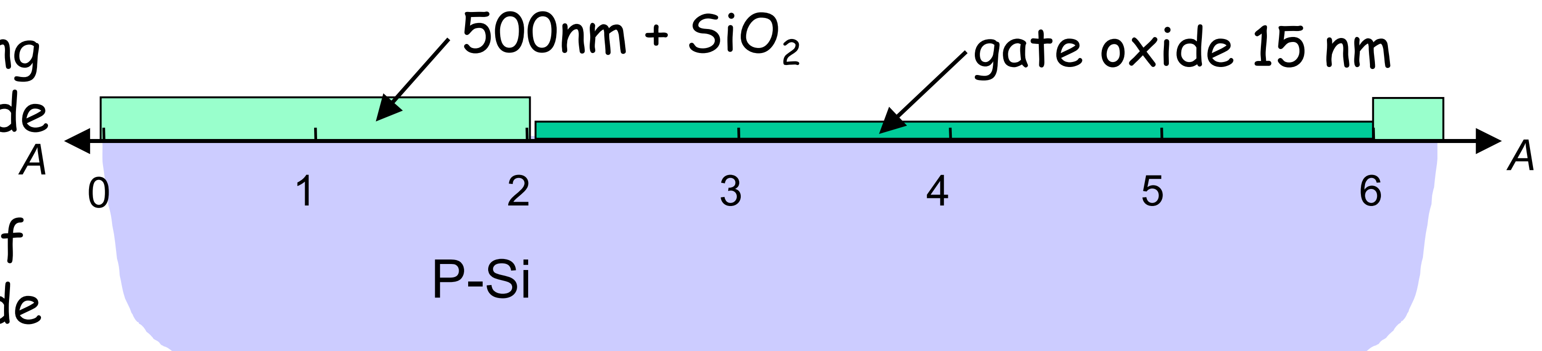
Copyright 2001, Regents of University of California

NMOS *A-A* Cross Sections

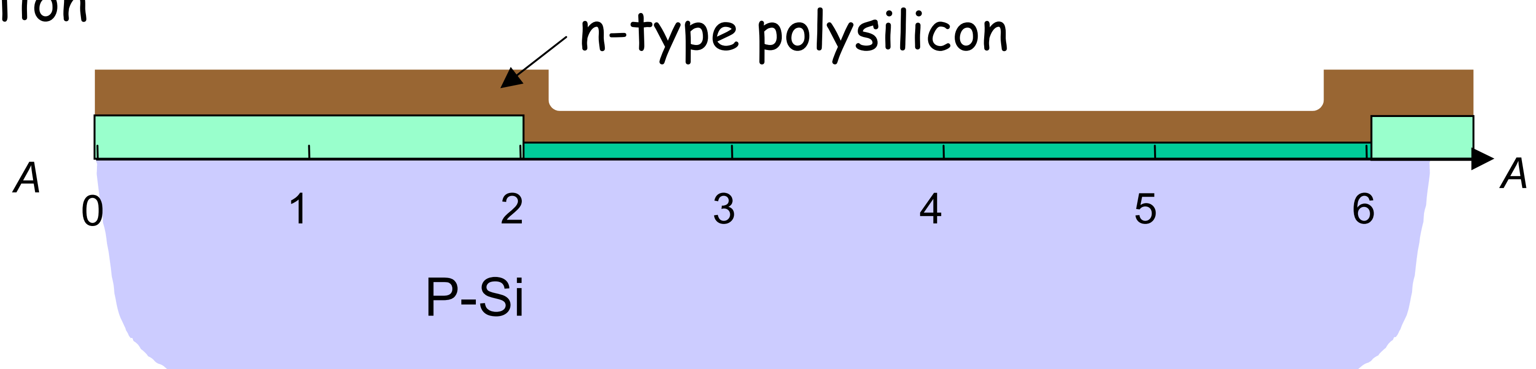
Version Date 12/01/01



After patterning field oxide and growth of gate oxide



After deposition of polysilicon

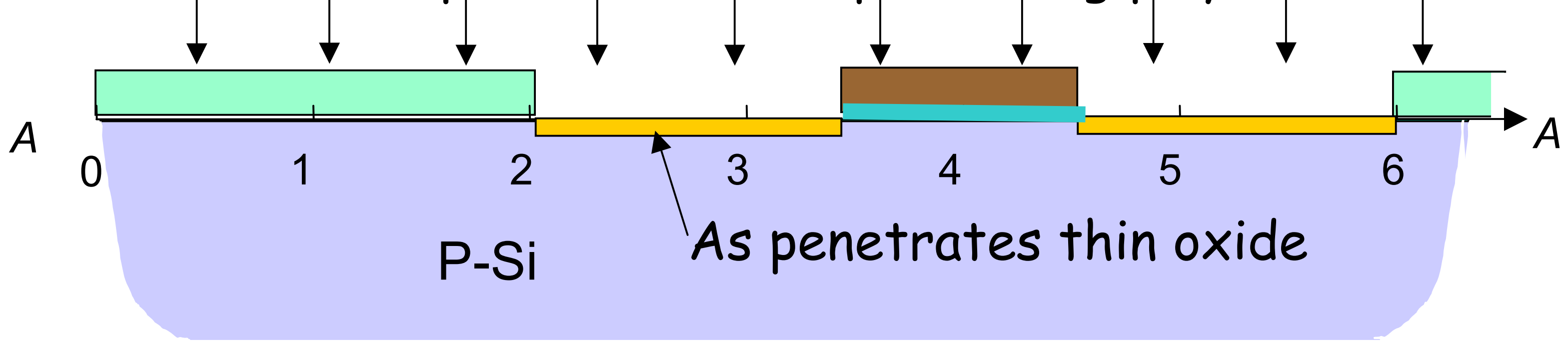


Copyright 2001, Regents of University of California

NMOS *A-A* Cross Sections

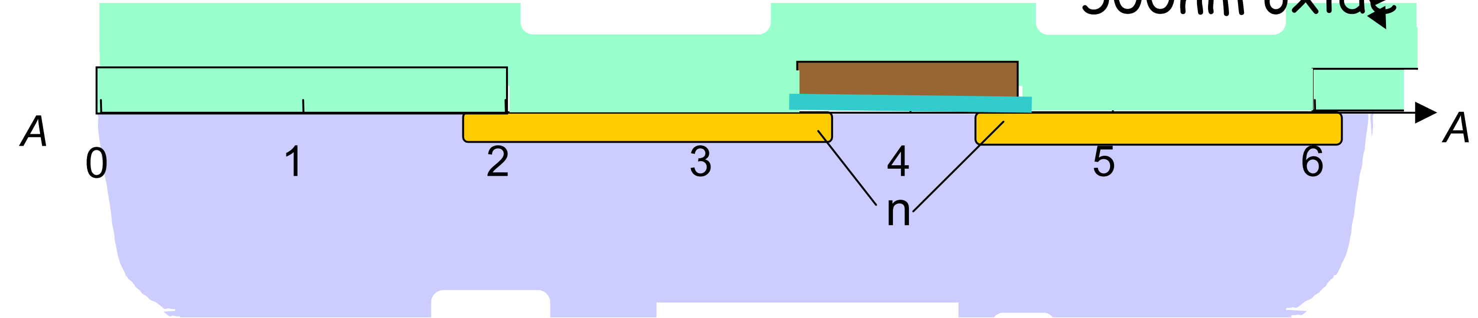
Arsenic ion implantation after patterning polysilicon

As doesn't penetrate through 500nm-thick SiO_2

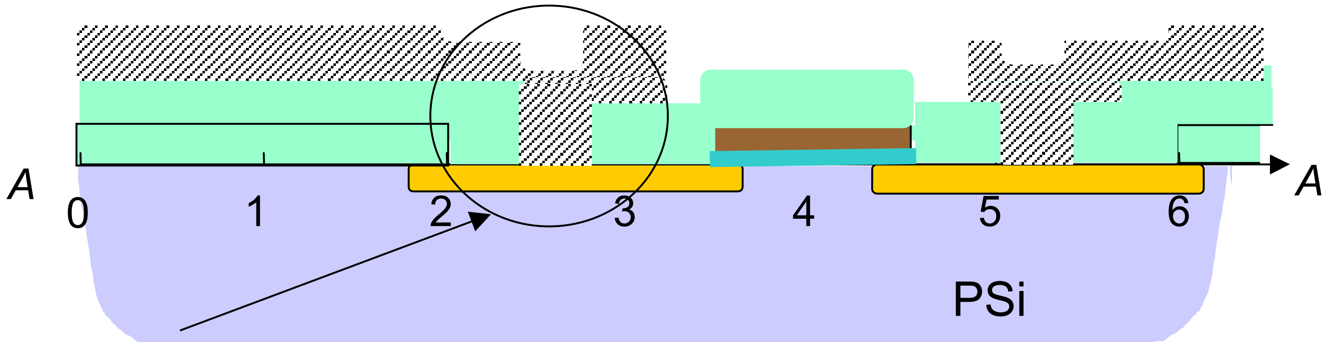


Deposited 500nm oxide

After annealing and oxide deposition

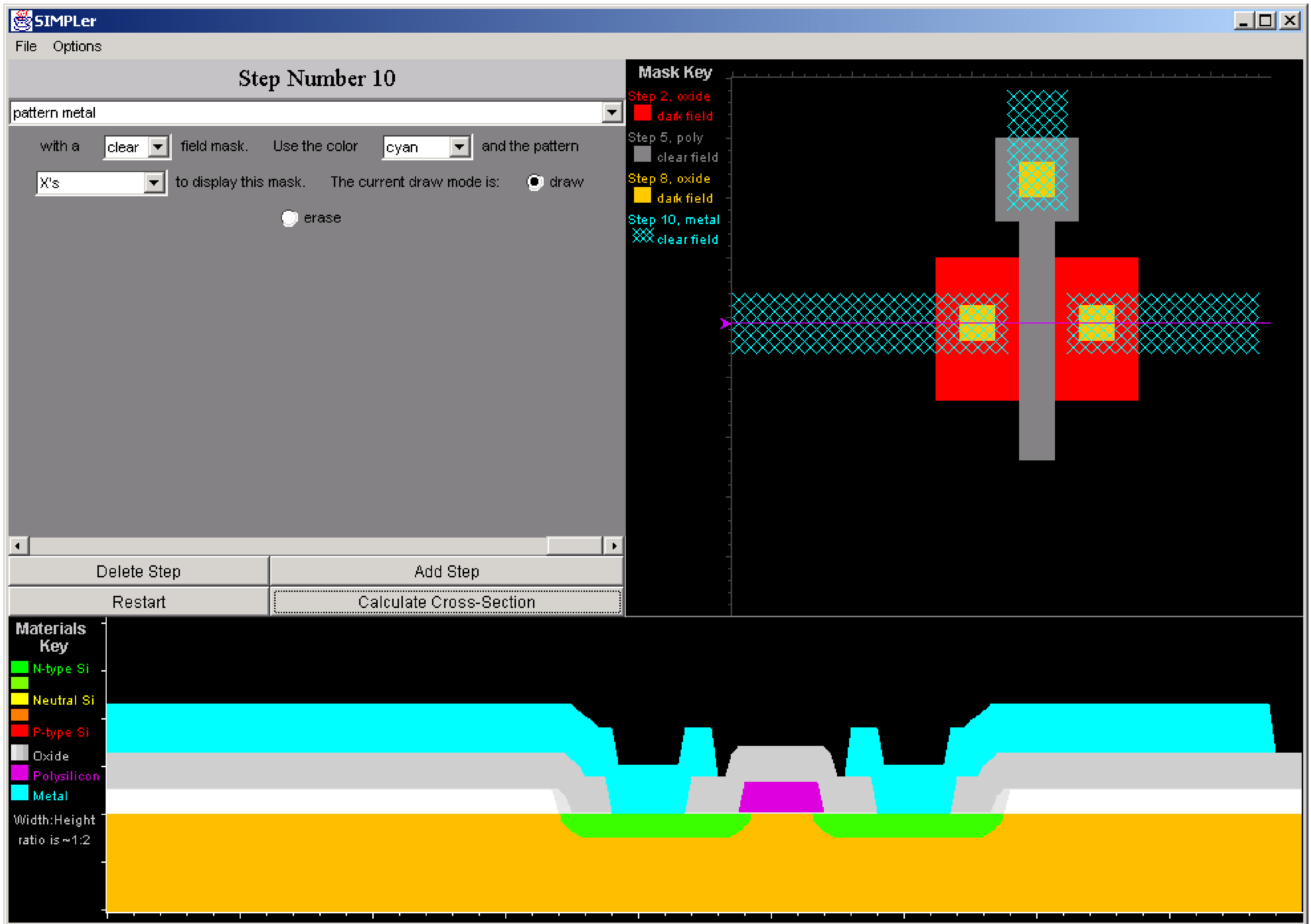


After contact and metal patterning and final anneal



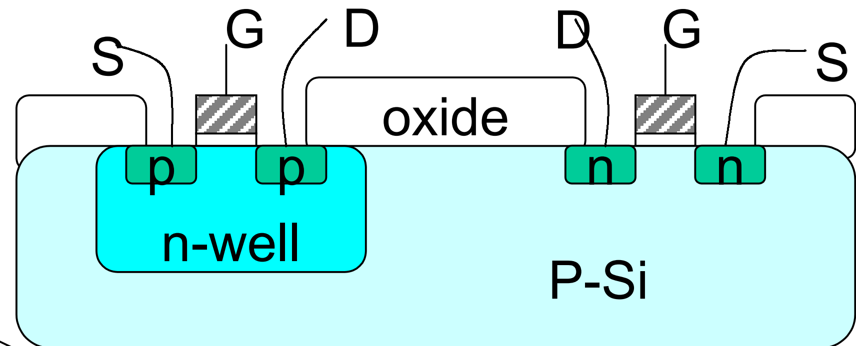
Note: Step 8 removes gate oxide from contacts to source and drain regions…otherwise, there's no current! (Al **must** touch n-type silicon!)

Copyright 2001, Regents of University of California



Copyright 2001, Regents of University of California

Conceptual CMOS Process



Start with p-type wafer

Create N-Well

Grow thick oxide

Remove it in transistor areas

Grow gate oxide

Grow and pattern polysilicon for gates

Dope n channel source and drains

Dope p-channel source and drains

Deposit oxide over gates

Pattern contacts

Deposit and Pattern Metal

NEW

Need to protect p-mos areas

Need to protect n-mos areas

It looks like we need three more masks than in NMOS

Copyright 2001, Regents of University of California