Lecture Review

Version Date 12/04/01

Review For Final

FINAL EXAM
12:30-3:30 Friday, December 14th, F0295 Haas
Closed Book, Device Equations Provided
Bring calculator, Paper Provided

Review Sessions:
Proposed 5-6:30 PM Mon Dec 10
Proposed 5-6:30 PM Wed Dec 12

Office hours:
Professor Neureuther: 11 M,Tu, W, Th, F but 10-11 on F Dec 14th
TA's: TBA on web

Congratulations Jason Gatt and Kevin Ha "Best in Show" in Tutbot/Calbot Contest

EE 42 Final Exam: Design Guidelines

- **Cover Material Since Midterm 2 at 2X compared to material on Midterms 1 and 2.**
  - **About 100 of 200 points on material since Midterm 2 and about 100 points on material prior to Midterm 2**
- **Change to an accomplishment basis instead of B- average standard normal distribution.**
  - **about 60 points of B level material**
  - **about 60 points of A level material**
  - **as a consequence exam average will be 120/200**
- **Results on 3 exams will be weighted by relative spread before merging to prevent large variation on final from wiping out Midterms.**

Key Material Since Midterm #2

- CMOS Static Type Analysis (big)
  - Current given voltage, V_{OUT} vs. V_{IN}, Short Circuit Current, D.C. power
- CMOS Transient Analysis (big)
  - Sources and amount of capacitance, propagation delay, a.c. power, clocked latches
- Diode and Bipolar Transistor (medium)
  - No physics but large signal analysis
- Physics (small)
  - Resistance from carrier motion, field effect carriers and resistance

About 100 pts with about

10-20 pts C, 20-30 pts B, and 40-50 pts A.

Key Material Before Midterm #2

- Equivalent Circuits and Load Lines
  - Simplify load circuits, find V_{OUT} vs. VIN
- Dependent Sources
  - Gain, input and output resistance
- Ideal Op-Amps
- Transients
- Gates
  - Logic function and timing diagrams

Total of about 100 Pts with about

50-60 pts C,

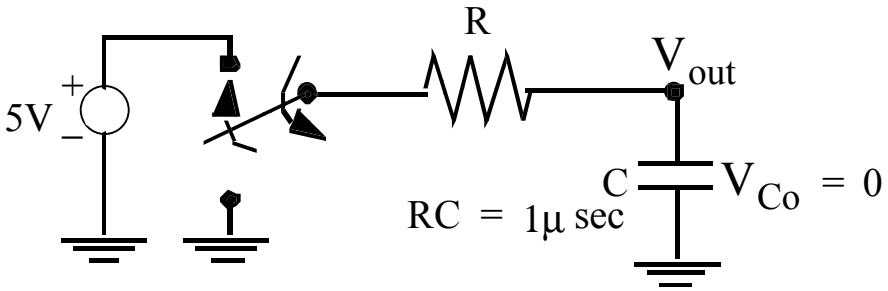
30-40 pts B, and

10-20 pts A.

PULSE: Output is Rising exponential then Falling exponential

Lecture 7

Example: Switch rises at t =0, falls at t = 0.1, 1 or 10μsec (Do 1μsec case)

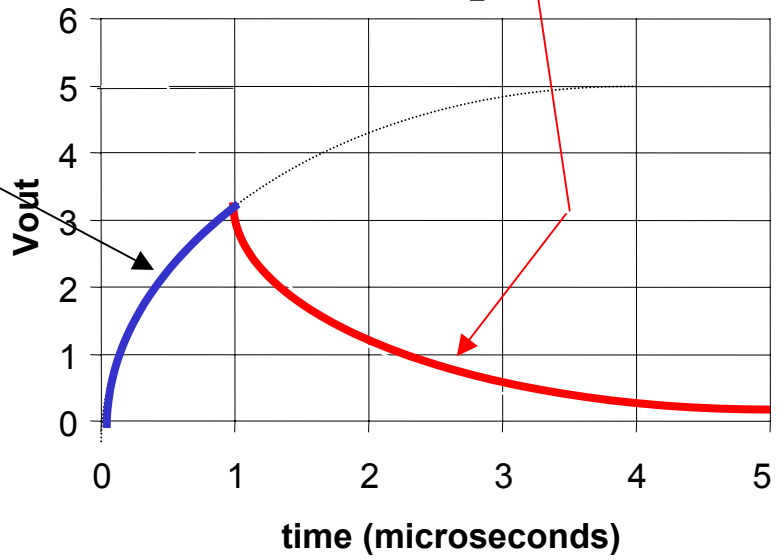


Now starting at 1μsec we are discharging the capacitor so the form is a falling exponential with initial value 3.16 V:

What is equation?

Solution: for RC = 1μsec: during the first rise V obeys:

$$V = 5[1 - e^{\frac{-t}{10^{-6}}}]$$

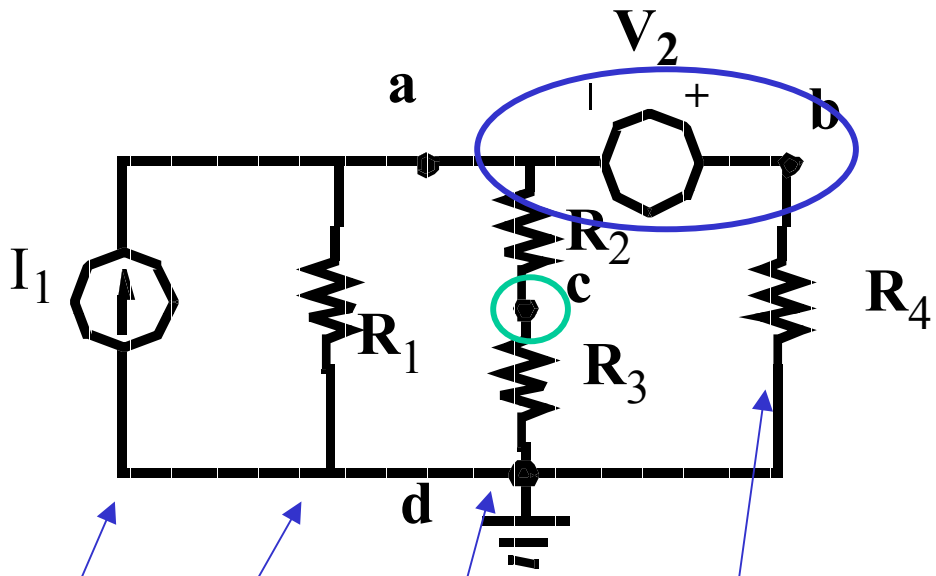


Thus at t = 1μsec, rising voltage reaches

$$5[1 - e^{-1}] = 3.16V$$

EXAMPLE WITH BOTH SPECIAL CASES

Lecture 8



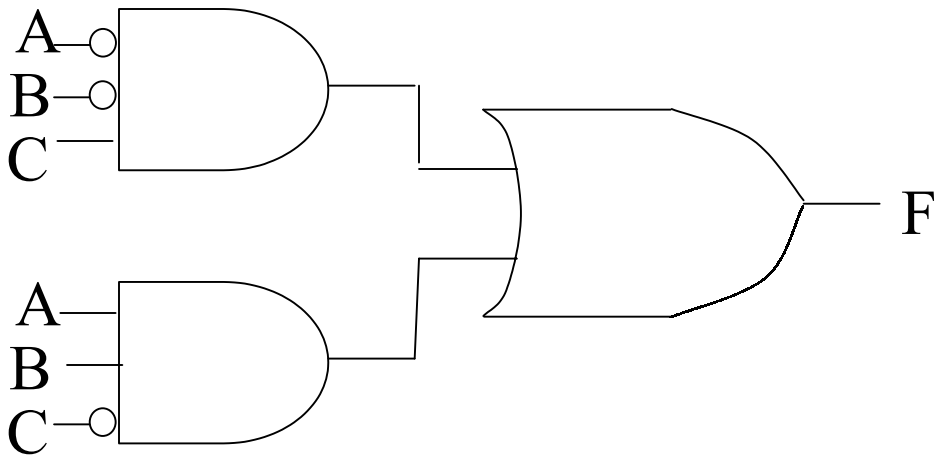
$$I_1 - \frac{V_a}{R_1} - \frac{V_a}{R_2 + R_3} - \frac{(V_a + V_2)}{R_4} = 0$$

Lecture 10

How to Combine Gate to Produce a Desired Logic Function? (More basic Logical Synthesis)

Example:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



$$F=\overline{A}\,\overline{B}C+AB\overline{C}$$

Lecture 11

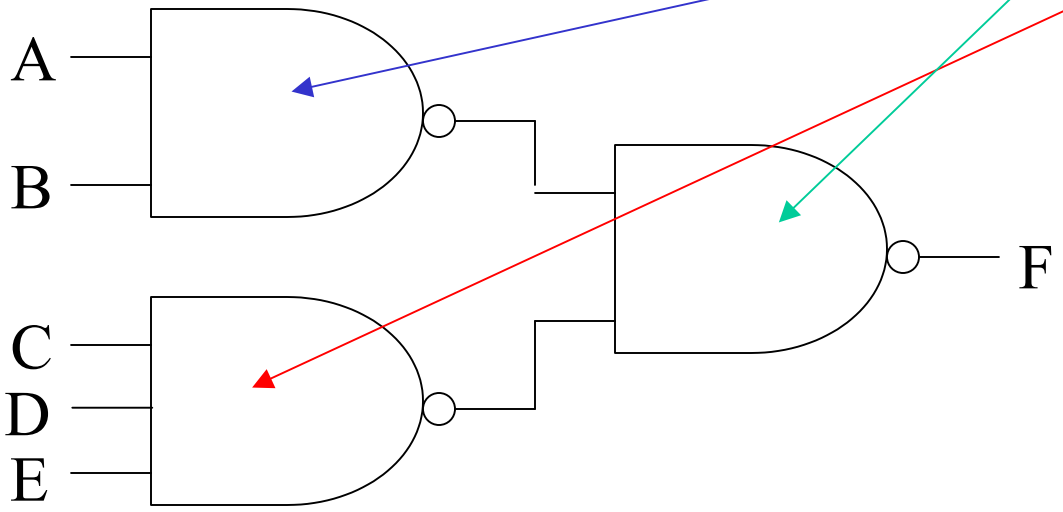
Logical Synthesis Guided by DeMorgan's Theorem

DeMorgan's Theorem :

$$A + B + C = \overline{\left[\overline{A}\,\overline{B}\,\overline{C}\right]} \quad \text{or} \quad \overline{A} + \overline{B} + \overline{C} = \overline{\left[A\,B\,C\right]}$$

Example of Using DeMorgan's Theorem:

$$F = A \bullet B + C \bullet D \bullet E = \overline{\overline{AB} \bullet \overline{CDE}}$$



Thus any sum of products expression can be immediately synthesized from NAND gates alone

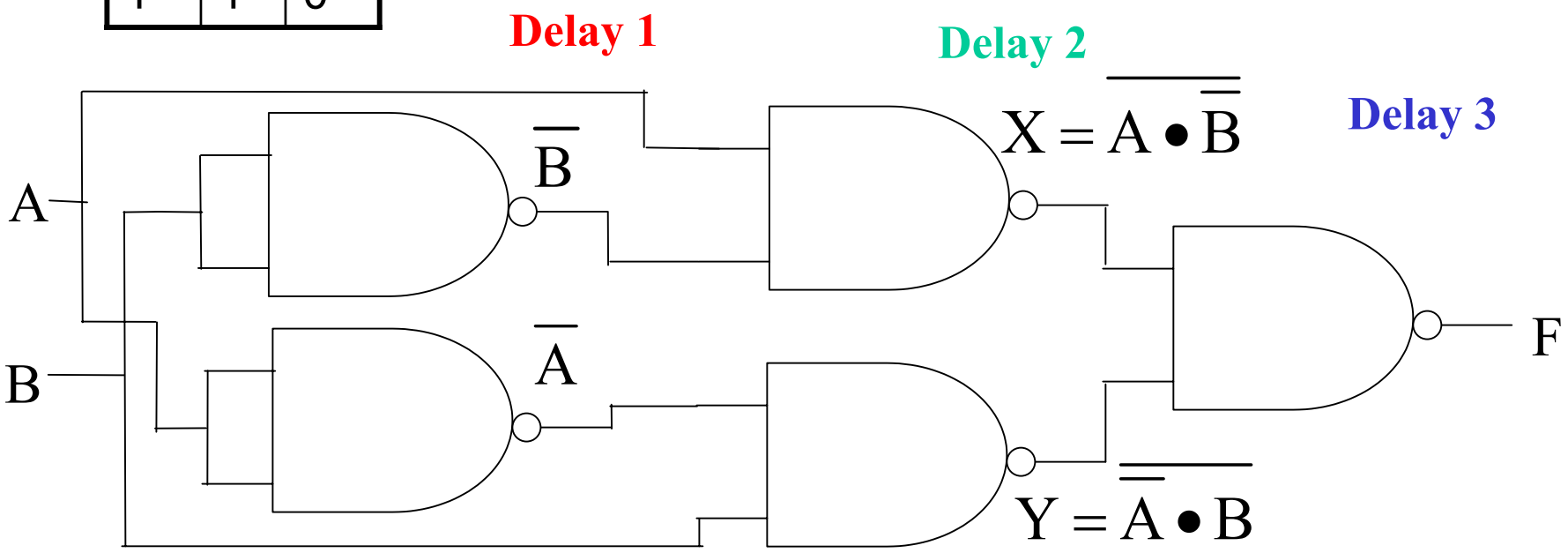
Lecture 11

Logical Synthesis of XOR

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

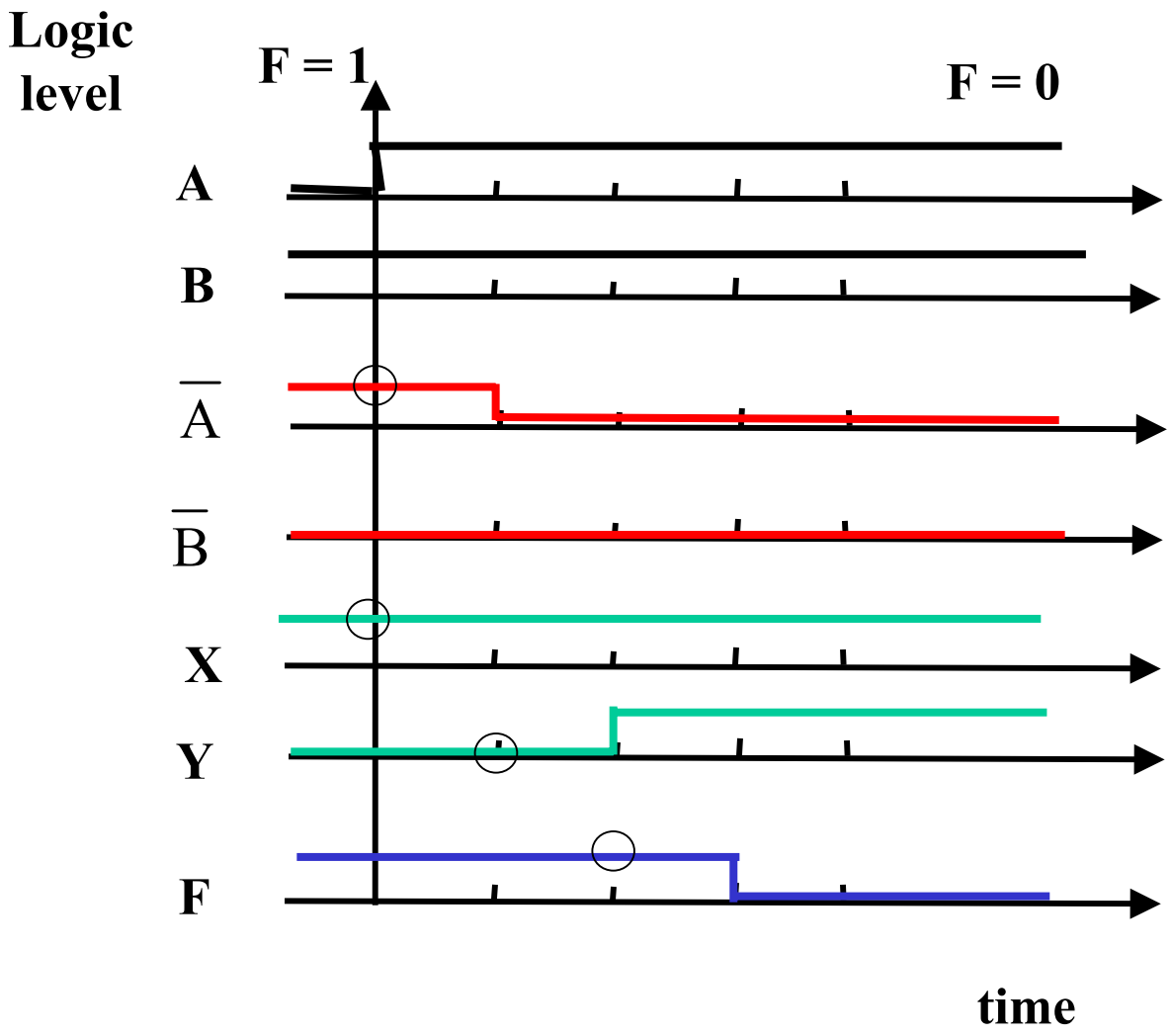
$$F = A \bullet \overline{B} + \overline{A} \bullet B$$

We Need a Timing Diagram!



Lecture 11

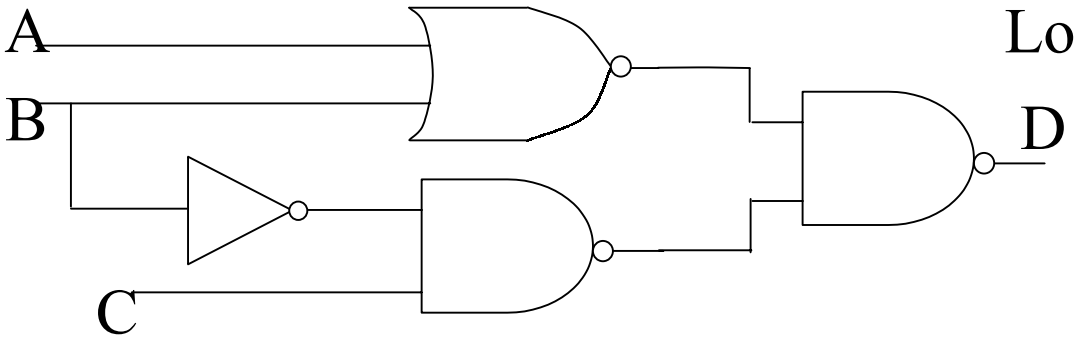
Timing Diagram for Delays in Logic

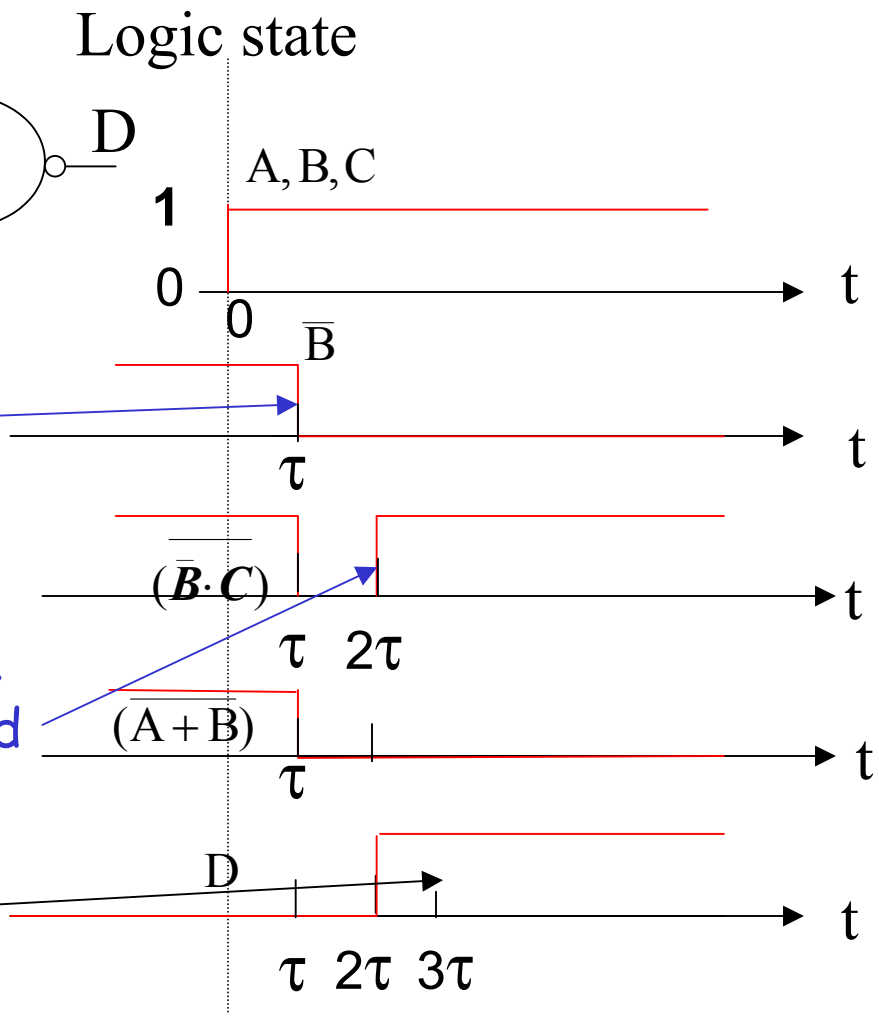


Lecture 11

TIMING DIAGRAMS

Show transitions of variables vs time





Note $\overline{B}$ becomes valid one gate delay after B switches

Note that $(\overline{B} \cdot C)$ becomes valid two gate delays after B&C switch, because the invert function takes one delay and the NAND function a second.

No change at t = 3τ

The 4 Basic Linear Dependent Sources

Lecture 13

Constant of proportionality

Parameter being sensed

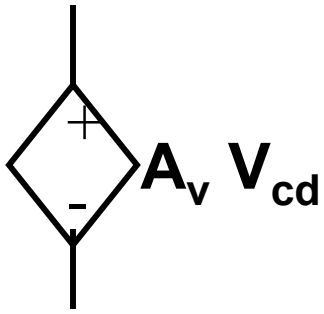
Output

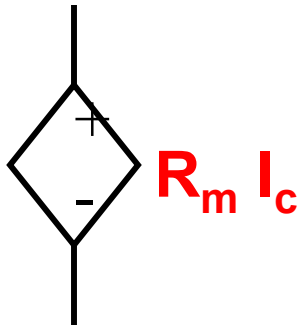
Voltage-controlled voltage source … $V = A_v V_{cd}$

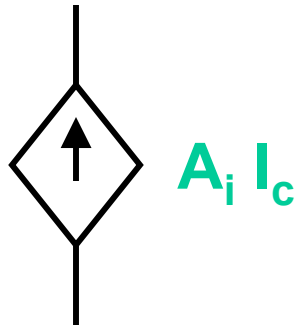
Current-controlled voltage source … $V = R_m I_c$

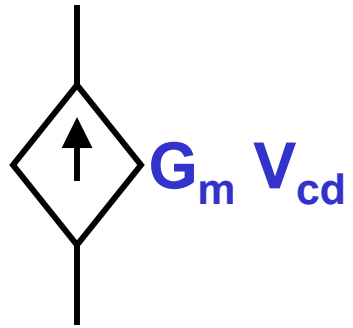
Current-controlled current source … $I = A_i I_c$

Voltage-controlled current source … $I = G_m V_{cd}$









Lecture 13

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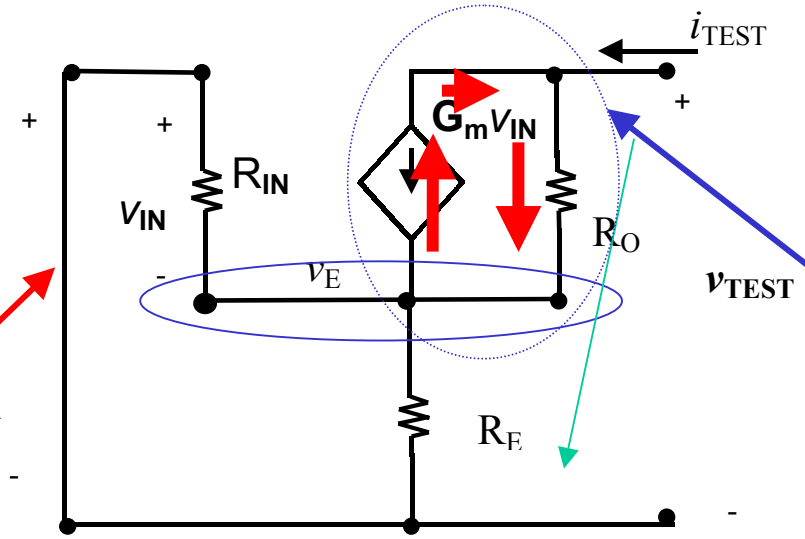
EXAMPLE CIRCUIT: INCREASED OUTPUT RESISTANCE

Add resistor R_E

$v = 0$

The input has been assumed to be shorted



Try a bag.
It is even easier

Analysis: apply i_{TEST} and evaluate v_{TEST}

Unknowns: i_{TEST}, v_{TEST}, v_{IN}, v_E

Need 3 equations to find the ratio of i_{TEST} / v_{TEST}

$v_{IN} = -v_E$ and is not zero!

KCL at v_E

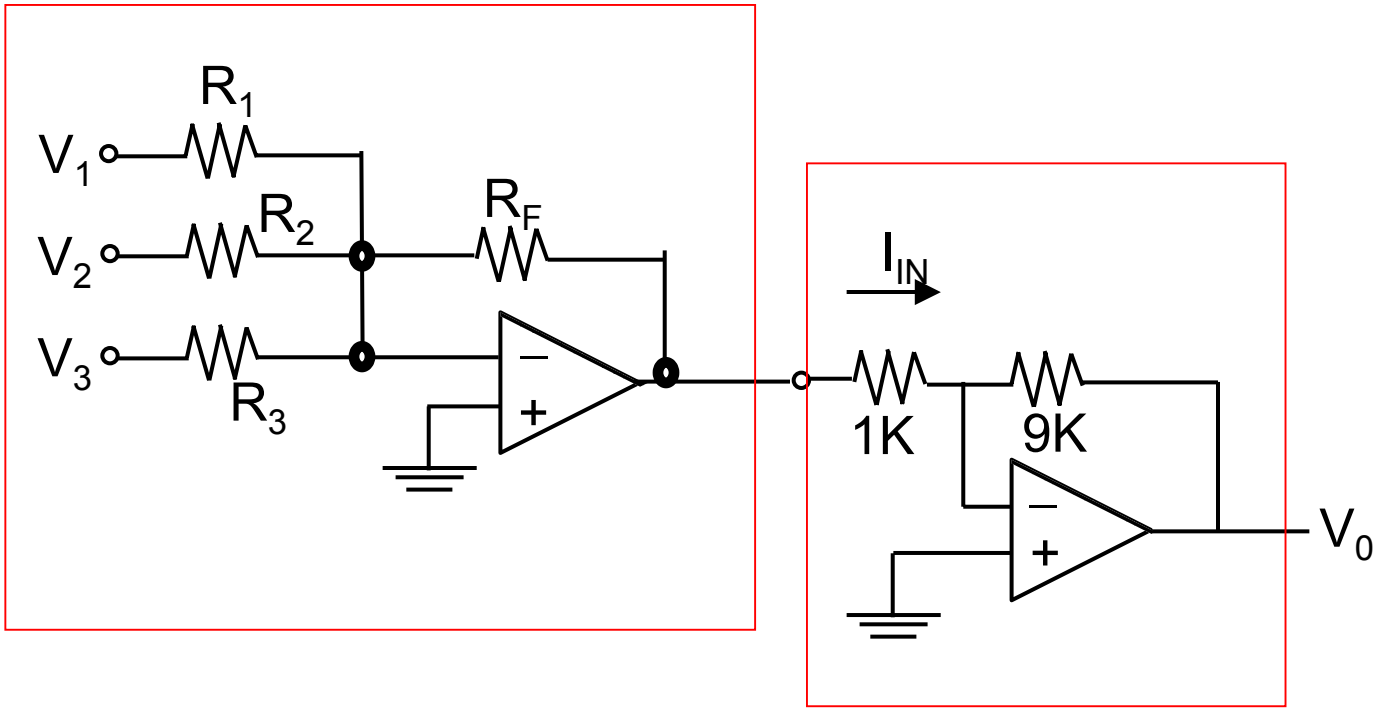
KVL at v_{OUT}

Intuitive Explanation: GmV_{IN} burps current which has to also go through R_0. This raises v_{TEST} and the output impedance v_{TEST}/i_{TEST}

Finish this in the homework

Lecture 14

CASCADE OP-AMP CIRCUITS



How do you get started on finding V_O?

Hint: Identify Stages

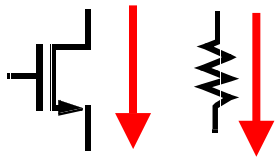
Hint: I_{IN} does not affect V_{O1}

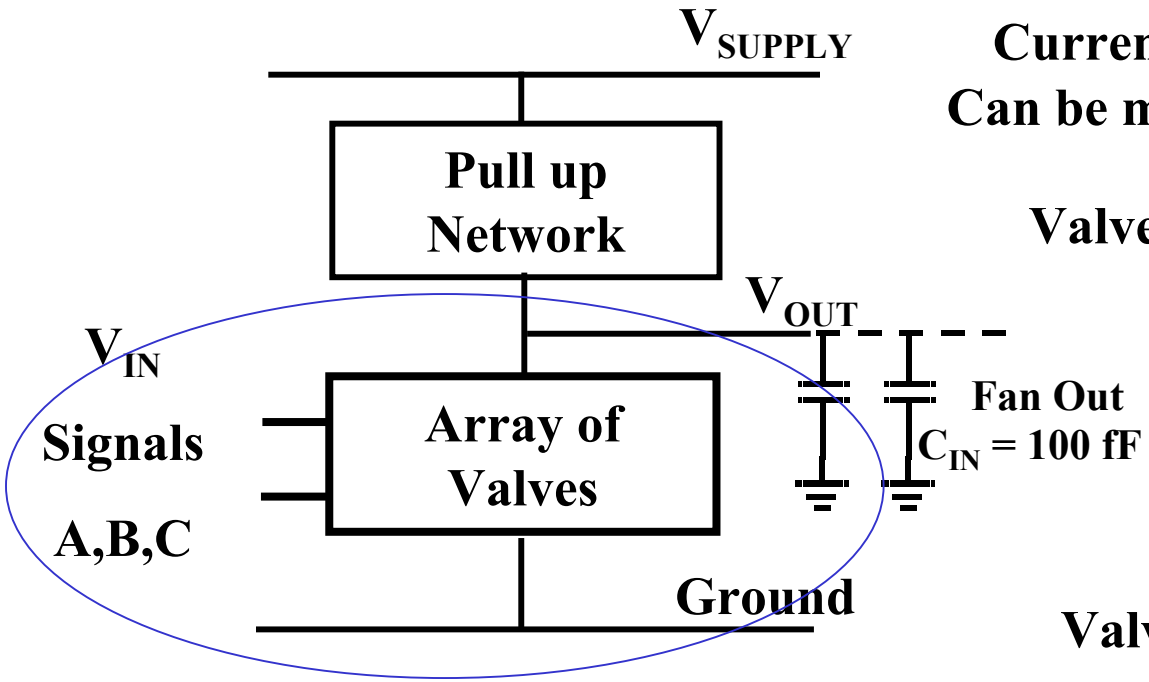
See the further examples of op-amp circuits in the reader

Logic Gates – How are they built in practice?

Lecture 15

A Valve is a Transistor

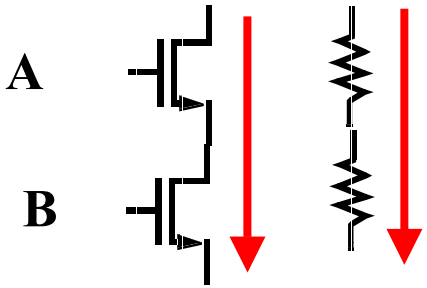




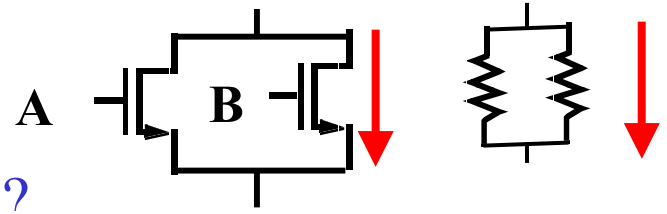
Current flows when V_{IN} is high

Can be modeled by a 10kΩ resistor

Valves in Series => NAND



Valves in Parallel => NOR

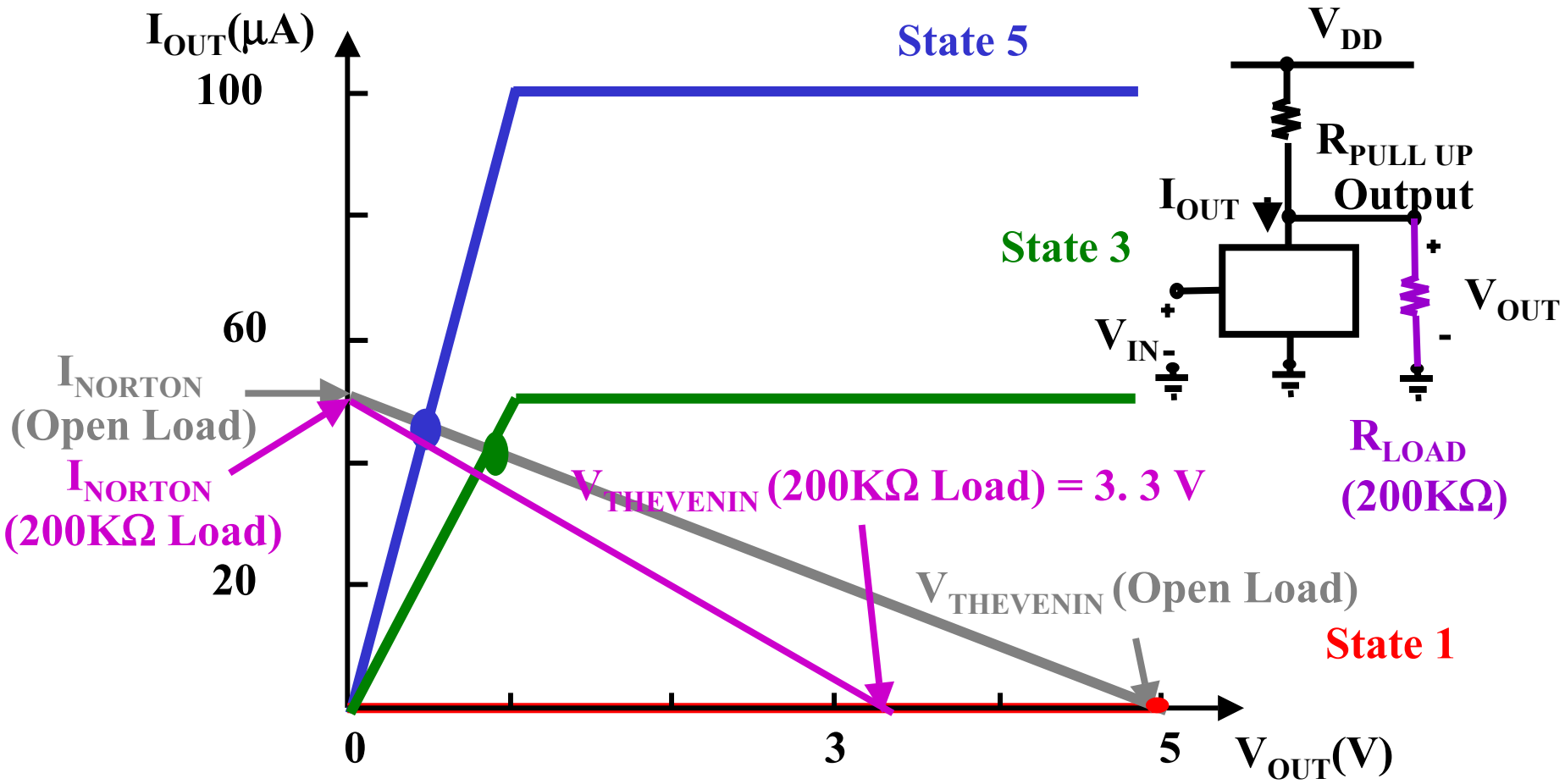


What goes in this box?

How does it affect digital performance?

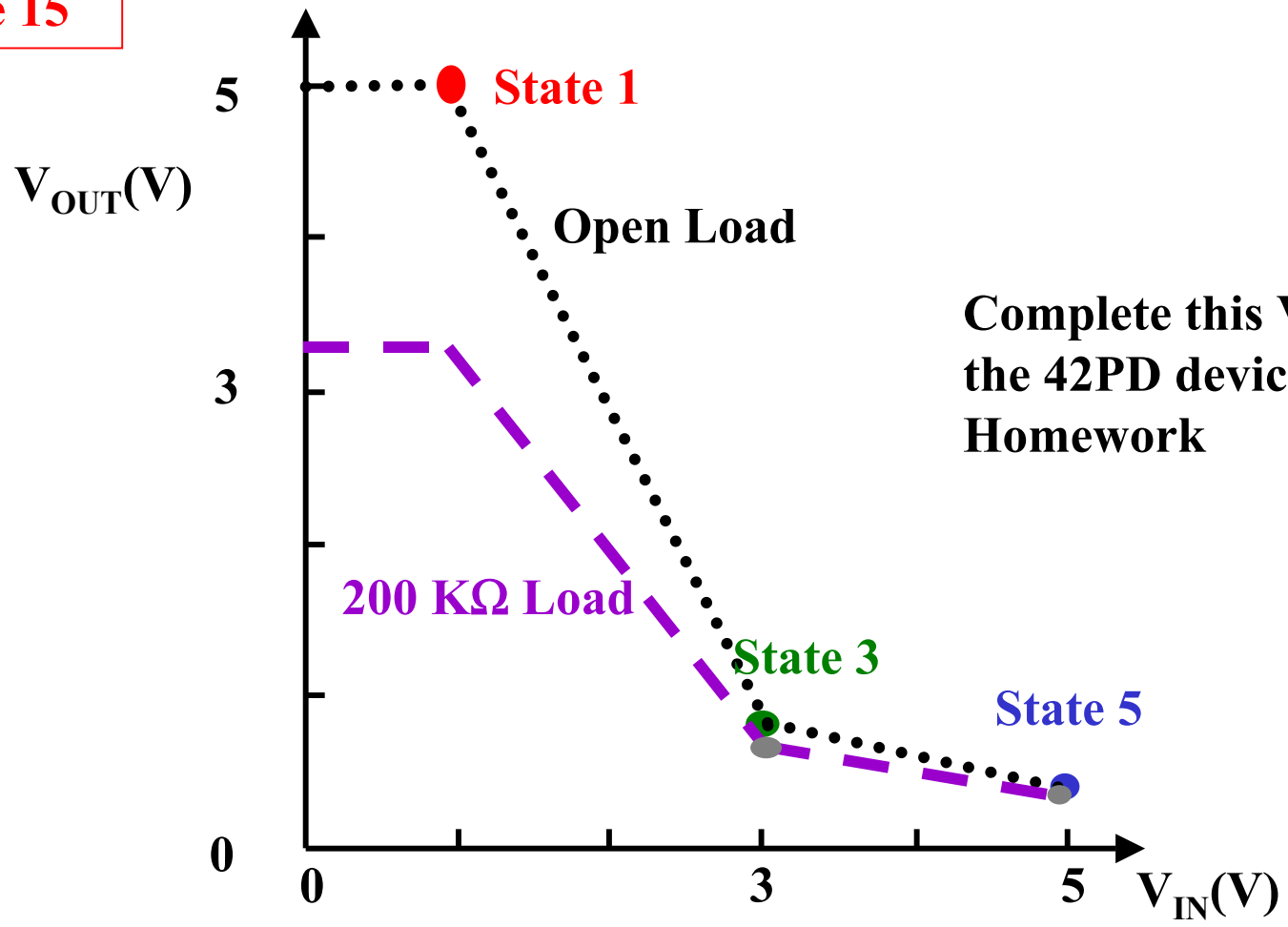
Composite Current Plot for the 42PD Circuit with 200kΩ Load to Ground

Lecture 15



Voltage Transfer Function for the 42PD Logic Circuit w/wo Load

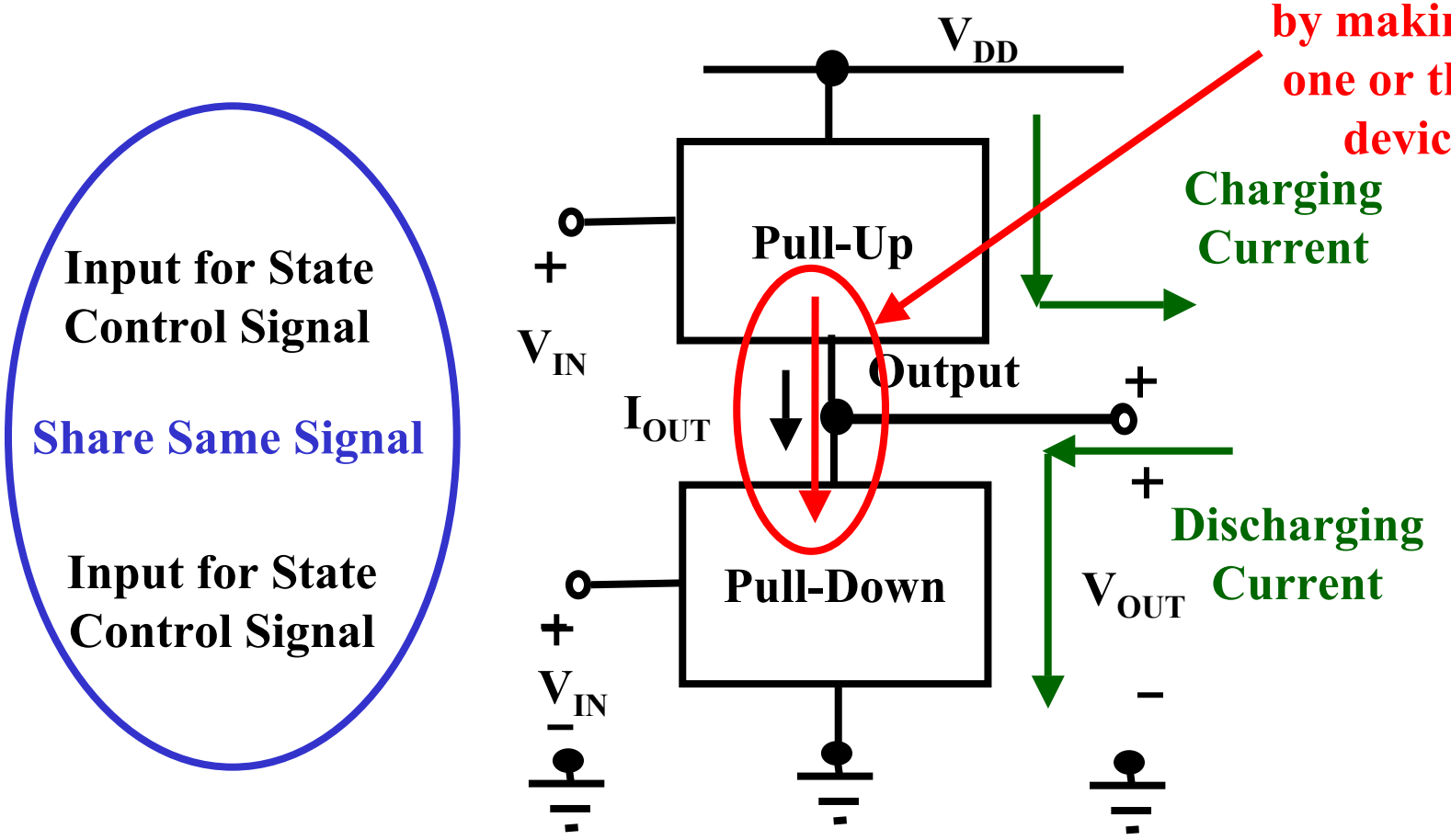
Lecture 15



Complete this VTC for the 42PD device in the Homework

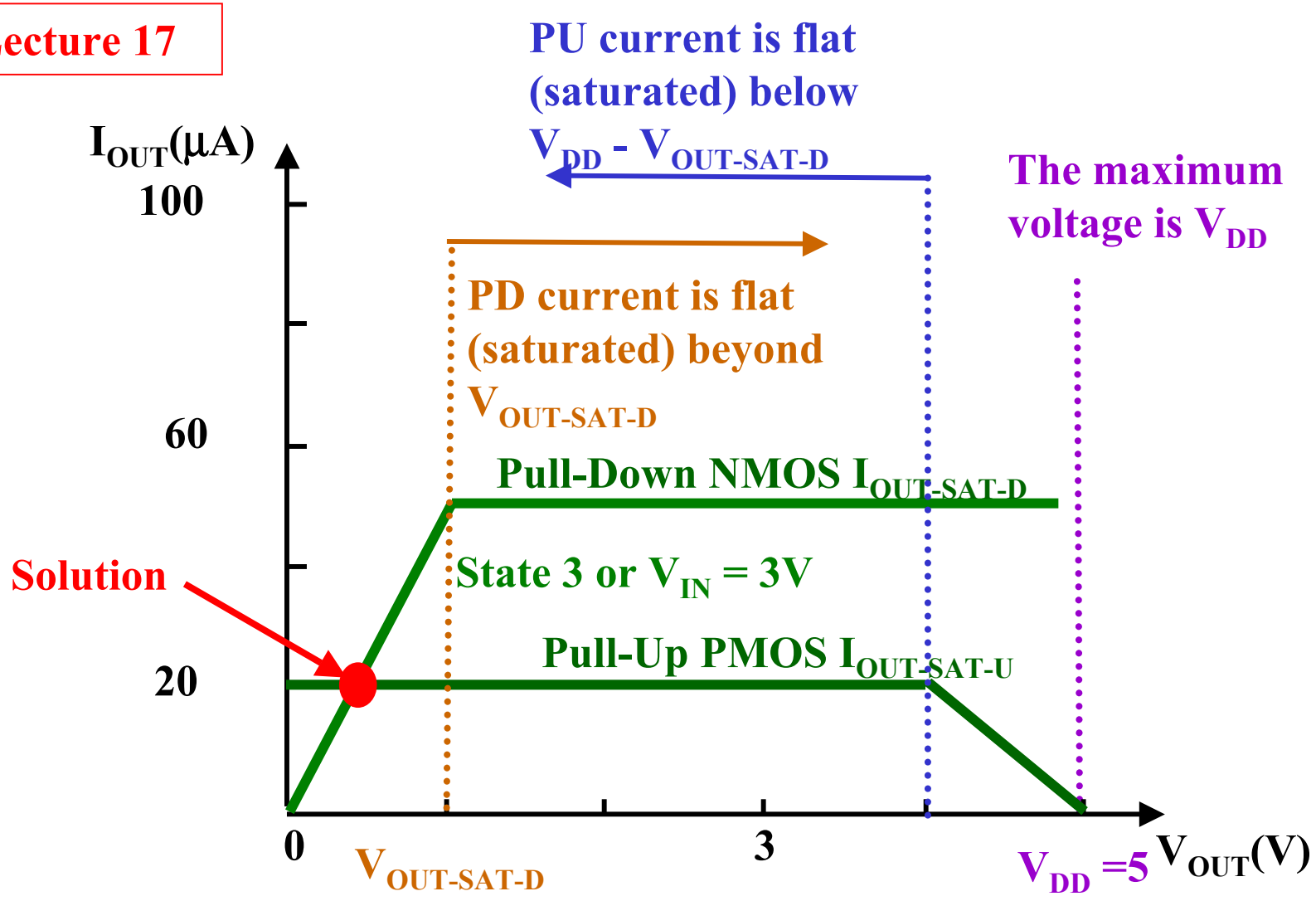
Pull-Down and Pull-Up Must Complement Rather Than Fight Each Other

Lecture 16



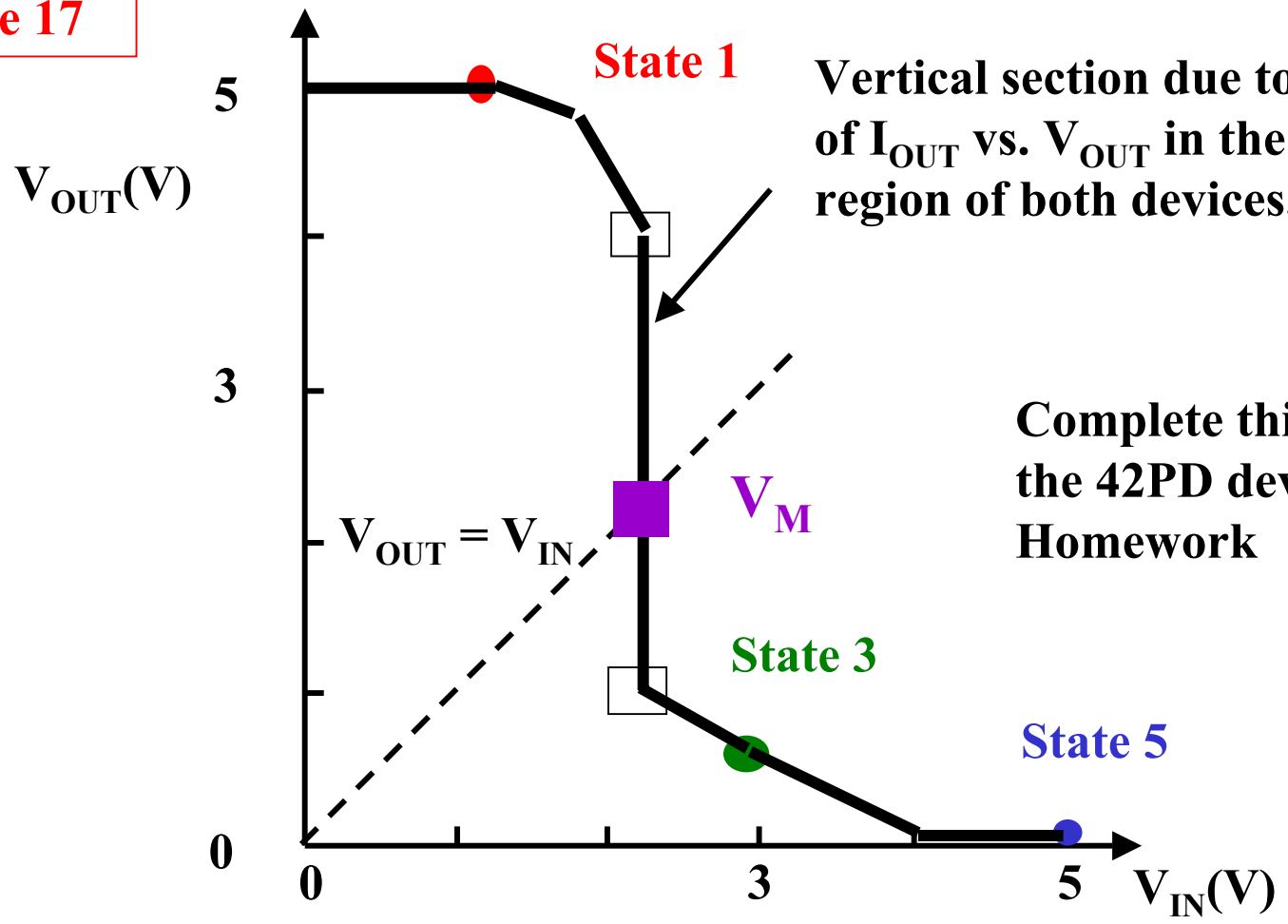
Composite I_{OUT} vs. V_{OUT} for CMOS

Lecture 17



Voltage Transfer Function for the Complementary Logic Circuit

Lecture 17



Vertical section due to zero slope of I_{OUT} vs. V_{OUT} in the saturation region of both devices.

Complete this VTC for the 42PD device in the Homework

Lecture 17

Method for Finding V_M

At V_M,

1) $V_{OUT} = V_{IN} = V_M$

2) Both devices are in saturation

3) $I_{OUT\ PD} = I_{OUT\text{-}PU}$

$$I_{OUT-PD} = k_D\left(V_{IN} - V_{TD}\right)V_{TD} = I_{OUT-PU} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{TU}$$

Substitute V_M

Solve for V_M

Example Result: When $k_D = k_P$ and $V_{TD} = V_{TU}$, $V_M = V_{DD}/2$

Switched Equivalent Resistance Model

Lecture 17

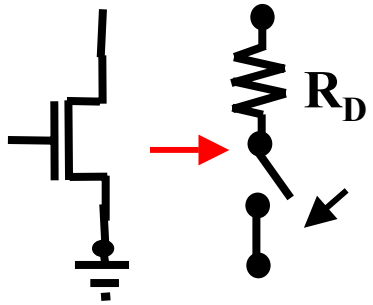
The above model assumes the device is an ideal constant current source.

1) This is not true below $V_{OUT\text{-}SAT\text{-}D}$ and leads to in accuracies.

2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting $0.69R_DC$ equal to the Δt found above

$$\Delta t = \frac{C_{OUT}V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_DC_{OUT}$$



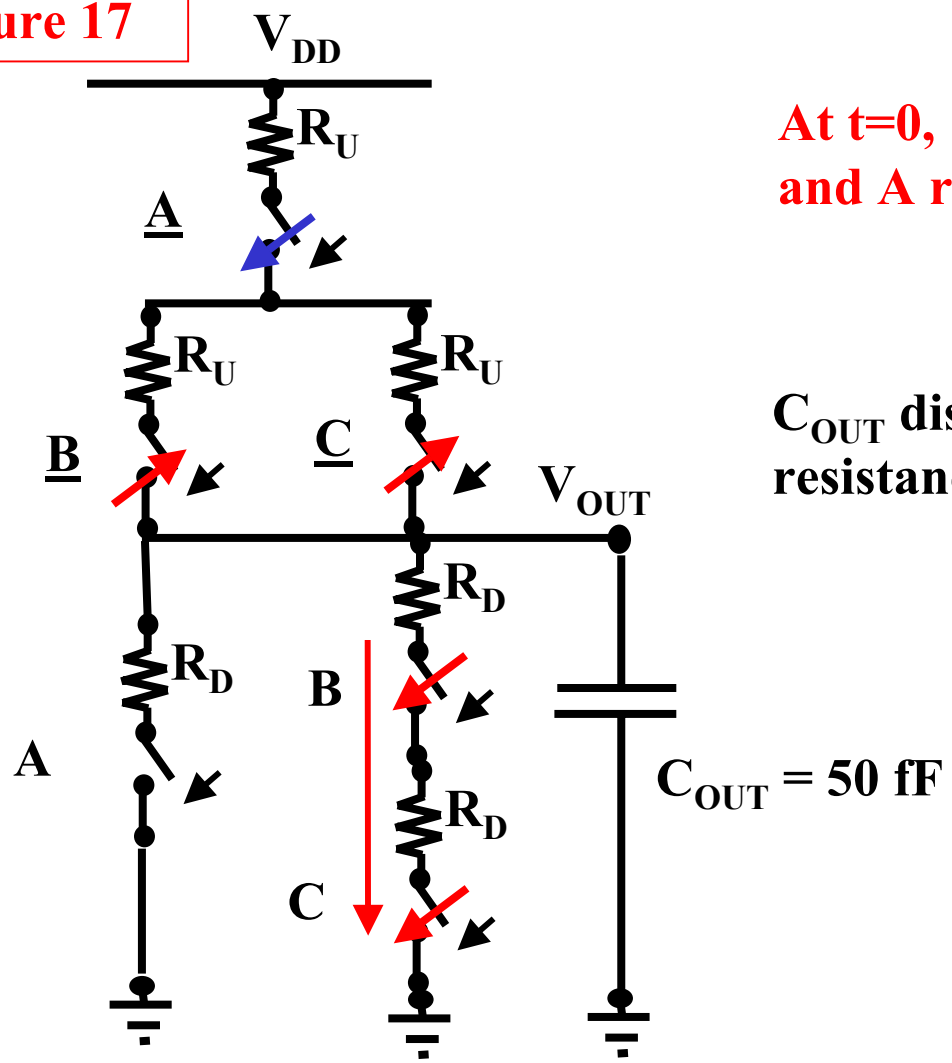
This gives

$$R_D = \frac{V_{DD}}{2\cdot(0.69)I_{OUT-SAT-D}} \approx \frac{3}{4}\frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4}\frac{5V}{100\mu A} = 37.5k\Omega$$

Each device can now be replaced by this equivalent resistor.

Logic Gate Propagation Delay (Cont.)

Lecture 17



At t=0, B and C switch to high = V_{DD} and A remains low.

C_{OUT} discharges through the pull-down resistance of gates B and C in series.

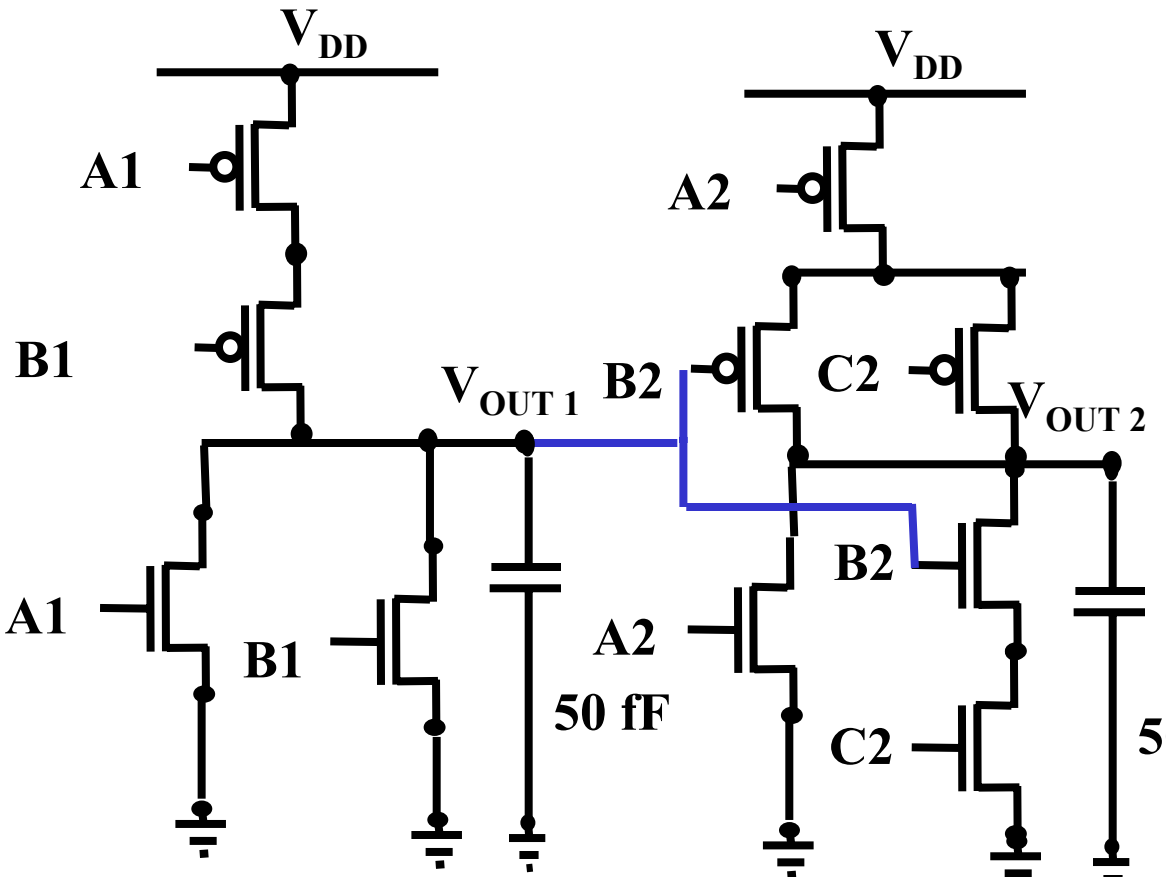
$$\Delta t = 0.69(R_{DB}+R_{DC})C_{OUT}$$
$$= 0.69(20k\Omega)(50fF) = 690 \text{ ps}$$

The propagation delay is two times longer than that for the inverter!

Lecture 18

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



$B2 = V_{OUT\ 1}$

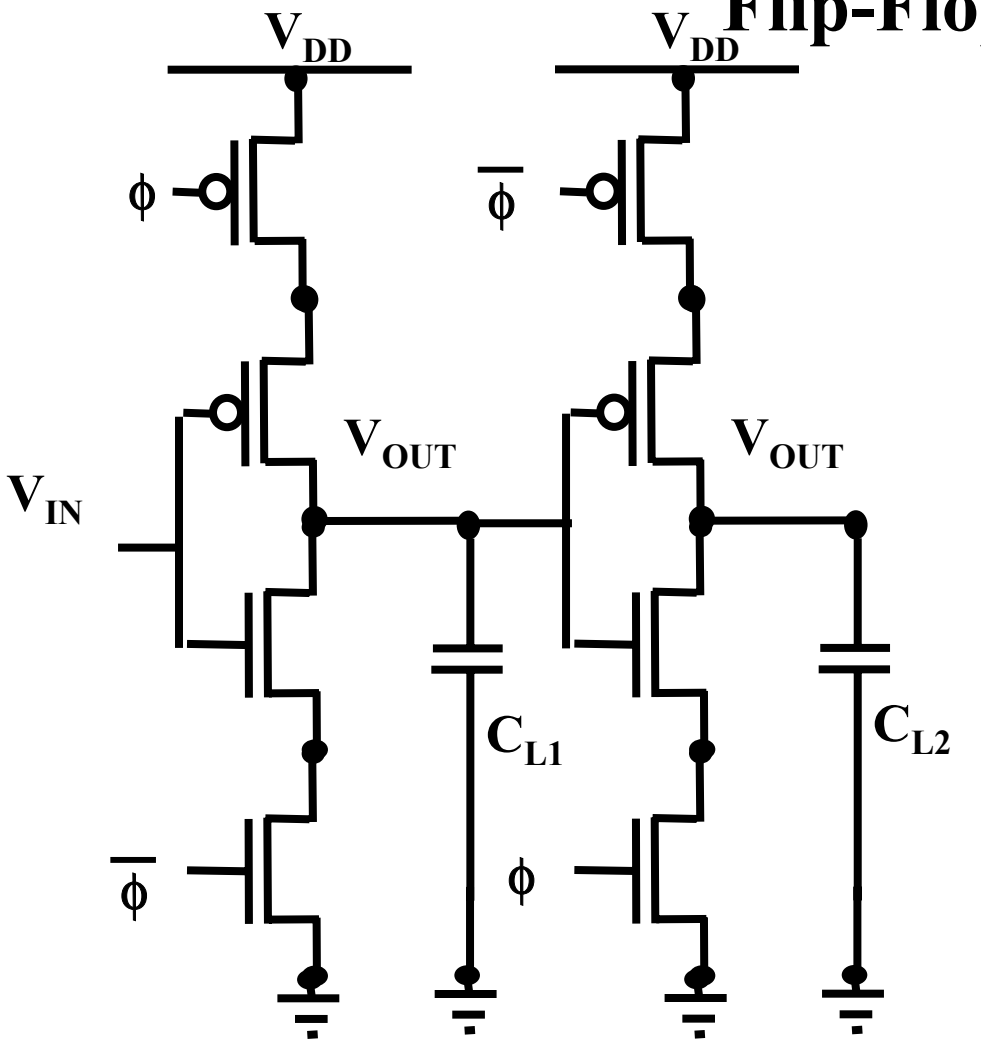
The four independent input are A1, B1, A2 and C2.

A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output

Lecture 18

A Double Latch is an Edge-Triggered D Type Flip-Flop

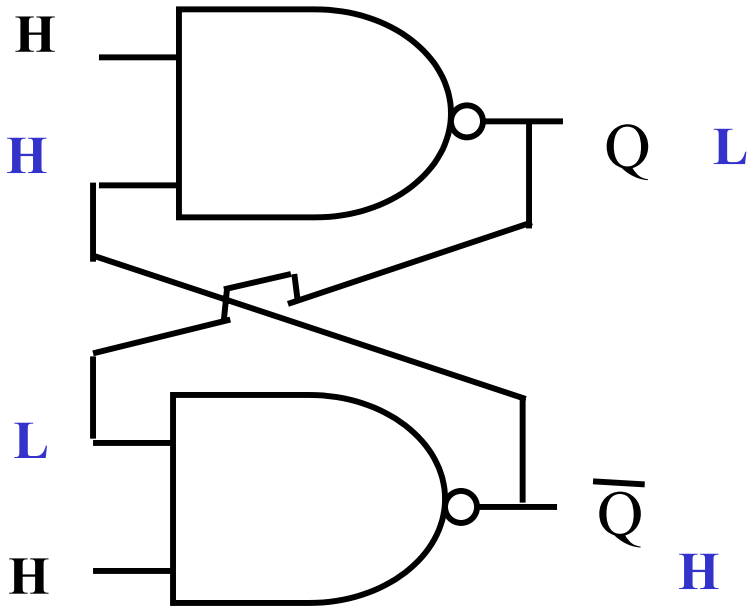


During the low part of the clock cycle this circuit records the input value and when the clock goes high drives $V_{OUT\,2}$ to the voltage level that arrived. (This is the classic function of a D flip-flop.)

Note that this circuit is not fooled by noise on the input and makes its decision on the rising edge of the clock (edge-triggered).

Feedback Can Provide Memory

Lecture 19



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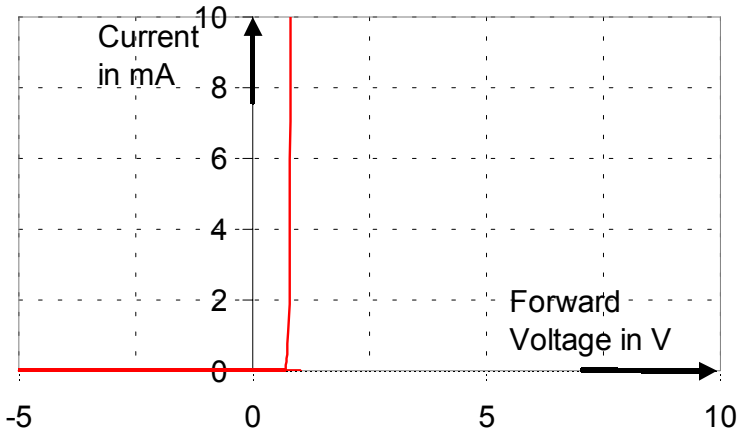
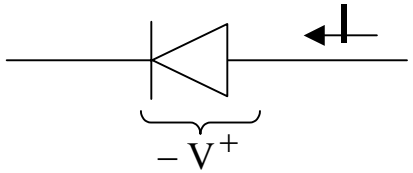
Lecture 20 DIODE I-V CHARACTERISTICS AND MODELS

The equation $I = I_0 \exp(qV/kT - 1)$

is graphed below for $I_0 = 10^{-15}$ A

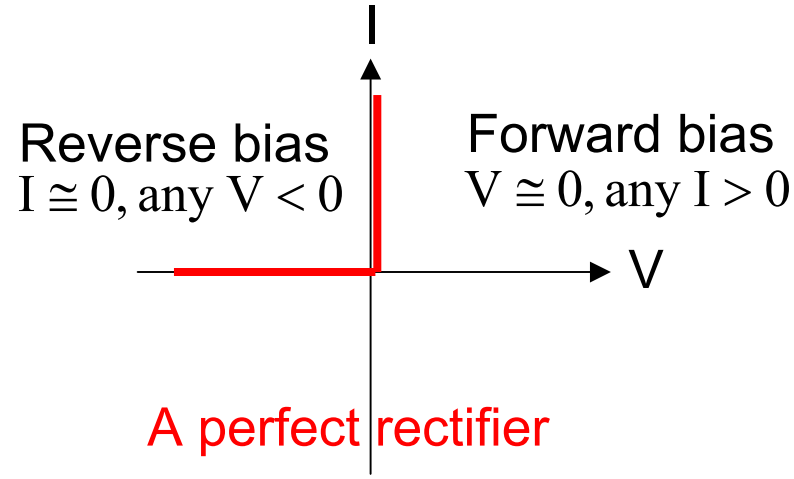


The characteristic is described as a "rectifier" – that is, a device that permits current to pass in only one direction. (The hydraulic analog is a "check value".) Hence the symbol:



Simple "Perfect Rectifier" Model

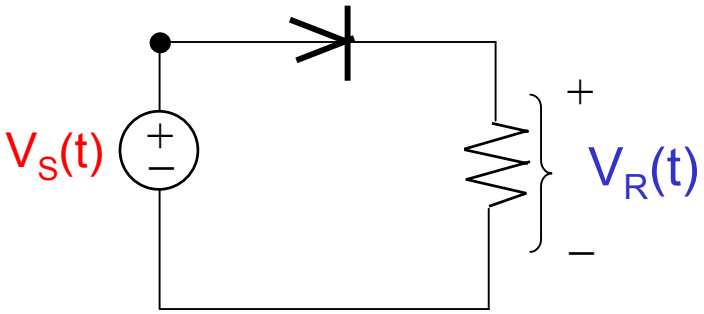
If we can ignore the small forward-bias voltage drop of a diode, a simple effective model is the "perfect rectifier," whose I-V characteristic is given below:

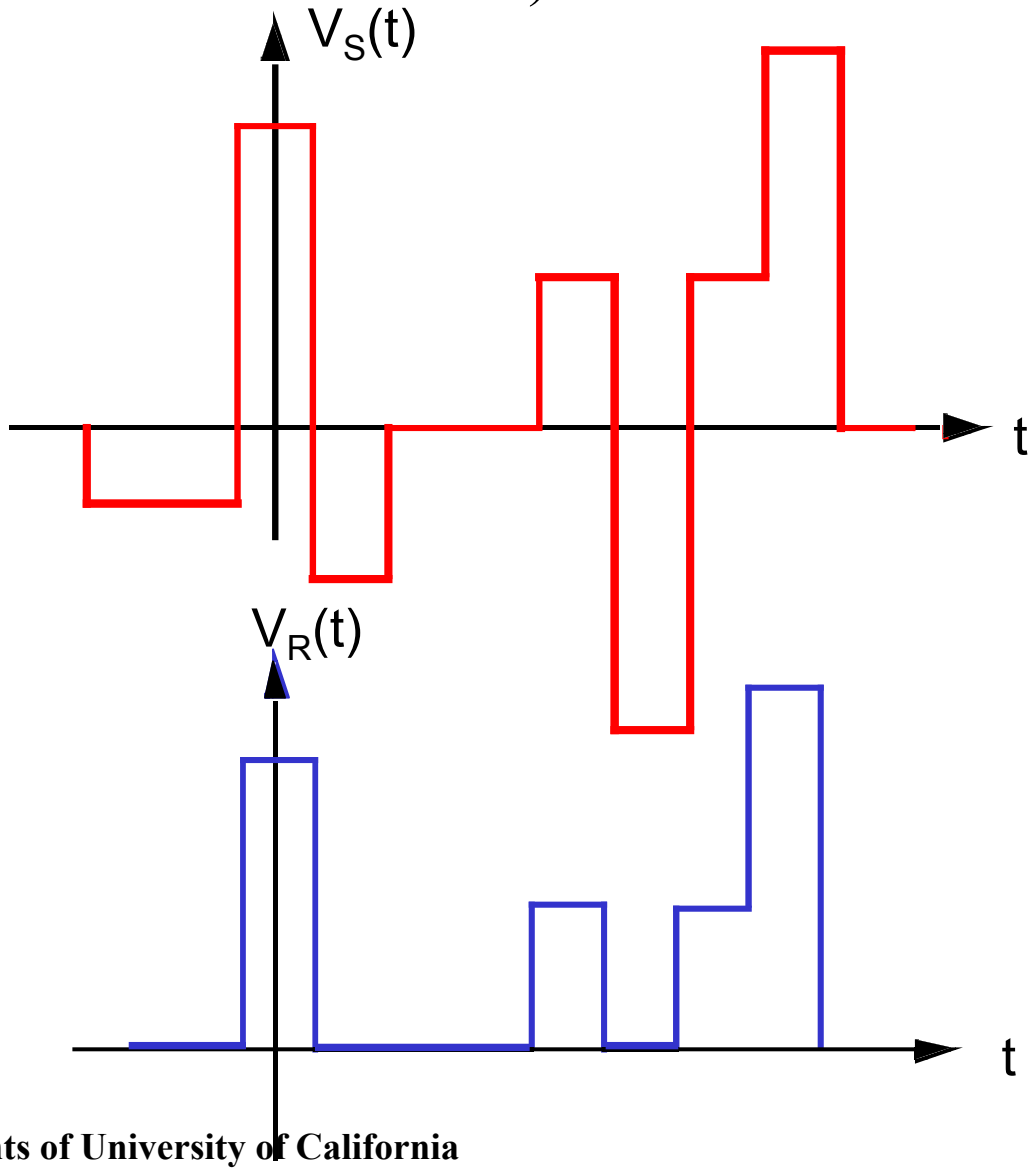


Lecture 20

COOL THINGS A DIODE CAN DO

(Use perfect rectifier model)

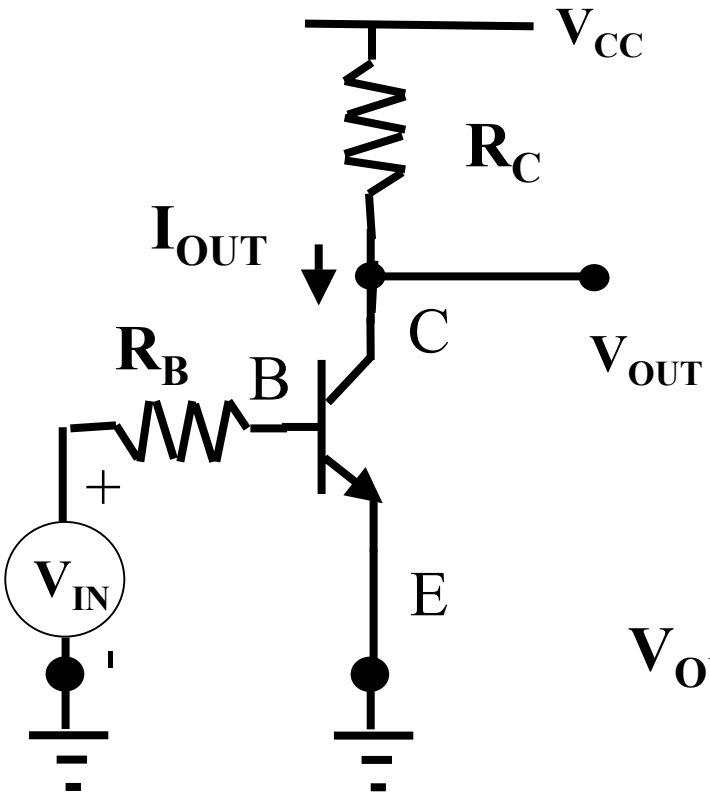




"rectified" version of input waveform

Lecture 21

npn Bipolar Transistor: V_{OUT} vs. V_{IN}



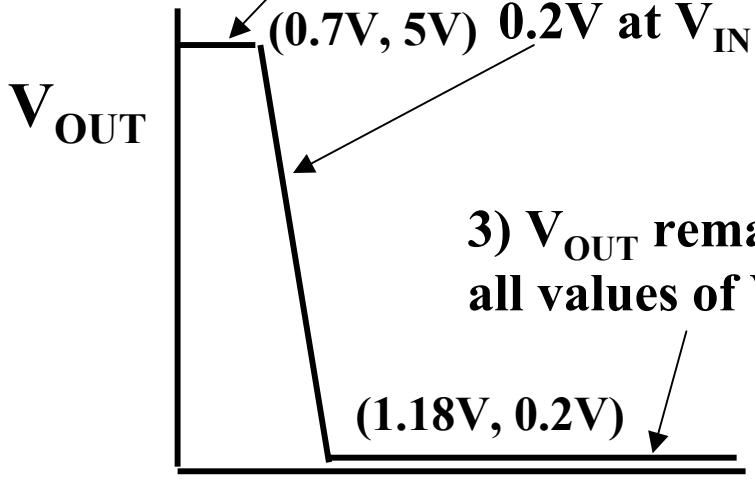
$\beta = 100$ $R_B = 10k\Omega$

$R_C = 1k\Omega$ $V_{CC} = 5V$

1) V_{OUT} is V_{CC} till V_{IN} reaches 0.7V

2) V_{OUT} decreases linearly with V_{IN} until V_{OUT} reaches 0.2V at V_{IN} = 1.18V

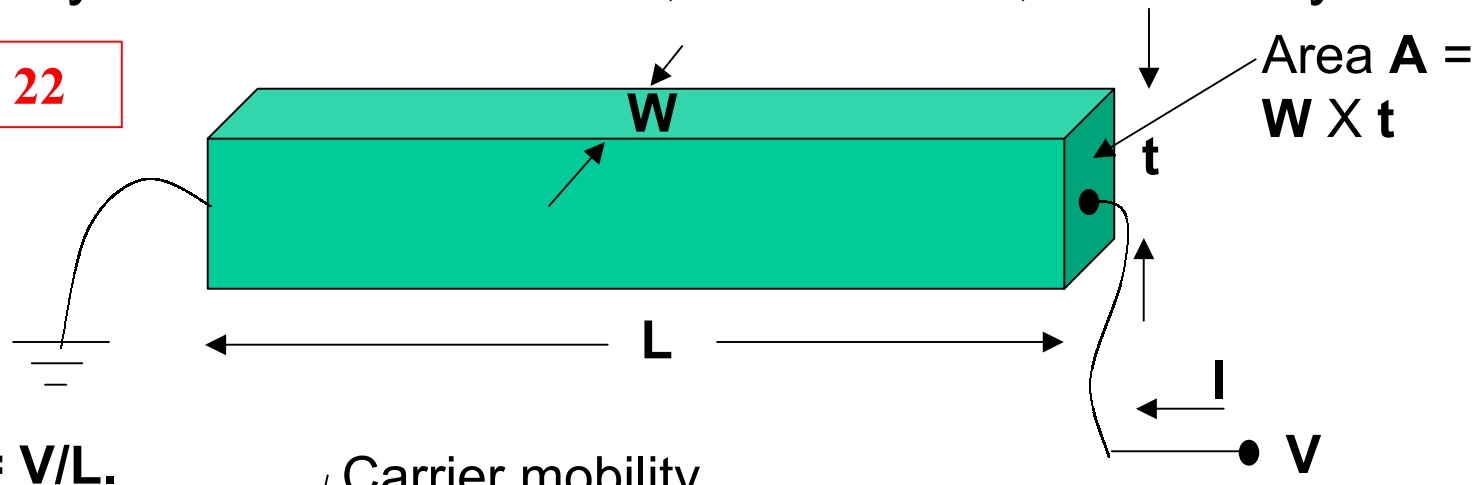
3) V_{OUT} remains at 0.2 V for all values of V_{IN} above 1.18V



2/04/01

Physics of Current Flow, Resistance, Resistivity

Lecture 22



E = V/L.

I = V/R

Carrier mobility

Carriers per unit volume

R = ρL/A =(1/q μN) L/W t = (L/W) /μ(qNt)

But **q N t** has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness **t** when the film has **N** carriers/cm^3 and is **t** units thick. Thus we call **q N t** the "**Q**" and

R = (L/W)/ μQ = L/W $R_{\square}$

Where $R_{\square}$ is the resistance of a "square" of the film. Clearly if L is four times W, then R = 4 $R_{\square}$.

Relation of Current to Physical Parameters

Lecture 23

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_T) \cdot V_{OUT-SAT-n}$$

Mobility of carriers

Oxide thickness

Geometrical Layout

Excess Gate drive

Voltage of scattering velocity limit

$$\mu_n = 500\left(cm^2/Vs\right) \qquad \mu_p = 150\left(cm^2/Vs\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\left(8.85x10^{-14}\,F/cm\right)(3.9)}{6x10^{-7}\,cm} = 5.75x10^{-7}\,F/cm^2$$

$$V_{OUT-SAT-n} = E_{Crit} \cdot L = 10^4\left(V/cm\right) \cdot 0.25x10^{-4}\,cm = 0.25V$$

CMOS Device Parameters at 0.25μm

Lecture 23

Gate length is 0.25 μm = 250 nm

V_{DD} = 2.5V

	V_T(V)	$V_{OUT-SAT}$ (V)	k' (μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

These parameters are from re-fitting I vs. V data in Chapter 3 of the EECS 141 Text Book by Rabaey with saturation current model we are using in EE42.

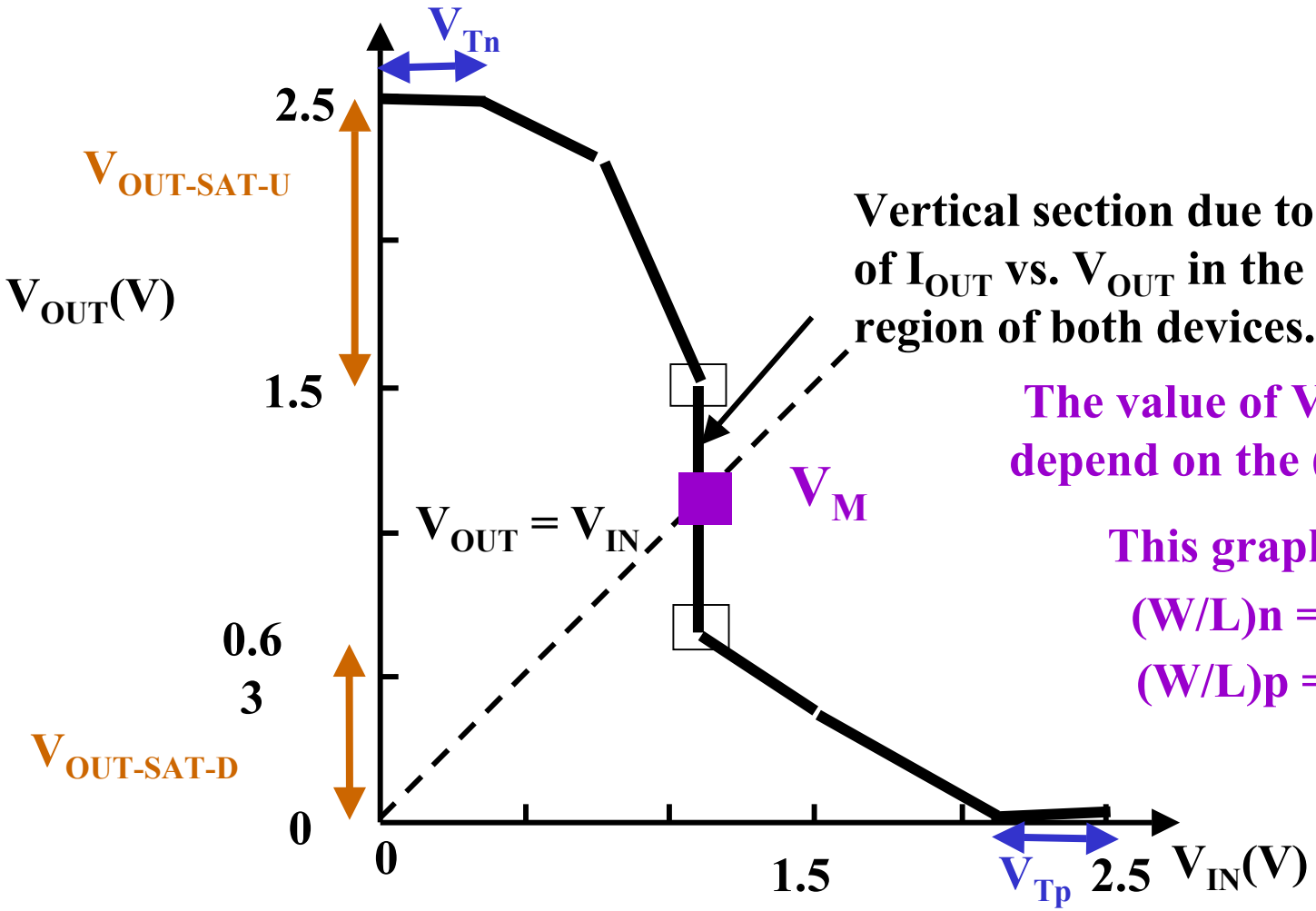
Here $V_{IN} = V_{DD}$ is used to estimate the maximum I_{DS}

$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

$$I_{OUT-SAT-D} = \left(100\mu A/V^2\right)\left(\frac{0.375}{0.25}\right)(2.5V - 0.43V)(0.63V) = 196\mu A$$

Voltage Transfer Function for the 0.25 μm CMOS Inverter

Lecture 23



Vertical section due to zero slope of I_{OUT} vs. V_{OUT} in the saturation region of both devices.

The value of VM will depend on the (W/L)'s

This graph is for

(W/L)n = 1.5

(W/L)p = 3.0

Lecture 23

Finding V_M for 0.25 μm Inverter

At V_M,

1) $V_{OUT} = V_{IN} = V_M$

2) **Both devices are in saturation**

3) $I_{OUT\text{-}SAT\text{-}n} = I_{OUT\text{-}SAT\text{-}p}$

Result will depend on (W/L) ratios.

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n\left(V_{IN} - V_{Tn}\right)V_{OUT-SAT-n} =$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p\left(V_{DD} - V_{IN} - V_{Tp}\right)V_{OUT-SAT-p}$$

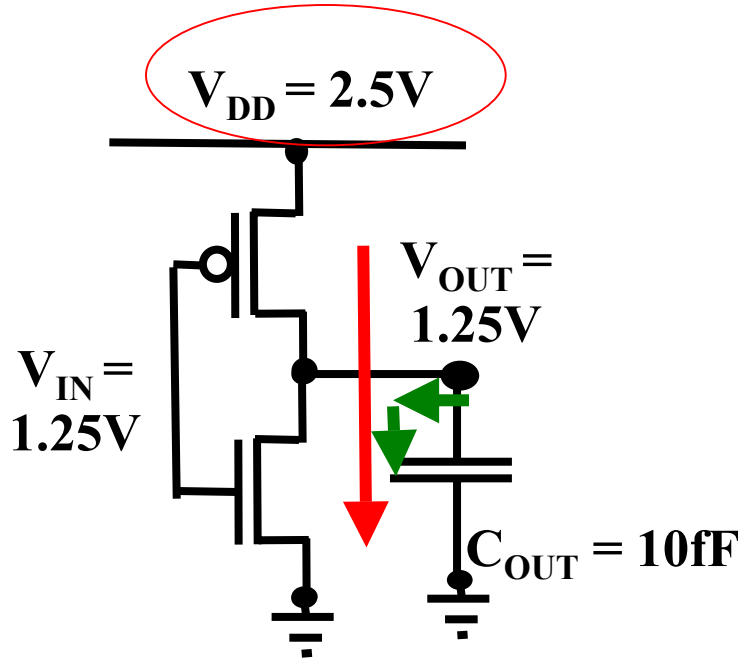
Substitute V_M **Solve for V_M**

For $(W/L)_n = 1.5$ and $(W/L)_p = 3.0$ V_M is 1.17V

Lecture 23

CMOS Inverter in Short-Circuit Condition

Assume the CMOS inverter from above with V_{IN} = 1.25V and V_{OUT} = 1.25V driving a 10 fF capacitor



What happens to the output signal?

The capacitor slowly discharges to try to find an output voltage that balances the NMOS and PMOS currents for the given value of V_{IN}.

$$\frac{\partial V}{\partial t} = \frac{I}{C} = \frac{13.7\mu A}{10\,fF} = 1.37(V/ns)$$

$I_{Short\text{-}Circuit}$ = 63.8 µA
(We used $V_{IN} = V_{DD}/2$)

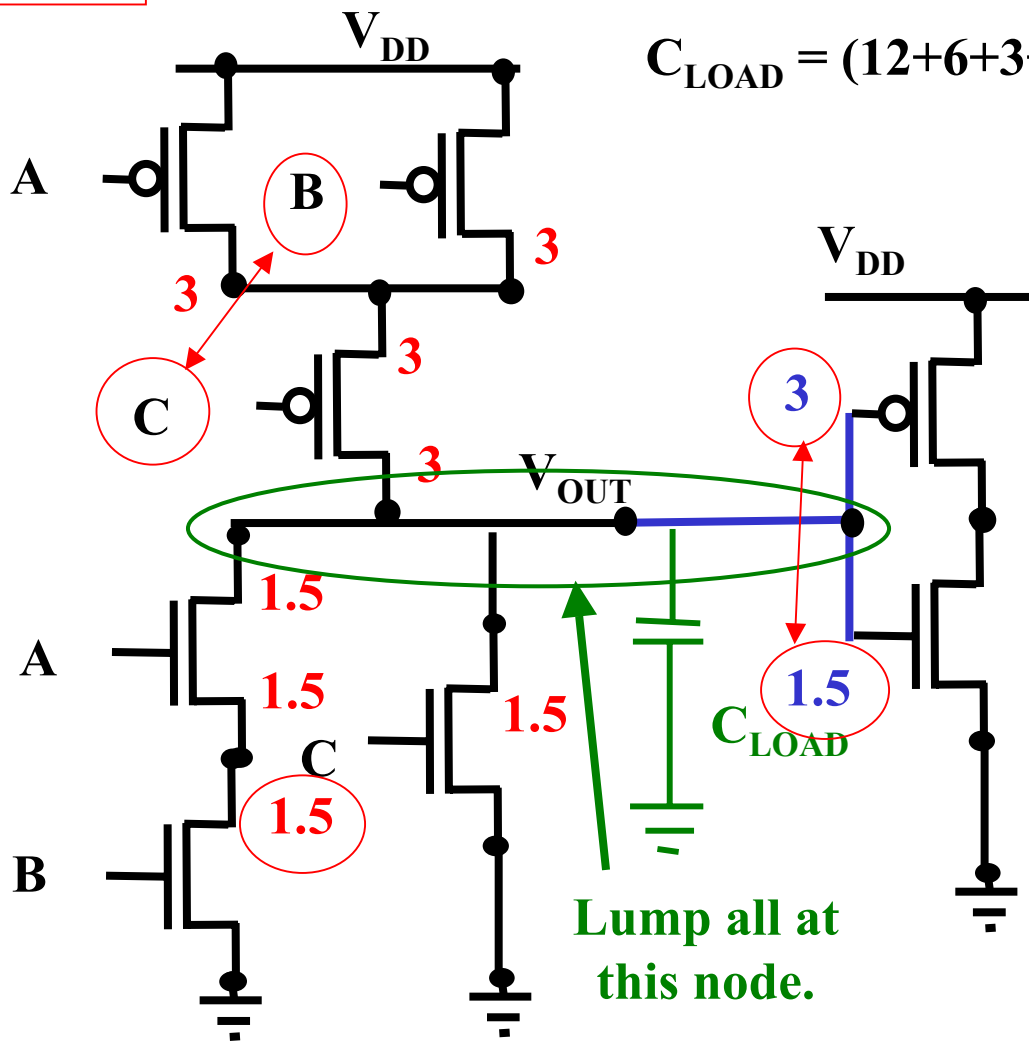
$I_{Discharge\_Load}$ = 13.7 µA
(We Used $V_{IN} = V_{DD}/2$)

Study this page carefully as three starting point mistakes were corrected.

Version Date 12/04/01

Lecture 24

Example CMOS Circuit



$C_{LOAD} = (12+6+3+1.5)(0.4fF) = 9$ fF

Worst case is a=1, c =0, and b changes 1 => 0

$R = 2R_{DP} = 24k\Omega$

$\Delta t = 0.69(24k\Omega)(9\text{ fF}) = 149$ ps

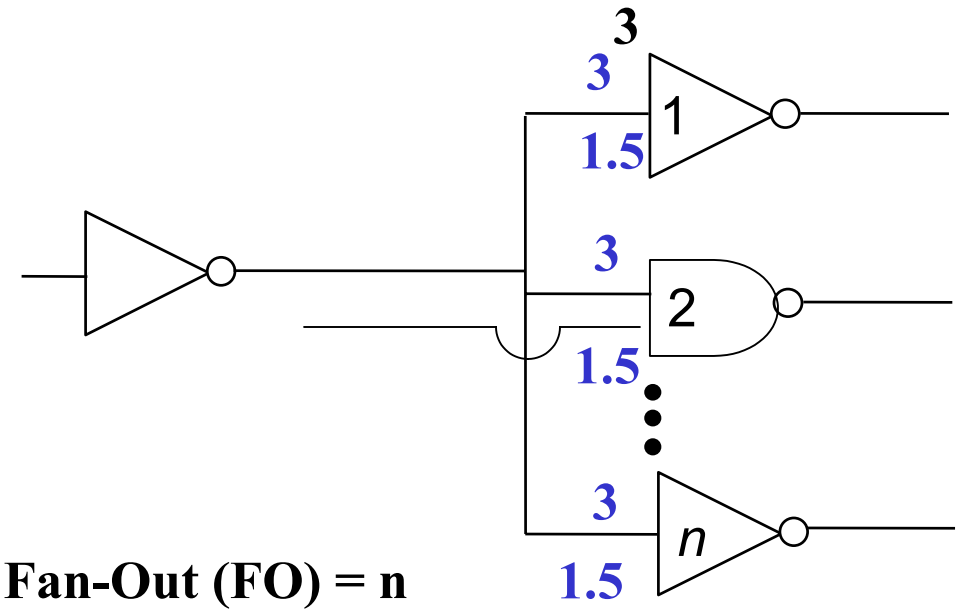
For comparison the inverter had a pull-up delay of 30 ps

Fanout

Lecture 24

Fanout is always ≥ 1 (there is always a load)

Gate capacitances sum and are charged by the driver resistance



Fan-Out (FO) = n

One load device was in included in the initial estimate of C_{LOAD}.

$$C'_{LOAD} = C_{LOAD} + (FO - 1)((W/L)_p + (W/L)_n)(C_{G/MS})$$

$$C'_{LOAD} = C_{LOAD} + (FO - 1)(1.5+3.0)(0.4\ fF)$$

Assumes minimum length devices.

Lecture 24

Coping with Power Consumption

D.C. POWER **a.c. POWER**

Tube: 300V x 20 mA = 6W

Bipolar Transistor: 5V x 20 mA = 200 mW

NMOS Transistor: 5V x 200 μA = 1 mW

CMOS Transistors: 5V x 100 nA = 0.5 μW

True of every gate!

$$P_{SHORT\text{-}CIRCUIT} = (1/2)\, I_{SHORT\text{-}CIRCUIT}\, V_{DD}\, \tau_{30\text{-}70}\, f_{CLOCK}$$

$$= (1/2)\,(60\ \mu A)\,2.5V\,(0.1ns)\,(10^9) = 7.5\ \mu W$$

Assumes ½ of the gates change state

$$P_{DYNAMIC} = (1/2)(1/2)\, C\, V_{DD}^{\,2}\, f_{CLOCK}$$

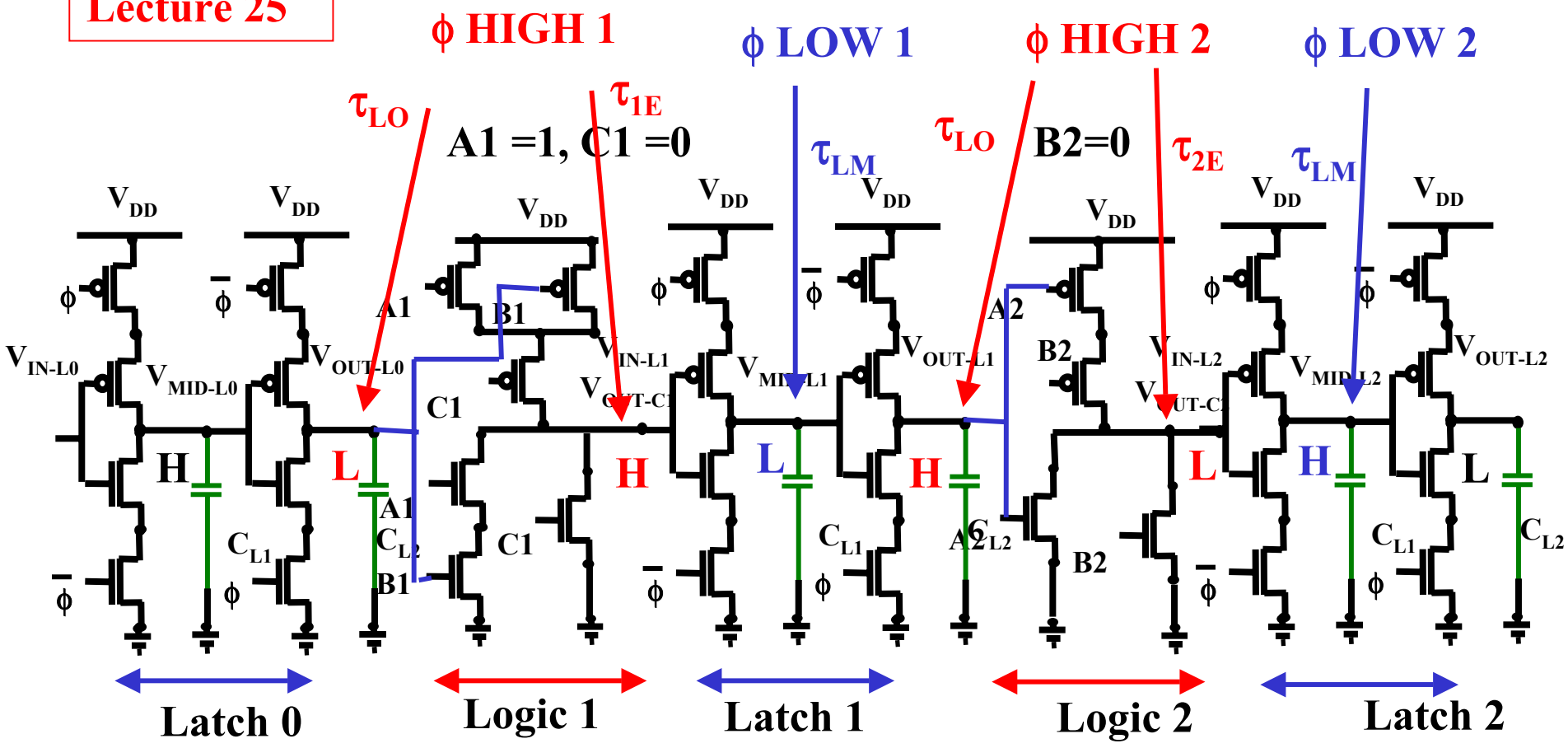
$$= (1/2)\,(1/2)(10\ fF)\,(2.5)^2\,10^9 = 15.6\ \mu W$$

Only the L =>H takes energy from V_{DD}

True for only active gates.

Combinatorial Logic and Clocked Latches: Signal Flow

HW 13
Lecture 25



$\tau_{\phi-HIGH} > \tau_{LO} + Max(\tau_{1E} \text{ or } \tau_{2E})$ $\quad \tau_{\phi-LOW} > \tau_{LM}$ $\quad f_{CLOCK} = 1/(\tau_{\phi-HIGH} + \tau_{\phi-LOW})$