Logic Circuit Supplement
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Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down device.
Terminology

\( V_{DD} \) = Power supply voltage

**Pull-Down Device** = Device used to carry current from the output node to ground to discharge the output node to ground.

**Pull-Up Device** = Device used to carry current from the power supply to the output node to charge the output node to the power supply voltage.

\( I_{OUT} \) = Current into the pull down device

\( V_{TD} \) = Value of \( V_{IN} \) at which the NMOS transistor begins to conduct.

\( V_{OUT-SAT-D} \) = Value of \( V_{OUT} \) beyond which the current \( I_{OUT} \) no longer increases in the NMOS.
States are Voltage Levels of $V_{IN}$

- **State 1 or $V_{IN} = 1V$**
- **State 3 or $V_{IN} = 3V$**
- **State 5 or $V_{IN} = 5V$**

The maximum voltage is $V_{DD}$

Current is flat (saturated) beyond $V_{OUT-SAT-D}$

Current is zero until $V_{IN}$ is larger than $V_{TD}$

$V_{OUT}(V)$

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Eliminating Point of Confusion

The use of $V_{TD}$ twice in the equation for $I_{OUT}$ is confusing (although it eliminates an extra parameter).

$$I_{OUT-PD} = k_D (V_{IN} - V_{TD}) V_{TD}$$

Instead we add an extra parameter to distinguish between threshold for conduction which is determined by $V_{IN}$ reaching $V_{TD}$ and saturation of the current level when $V_{OUT}$ reaches $V_{OUT-SAT-D}$.

$$I_{OUT-PD} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$
Single Equation EE42 NMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is larger than the threshold value $V_{TD}$ and the current is proportional to $V_{OUT}$ up to $V_{OUT-SAT-D}$ where it reaches

$$I_{OUT-PD} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold ($V_{TD}$) and saturation ($V_{OUT-SAT-D}$).

Example:

$k_D = 25 \mu A/V^2$

$V_{TD} = 1V$

$V_{OUT-SAT-D} = 1V$

$$I_{OUT-PD} = 25 \frac{\mu A}{V^2} (3V - 1V) lV = 50 \mu A$$

Use these values in the homework.
Single Equation EE42 PMOS Model

Current $I_{OUT}$ only flows when $V_{IN}$ is smaller than $V_{DD}$ minus the threshold value $V_{TU}$ and the current is proportional to $(V_{DD} - V_{OUT})$ up to $(V_{DD} - V_{OUT-SAT-U})$ where it reaches

$$I_{OUT-PU} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}$$

Example:
$k_U = 20 \, \mu A/V^2$
$V_{TU} = 1V$
$V_{OUT-SAT-u} = 1V$

Use these values in the homework.

$I_{OUT-PD} = 20 \frac{\mu A}{V^2} (5V - 3V - 1V) V = 20 \mu A$

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Composite $I_{OUT}$ vs. $V_{OUT}$ for CMOS

State 3 or $V_{IN} = 3V$

- PD current is flat (saturated) beyond $V_{OUT-SAT-D}$
- Pull-Down NMOS

- PU current is flat (saturated) below $V_{DD} - V_{OUT-SAT-D}$
- Pull-Up PMOS

The maximum voltage is $V_{DD}$

Solution
Voltage Transfer Function for the Complementary Logic Circuit

State 1 for $V_{IN} = 1V$

Vertical section due to zero slope of $I_{OUT}$ vs. $V_{OUT}$ in the saturation region of both devices.

State 3 for $V_{IN} = 3V$

State 5 for $V_{IN} = 5V$
Method for Finding $V_M$

At $V_M$,
1) $V_{OUT} = V_{IN} = V_M$
2) Both devices are in saturation
3) $I_{OUT-PD} = I_{OUT-PU}$

\[
I_{OUT-PD} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D} = k_U (V_{DD} - V_{IN} - V_{TU}) V_{OUT-SAT-U}
\]

Substitute $V_M$

Solve for $V_M$

Example Result: When $k_D = k_P$, $V_{OUT-SAT-D} = V_{OUT-SAT-U}$ and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$