Supplement #1: October 27, 2001

Logic Circuit Supplement

A) Transistor Inverter Example

B) Terminology and Using $V_{OUT-SAT-D}$

C) States are Voltage Levels of V_{IN}

D) Single Equation I_{OUT} vs. V_{OUT}

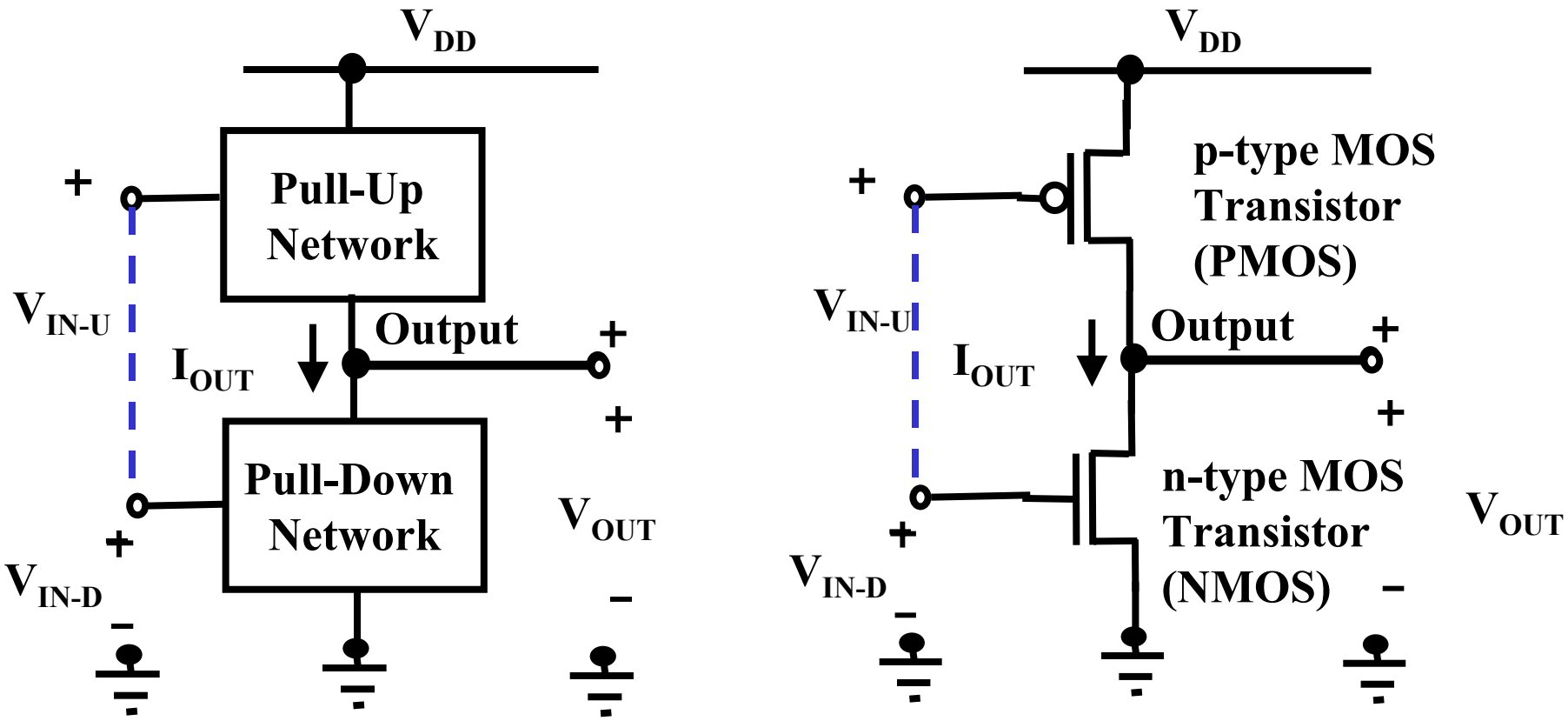
E) Composite I_{OUT} vs. V_{OUT} for $R_{PULL-UP}$

F) Composite I_{OUT} vs. V_{OUT} for Active Pull-Up

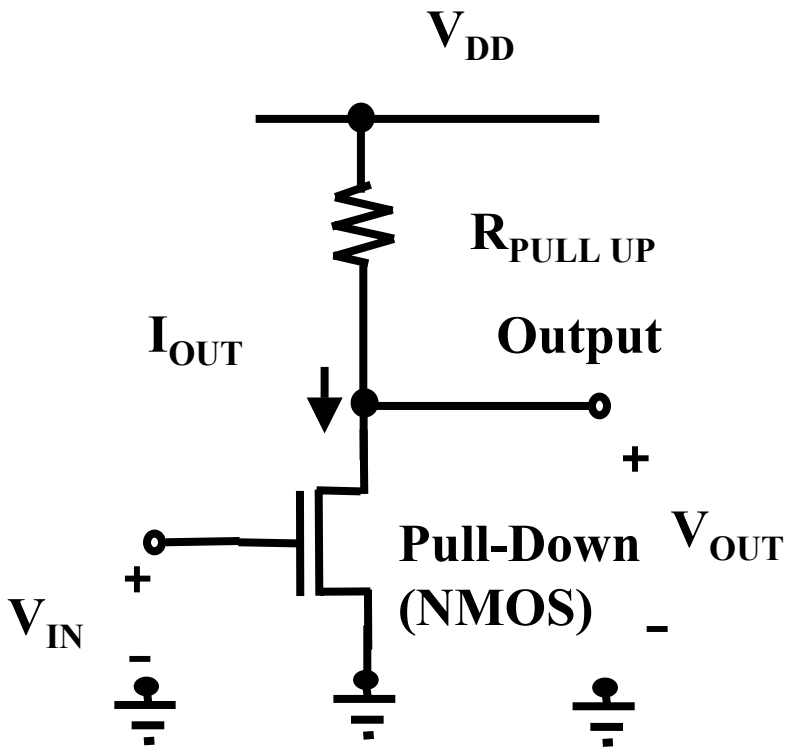
G) Voltage Transfer Function and V_M

Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down device.



Terminology



V_{DD} = Power supply voltage

Pull-Down Device = Device used to carry current from the output node to ground to discharge the output node to ground.

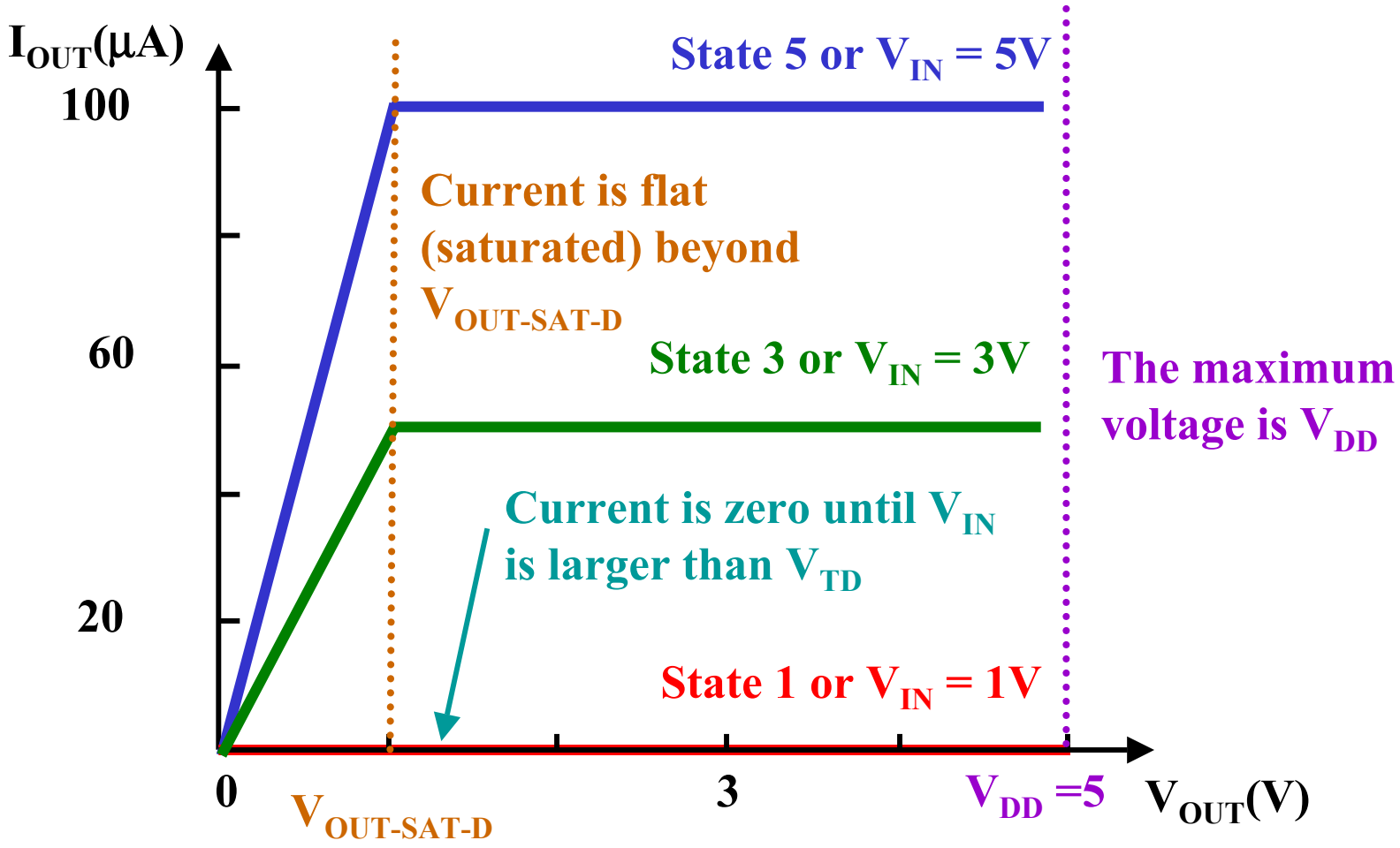
Pull-Up Device = Device used to carry current from the power supply to the output node to charge the output node to the power supply voltage.

I_{OUT} = Current into the pull down device

V_{TD} = Value of V_{IN} at which the NMOS transistor begins to conduct.

$V_{OUT-SAT-D}$ = Value of V_{OUT} beyond which the current I_{OUT} no longer increases in the NMOS.

States are Voltage Levels of V_{IN}



Eliminating Point of Confusion

The use of V_{TD} twice in the equation for I_{OUT} is confusing (although it eliminates an extra parameter).

$$I_{OUT-PD} = k_D\left(V_{IN} - V_{TD}\right)V_{TD}$$

Instead we add an extra parameter to distinguish between threshold for conduction which is determined by V_{IN} reaching V_{TD} and saturation of the current level when V_{OUT} reaches $V_{OUT\text{-}SAT\text{-}D}$.

$$I_{OUT-PD} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

Single Equation EE42 NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches

$$I_{OUT-PD} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:

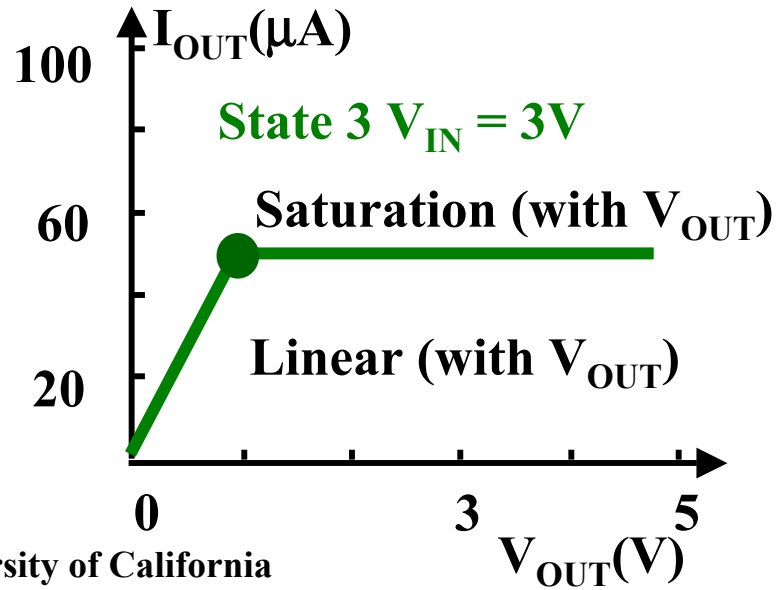
k_D = 25 μA/V²

V_{TD} = 1V

$V_{OUT-SAT-D}$ = 1V

Use these values in the homework.

$$I_{OUT-PD} = 25\frac{\mu A}{V^2}\left(3V - 1V\right)1V = 50\mu A$$



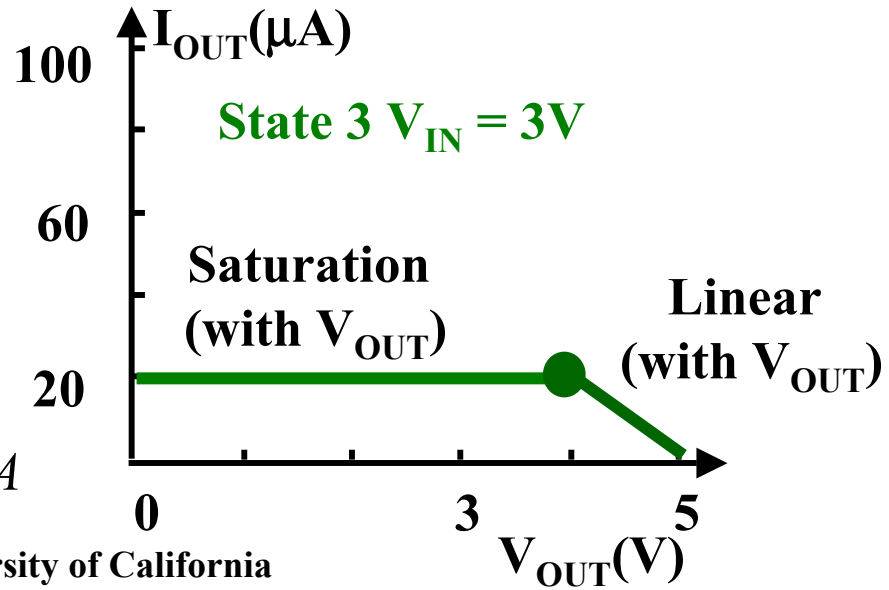
Single Equation EE42 PMOS Model

Current I_{OUT} only flows when V_{IN} is smaller than V_{DD} minus the threshold value V_{TU} and the current is proportional to (V_{DD}-V_{OUT}) up to (V_{DD}-$V_{OUT-SAT-U}$) where it reaches

$$I_{OUT-PU} = k_U\left(V_{DD} - V_{IN} - V_{TU}\right)V_{OUT-SAT-U}$$

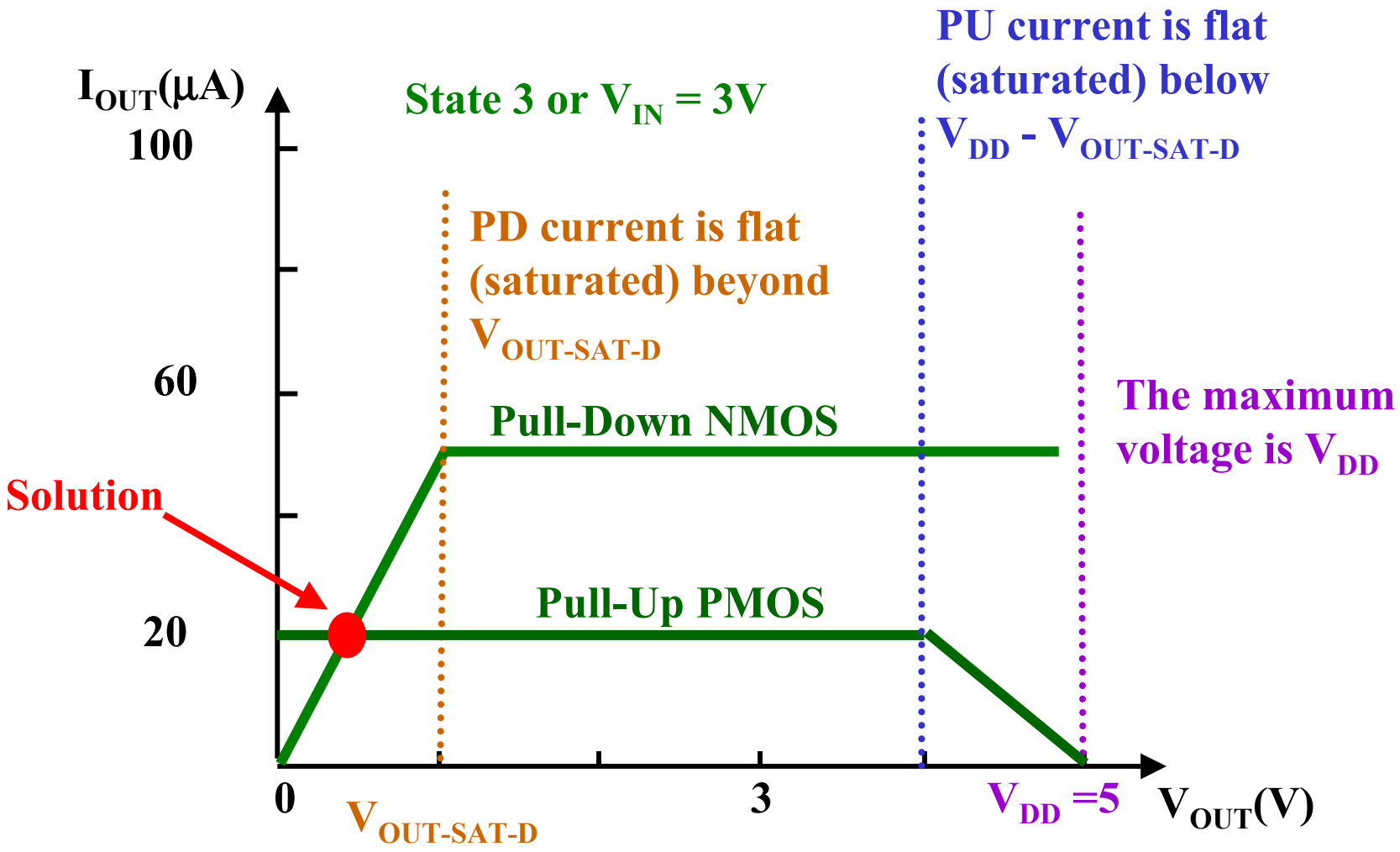
Example:
k_U = 20 μA/V²
V_{TU} = 1V
$V_{OUT-SAT-u}$ = 1V

Use these values in the homework.

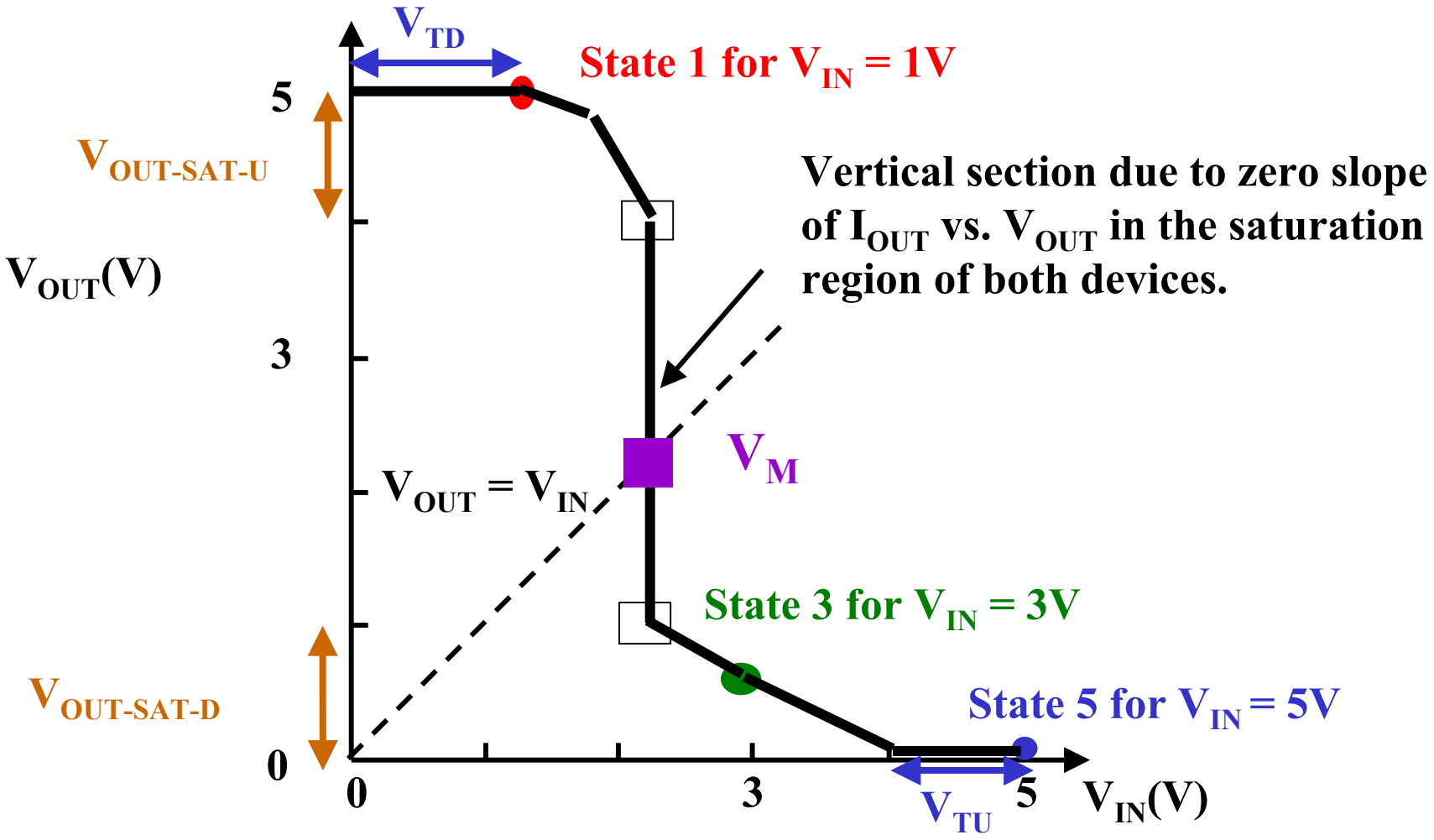


$$I_{OUT-PD} = 20\frac{\mu A}{V^2}\left(5V - 3V - 1V\right)1V = 20\mu A$$

Composite I_{OUT} vs. V_{OUT} for CMOS



Voltage Transfer Function for the Complementary Logic Circuit



Vertical section due to zero slope of I_{OUT} vs. V_{OUT} in the saturation region of both devices.

Method for Finding V_M

At V_M,

1) $V_{OUT} = V_{IN} = V_M$

2) **Both devices are in saturation**

3) $I_{OUT\text{-}PD} = I_{OUT\text{-}PU}$

$$I_{OUT-PD} = k_D \left(V_{IN} - V_{TD}\right) V_{OUT-SAT-D}$$

$$= I_{OUT-PU} = k_U \left(V_{DD} - V_{IN} - V_{TU}\right) V_{OUT-SAT-U}$$

Substitute V_M

Solve for V_M

Example Result: When $k_D = k_P$, $V_{OUT\text{-}SAT\text{-}D} = V_{OUT\text{-}SAT\text{-}U}$ and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$